A Modified Asymmetrical Pulse-Width-Modulated Resonant DC/DC Converter Topology

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Abstract - **A modified asymmetrical pulse-width-modulated resonant DC/DC converter employing an auxiliary circuit will be proposed in this paper. The auxiliary circuit consists of a network of two capacitors and an inductor. The aim of this network is to produce zero-voltage-switching (ZVS) over a wide input voltage range, while reducing the voltage and current stress across the resonant inductor. A detailed analysis is presented and performance curves are given. Experimental results for a 35 W, 5 V converter show an efficiency of about 81% at a constant operating frequency of 500 kHz.**

I. INTRODUCTION

In order to meet the requirements of point-of-use power supplies in telecommunication and computer systems, many constant frequency resonant converter topologies have been reported in the literature [1]-[5]. The goal of these topologies is to try and achieve high power density, high efficiency, low switching losses while operating at a constant frequency. In examining these topologies, their switching losses are low and they can be operated at high frequencies. Also, they offer high power density at medium to high power levels. However, their component count is high resulting in lower power densities at low to medium power levels. The asymmetrical pulse-width-modulated (APWM) resonant DC/DC converter topology [6],[7] has been presented and it offers near-zero switching losses while operating at constant and very high frequencies. Its component count is low, making operation at low to medium power levels feasible. The input voltage range over which ZVS is achieved is narrow, however, and the efficiency of the converter decreases as the input voltage is increased. Also, the resonant inductor incurs higher losses because of high voltage across it.

This paper discusses an auxiliary circuit that can be added to the APWM resonant DC/DC topology and can overcome the drawbacks described above. The network acts as a current compensation branch for the resonant stage as shall be described further.

The next section will give the description of this modified topology. Section III will present the mode of operation during each of the four intervals of one cycle and key waveforms of the circuit. Section IV covers the steady-state analysis. Section V presents the performance curves that aid in the design of the network. Section VI gives the experimental results of a 35 W 500 kHz prototype and section VII provides a comparison of the original topology and the improved one.

II. A MODIFIED APWM RESONANT DC/DC CONVERTER TOPOLOGY

Fig. 1 shows an APWM resonant DC/DC converter topology employing the additional network, which is shown within the dotted lines.

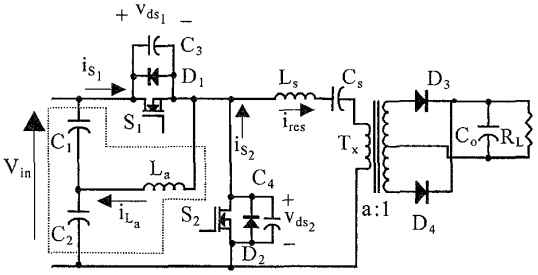

Fig. 1 Modified APWM Resonant DC/DC Converter Topology.

The above circuit can be broken down into functional blocks: the compensating network (C_1,C_2 and L_a), a chopper, a series-resonant tank (L_s&C_s), a power transformer (T_x), a rectifying block (D_3&D_4) and the output filter. The chopper consists of the two switches (S_1&S_2), the two snubber capacitors (C_3&C_4) and two anti-parallel diodes (D_1&D_2). With the presence of the auxiliary circuit, the switch current is the sum of the resonant current and the auxiliary current.

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III. OPERATING PRINCIPLE

This circuit consists of two switches, S_1 and S_2, which are controlled by two complementary gating signals, v_{gs_1} and v_{gs_2}, respectively. The gating signal of S_1 has a duty cycle of D and that of S_2 is 1-D. When S_1 is on, the power from the source is transferred to the load and the output of the chopper sees a positive voltage of V_{in} from the source. When S_2 turns on, the source is separated from the rest of the power circuit and the output of the chopper sees the voltage across S_2 which is zero volts. The energy from the resonant components now freewheels through S_2 and supplies power to the load. By varying D, we can control the output voltage. This requires a feedback network which increases D if the output voltage becomes too low and vice versa.

The operation of this circuit can be seen in four intervals. Fig.2 shows the key waveforms during each of these intervals. For each interval, the operation of the converter is described below.

Interval I: Prior to this interval, S_2 was switched on. At the beginning of this interval, the gate drive to S_2 is removed and this switch turns off. The currents flowing through the auxiliary inductor and the resonant branch are negative thus forcing the discharging of C_3 and the charging of C_4. This charging-discharging process is complementary, i.e. as C3 discharges from V_{in} to 0, C_4 charges from 0 to V_{in}. At any given moment throughout the cycle the total charge in both C_3 and C_4 is V_{in}. In order to maintain this, the voltage across L_a changes from $-V_2$ to V_1, where V_1 is the voltage across C_1 and V_2 is the voltage across C_2. Once C_3 has fully discharged and C_4 has fully charged, the negative currents force the conduction of diode D_1. The voltage across S_1 is now set at 0 volts.

Interval II: At the beginning of this interval, gating signal v_{gs_1} is applied to the gate of S_1 to switch it on. The current previously flowing through D_1 now flows through S_1. The switch thus turns on under zero voltage. The voltage across L_a remains constant at V_1. The voltage across S_2 is set at V_{in} during this interval since C_4 maintains its charge. Power flows from the input dc source to the resonant circuit and to the output load.

Interval III: At the beginning of this interval, the gate drive to S_1 is removed and this switch is turned off. The currents flowing through the auxiliary inductor and the resonant branch are negative thus forcing the charging of C_3 and the discharging of C_4. The voltage across L_a changes form V_1 to $-V_2$. Once C_3 has fully charged and C_4 has fully discharged, the positive currents force the conduction of diode D_2. The voltage across S_2 is now set at 0 volts.

Interval IV: At the beginning of this interval, gating signal v_{gs_2} is applied to the gate of S_2 to switch it on.

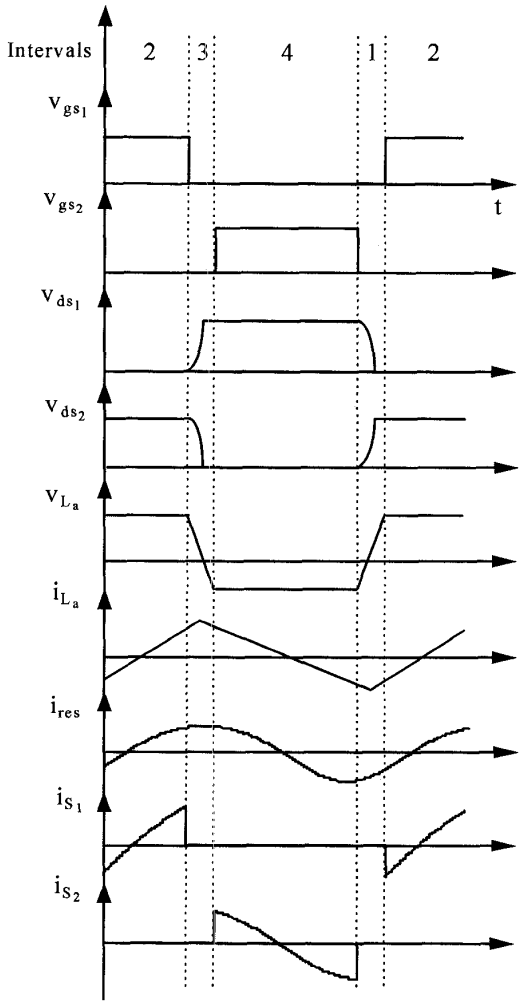

Fig. 2 Key waveforms of the circuit diagram in Fig. 1

The current previously flowing through D_2 now flows through S_2. The switch thus turns on under zero voltage. The voltage across L_a remains constant at $-V_2$. The voltage across S_2 is set at 0 during this interval since C_4 maintains its charge of 0 volts. To maintain a constant supply of power to the output load, the energy stored in the resonant components during Interval II now flows through S_2.

IV. STEADY-STATE ANALYSIS OF THE CONVERTER

This section will present the steady-state analysis of the circuit in Fig.1. In doing the analysis, the following assumptions will be made:

1) The semiconductor switches and diodes are ideal.
2) The effect of the capacitors across the switches is negligible.
3) The output rectification stage is represented by an ac equivalent resistance at the primary of the transformer.
4) The delay time between the two switches is neglected.

The minimum input voltage, $V_{in,min}$ (volts), the equivalent ac resistance R_{ac} (Ω), and the resonant frequency f_r (Hz) of the series resonant components are chosen as the base values. The following equations have been developed from the original circuit [1], but are still valid for this topology:

$$Q_o = \frac{2\pi f_r L_s}{R_{ac}} \tag{1}$$

$$\omega = \frac{f_o}{f_r} \tag{2}$$

$$R_{ac} = \frac{8}{\pi^2}\left(\frac{N_p}{N_s}\right)\cdot R_L \tag{3}$$

$$f_r = \frac{1}{2\pi\sqrt{L_s C_s}} \tag{4}$$

The voltage across S_2, v_{ds2}, is given by the following using Fourier series

$$v_{ds_2}(t) = V_{in}D + \sum_n \left[\frac{\sqrt{2}V_{in}}{n\pi}\cdot\sqrt{1-\cos 2n\pi D}\cdot\sin(n\omega_o t + \theta_n)\right] \tag{5}$$

where

$$\theta_n = \tan^{-1}\left[\frac{\sin 2n\pi D}{1-\cos 2n\pi D}\right] \tag{6}$$

The resonant current is derived from the ac component of v_{ds2}

$$i_s(t) = \sum_n \frac{\sqrt{2}V_{in}}{n\pi Z_{in}}\cdot\sqrt{1-\cos 2n\pi D}\cdot\sin(n\omega_o t + \theta_n - \phi_n) \tag{7}$$

where

$$Z_{in} = \sqrt{1+Q_o^2\left(n\omega - \frac{1}{n\omega}\right)^2} \tag{8}$$

$$\phi_n = \tan^{-1}\left[Q_o\left(n\omega - \frac{1}{n\omega}\right)\right] \tag{9}$$

In the above equations, $D=t_{on}/T$=effective duty cycle for switch S_1; n =nth order odd harmonic; V_{in}= dc input voltage; ω_o = fundamental switching frequency (r/s).

The current through the auxiliary inductor is given by

$$i_{L_a}(t) = \sum_n \left[\frac{\sqrt{2}I_z}{(n\pi)^2 D(1-D)}\cdot\sqrt{1-\cos 2n\pi D}\cdot\sin(n\omega_o t + \delta_n)\right] \tag{10}$$

where

$$I_z = \frac{D(1-D)V_{in}}{2f_o L_a} \tag{11}$$

$$\delta_n = \tan^{-1}\left[\frac{\cos 2n\pi D - 1}{\sin 2n\pi D}\right] \tag{12}$$

The voltage across this inductor is given by

$$v_{L_a}(t) = \sum_n \frac{\sqrt{2}V_{in}}{n\pi}\cdot\sqrt{1-\cos 2n\pi D}\cdot\sin(n\omega_o t + \delta_n) \tag{13}$$

As shown in Fig.2, the positive area of the inductor voltage is equal to the negative area, therefore no dc component exists.

V. PERFORMANCE CURVES OF THE CONVERTER

This section presents the steady-state characteristics of the converter. The analysis that was developed in the last two sections will be used in deriving the performance equations and curves. In order to simplify the design, it would be useful to relate the auxiliary inductor to the resonant inductor. If we define a variable K which relates L_s to L_a, i.e.

$$K = \frac{L_a}{L_s} \tag{14}$$

then we can redefine I_z in terms of K, ω and Q_o

$$I_z = \frac{D(1-D)\cdot V_{in}\cdot\pi}{K\cdot\omega\cdot Q_o} \tag{15}$$

This can then be used to plot the design curves. The curves are designed as follows:

Turn-off current I_2 of Switch S_2: In order to achieve ZVS for S_1, the current at the turn-off of S_2 must be negative. If we take the equations (7) and (10) and solve for them at $t=T_s$, we get the following

$$I_2 = \sum_n \frac{\sqrt{2}}{n\pi} \cdot \sqrt{1-\cos 2n\pi D} \left[\frac{V_{in}}{Z_{in}} \cdot \sin(\theta_n - \phi_n) + \frac{I_z \cdot \sin(\delta_n)}{(n\pi) D(1-D)} \right] \quad (16)$$

Figs. 3, 4 and 5 show I_2 as a function of D with various values for Q, ω, and K. Operation with ZVS is achievable over the range of K values listed, but the current through the auxiliary inductor and hence the current through the switches is inversely proportional to the value of the inductor, i.e. as the value of K (or L_a) decreases, the amount of current present increases.

Turn-off current I_1 of Switch S_1: In order to achieve ZVS for S_2, the current at the turn-off of S_1 must be positive. If we take equations (7) and (10) and solve for them at $t=DT_s$, we get the following

$$I_1 = \sum_n \frac{\sqrt{2}}{n\pi} \cdot \sqrt{1-\cos 2n\pi D} \left[\frac{V_{in}}{Z_{in}} \cdot \sin(2n\pi D + \theta_n - \phi_n) + \frac{I_z \cdot \sin(2n\pi D + \delta_n)}{(n\pi) D(1-D)} \right] \quad (17)$$

Figs. 6, 7 and 8 show I_1 as a function of D with various values for Q, ω and K. From these graphs, it is apparent that ZVS in S_2 is lost for high values of K. However, if K is too small, then the current through L_a and hence the switches becomes too big resulting in conduction losses. It is important that the right value of K is chosen for operation with ZVS and low conduction losses.

It is also evident from the previous graphs that the values of Q and ω chosen affect the amount of current passing through the switches. The chosen parameters should ideally present a low amount of current, but not at the expense of losing ZVS. Overall, the best results occur for Q_o=1.5 and ω=1.1. This shows that this circuit can operate at frequencies very close to the resonant frequency. The best value for the auxiliary inductor is K=1, which means that the auxiliary inductor and the resonant inductor can have the same value, thus lowering production costs.

VI. EXPERIMENTAL RESULTS

To verify this modified topology, a 35 W converter with dual 5 V outputs was constructed. The switching frequency is 500 kHz. In the resonant circuit, the following values were used: the resonant capacitor was 22 nF, the resonant inductor was 6.5 μH and the transformer turn ratio was 2.5 to 1. The value of the auxiliary inductor used was 6 μH, therefore K was

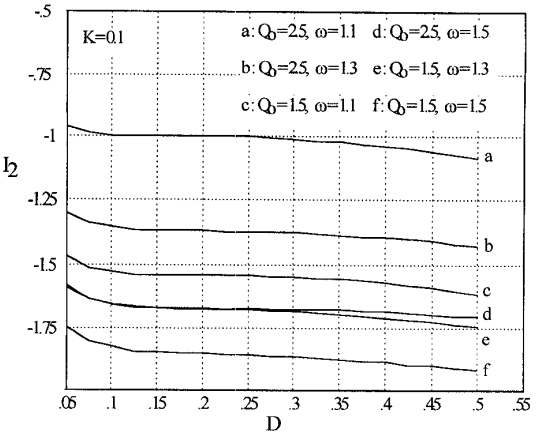

Fig. 3 Current through S_2 at turn-off, I_2, as a function of D for K=0.1

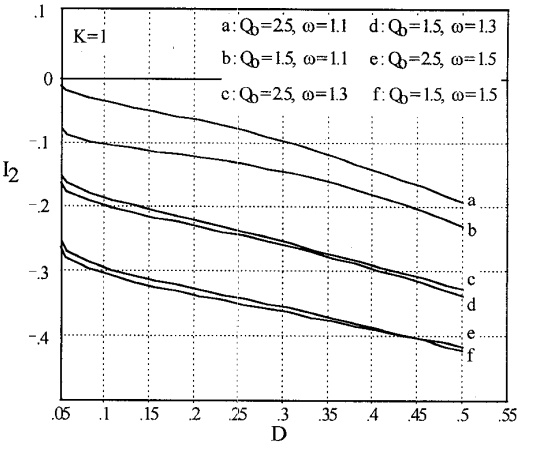

Fig. 4 Current through S_2 at turn-off, I_2, as a function of D for K=1

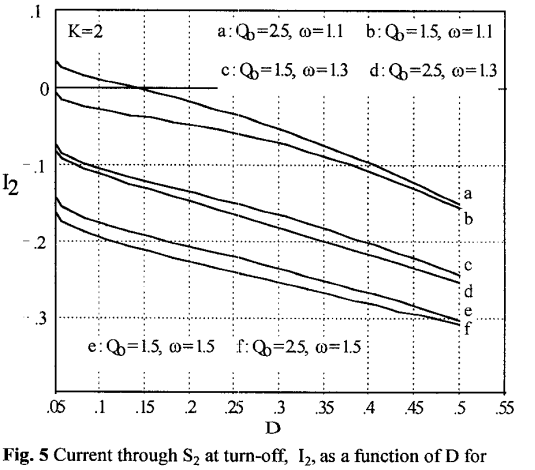

Fig. 5 Current through S_2 at turn-off, I_2, as a function of D for K=2

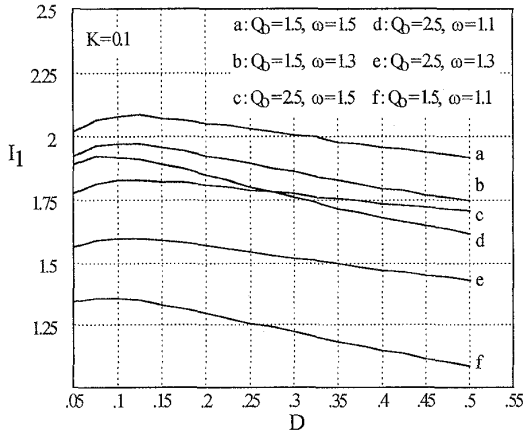

Fig. 6 Current through S_1 at turn-off, I_1, as a function of D for K=0.1

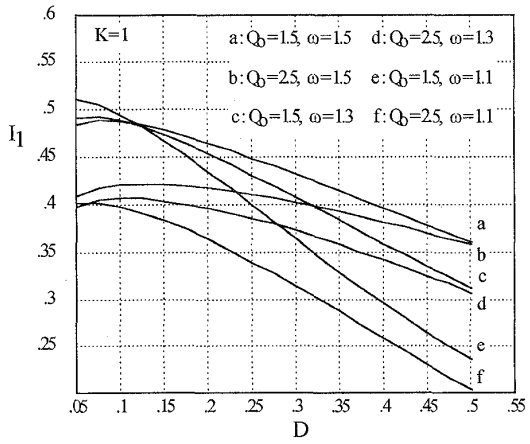

Fig. 7 Current through S_1 at turn-off, I_1, as a function of D for K=1

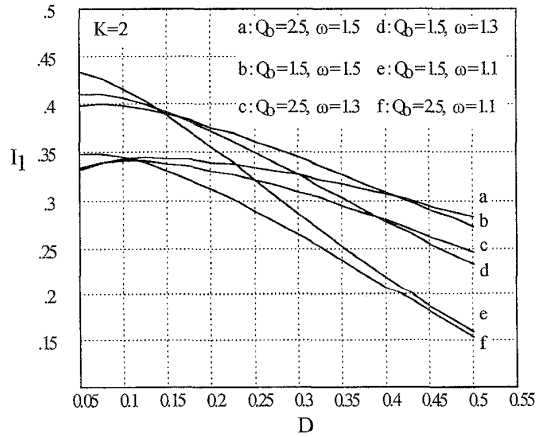

Fig.8 Current through S_1 at turn-off, I_1, as a function of D for K=2

close to 1. The capacitors in the auxiliary circuit (C_1, C_2) were chosen as 2.2 μF.

The main goal of the modified topology is to achieve ZVS for higher input voltages. Figs. 9 and 10 show the effect of ZVS at the turn-on of both switches, S_1 and S_2. The input voltage was set at 80 V at full load. On both figures, the dotted vertical line shows that the drain-to-source voltage reaches zero before the gate signal is applied.

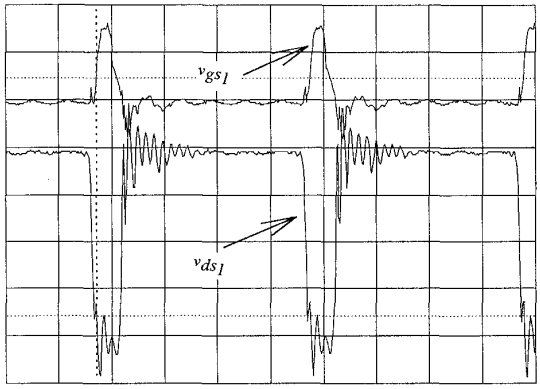

Fig. 9 Waveforms at turn-on of switch S_1. Top trace: gate signal (5 V/div, 5 μs/div). Bottom trace: drain-to-source voltage (20 V/div, 5 μs/div). Input voltage is 80 V, operating frequency is 495 kHz, output voltage is 4.8 V and output power is 30 W.

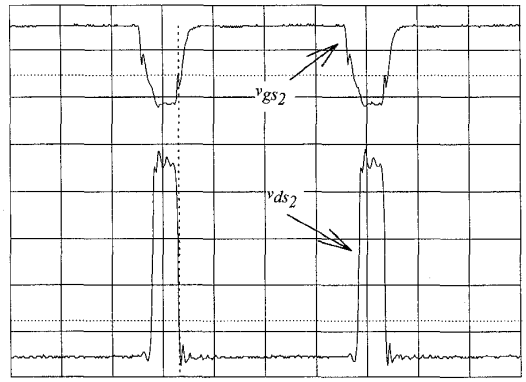

Fig. 10 Waveforms at turn-on of switch S_2. Top trace: gate signal (5 V/div, 5 μs/div). Bottom trace: drain-to-source voltage (20 V/div, 5 μs/div). Input voltage is 80 V, operating frequency is 495 kHz, output voltage is 4.8 V and output power is 30 W.

VII. COMPARISON BETWEEN ORIGINAL APWM CONVERTER AND MODIFIED TOPOLOGY

The mode of operation described in Section III is similar to the operation of the original APWM resonant DC/DC converter, yet at higher voltages ZVS is lost while this new topology maintains it. For example, at V_{in}=80 volts, Fig. 11 shows that ZVS is lost for S_1 in the original circuit. Notice that for S_1 to achieve ZVS,

the resonant current (which is also the current that flows through the switches) at the turn-off of S_2 must have enough negative current in order to discharge C_3 to zero volts for ZVS to occur. At 80 volts however, the resonant branch doesn't supply enough negative current to discharge C_3, therefore ZVS is lost. With the addition of the auxiliary branch however, it supplies the additional current to the switch in order to discharge C_3 and achieve ZVS. The current through this auxiliary branch acts as a compensation for the resonant current when the input voltage increases whereas earlier the original APWM was limited to a narrow range of input voltage.

It has just been described how the auxiliary inductor acts as a compensation for the resonant branch. The parameters of the resonant branch can therefore be improved as was explained earlier when looking at the performance curves. The value of Q_o can be reduced to 1.5 from 2.5 in the original circuit. This helps then in reducing the voltage stress across the inductor, $v_{L_s}(t)$,

$$v_{L_s}(t) = \sum \frac{\sqrt{2}\cdot V_{in}\cdot Q_o\cdot \omega}{\pi\cdot Z}\cdot\sqrt{1-\cos(2n\pi D)} \cdot\cos(n\omega_o t+\theta_n-\phi_n) \quad (18)$$

where $i_s(t)$ is the resonant current and it is given in eq. (7). The curves for $v_{L_s}(t)$ are shown in Fig. 12 with $Q_o = 2.5$ and $Q_o = 1.5$. As can be seen from Fig. 12, the inductor voltage of the original circuit will have notably higher frequency harmonics and thus higher core losses compared to the modified topology with $Q_o = 1.5$. The significant reduction in core losses of the modified topology will make the resonant inductor much easier to manufacture.

Figure 13 shows the efficiency, η, of the modified topology and the original one in relation with the input voltage. It is easily seen that overall the modified topology has a higher efficiency than the original

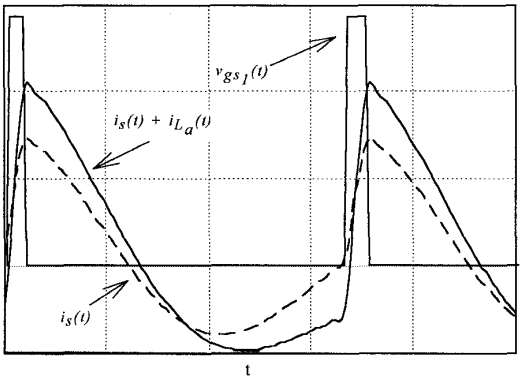

Fig. 11 Waveforms of original and modified APWM resonant DC/DC converter with K=1, Q=2.5 and ω=1.2.

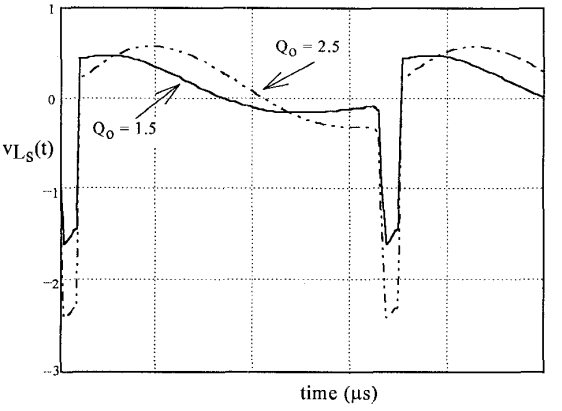

Fig. 12 Voltage across resonant inductor for Q=2.5 (original circuit) and Q=1.5 (modified circuit).

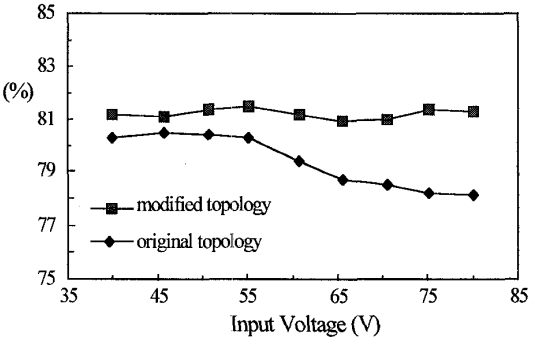

Fig. 13 Efficiency, η, of original APWM resonant DC/DC converter and modified topology with variation of input voltage.

design, but this is more evident at higher voltages where the efficiency of the original design begins to fall after 55 V. The main reason for this is the loss of ZVS and soft switching at higher voltages. The efficiency of the modified topology however is consistent at 81% throughout the whole input voltage range with a variation of about 1% due to the fact that ZVS is maintained.

Figure 14 shows the efficiency, η, of the modified topology and the original one in relation with the load current. It can be seen that the modified topology shows about 2% higher efficiency than the original converter.

VIII. CONCLUSION

This paper has presented a modified design of the APWM resonant DC/DC converter topology. Its operation principle and steady-state analysis has been described in detail. It has been proved with the aid of performance curves and experimental results that the modified topology achieves ZVS over a wider input

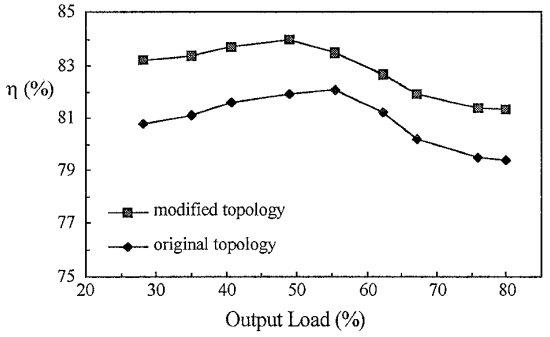

Fig. 14 Efficiency, η, of original APWM resonant DC/DC converter and modified topology with variation of output load.

voltage range than the original design. The converter also maintains near constant efficiency from low-to-high input voltage and 20-80% output load.

ACKNOWLEDGMENTS

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