A NOVEL ZERO VOLTAGE SWITCHED (ZVS) BUCK CONVERTER USING COUPLED INDUCTOR

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ABSTRACT

A novel zero-voltage switched (ZVS) Buck converter using coupled inductor is proposed in this paper. An additional winding is added on the same core of the output filter inductor for the purpose of commutation. The output inductor current is kept in continuous conduction mode (CCM) with small ripple. ZVS conditions for both switches are satisfied over wide load range. The converter can be operated at a fixed switching frequency. High switching frequency and high efficiency can be achieved due to soft switching. The proposed converter is analyzed in detail. Simulation is used to verify the analysis. The concept of ZVS using coupled inductor can also be applied to other PWM converters. ZVS-Boost and ZVS-Buck-Boost converters are derived based on the same concept.

1.INTRODUCTION

Switching mode power supplies are widely used in industrial, residential and aerospace environments. They play an important role in modern telecommunication systems as well. The advancement in computer and communication technology requires that the power supplies have high efficiency and high power density. The sizes of filter components and isolated transformers are determined by the switching frequency. To achieve high power density, high switching frequency is necessary. However, the increase of switching frequency results in an increase of switching loss and decreases the efficiency of the conventional Pulse Width Modulated (PWM) converters [1].

To achieve high efficiency in PWM converters, soft switching is required. Zero Voltage Switched (ZVS) technique and Zero Current Switched (ZCS) technique are two commonly used soft switching methods.

Quasi-resonant converters (QRCs) were introduced in [2-3] to overcome the disadvantage of PWM converters operating at high switching frequency. They can be viewed as the hybrid of the resonant converters [4] and PWM converters. In QRCs, switches can be turned on at zero voltage or turned off at zero current. However, the switches in QRCs withstand high voltage stress or high current stress. Also, the switching frequency changes over a wide range when the load changes.

In Zero Voltage Transition (ZVT) [5] and Zero Current Transition (ZCT) [6] converters, commutation cells are introduced to improve the switching conditions of the main switches. However, the auxiliary switches still have some switching loss during turn on or the circulating current is comparatively large.

Among all the PWM converters, Buck converters are the simplest ones. The attractive advantages include few components, low voltage and current stresses and easy to be implemented. They are widely used in low and medium power applications.

In [7, 8], Zero Voltage Resonant Transition (ZVRT) Buck converters were proposed where the output inductor is comparatively small. This converter is shown in Fig. 1. In this converter, the inductor current is bi-directional so that both switches have ZVS conditions. Fig. 2 shows the inductor current waveform. However, this converter has some drawbacks. Large ripple current exists in the output inductor. To obtain output voltage with small ripple, large output filter capacitor is needed. The other drawback is that the switching frequency changes during power regulation, which makes it difficult to optimize the filter components. This converter is only suitable for low power applications. These problems are addressed in this paper.

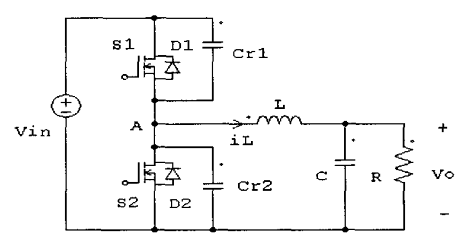


Fig. 1 ZVRT Buck converter

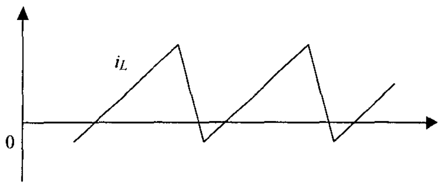


Fig.2 Bi-directional inductor current

In this paper, a new ZVS Buck converter is proposed. It maintains the advantages of traditional PWM converters and the ZVRT Buck converters. There is an additional winding on the same core of the output inductor. The voltage across the auxiliary inductor can be used for the purpose of commutation. By this method, the output inductor current is continuous with small ripple as in traditional Buck converters. At the same time, the ZVS conditions for switches are satisfied. The proposed converter can operate at fixed switching frequency during load regulation or input voltage variation.

2. ZVS BUCK CONVERTER USING COUPLED INDUCTOR

The proposed ZVS Buck converter using coupled inductor is shown in Fig.3. Inductor L_2 and L_1 are tightly coupled on the same ferrite core. The polarities of the inductor L_2 and L_1 are marked as in Fig.3 to ensure that the voltage across the coupled inductor (L_2) can be used as the commutation source for soft switching for MOSFETs.

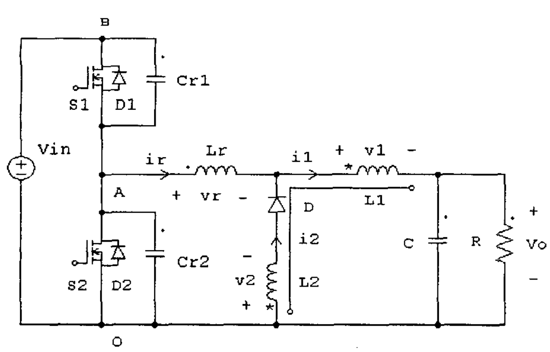


Fig.3 ZVS Buck converter using coupled inductor

The inductor L_r is small while the output inductor L_1 is comparatively large. The commutation cell is consisted of L_r, D and L_2. By introducing such commutation cell, current i_r can be bi-directional while the output current i_1 has small ripple. Bi-directional current in L_r ensures ZVS conditions for the two MOSFETs. Small ripple output current allows higher output power and lower requirements of the output filter capacitors.

3. PRINCIPLE OF OPERATION

To simplify the analysis, all the switching components are treated as ideal. Also, assume that the converter is in steady state operation. There are seven operating modes as illustrated in Fig.4. The circuit configurations during these modes are shown in Fig.5 and described as follows.

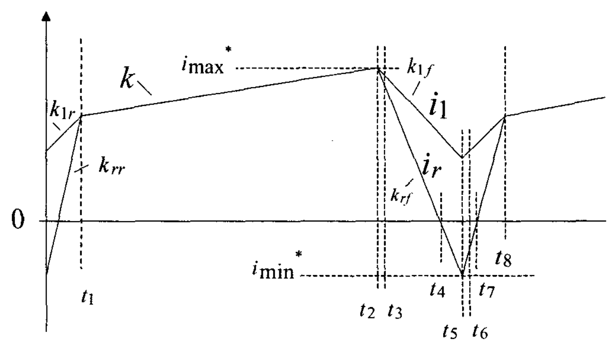


Fig.4 Waveforms of i_r and i_1

Mode 1 [t_1-t_2]: at time t_1, S_1 is turned on and D is off. L_r is in series with L_1. The current i_r will rise linearly at the slope of $k = \frac{V_{in} - V_o}{L_1 + L_r}$. When the current reaches the current reference i_{max}^* that is the output of voltage regulation loop, S_1 is turned off.

Mode 2 [t_2-t_3]: When S_1 is turned off at t_2, resonance occurs between the inductor L_r and snubber capacitors (C_{r1}, C_{r2}). In this interval, C_{r1} is charged and C_{r2} is discharged. At time t_3, the voltage across C_{r2} becomes zero and D_2 begins to conduct.

Mode 3 [t_3-t_4]: When D_2 conducts, the voltage across the output inductor (v_1) changes its polarity. Because inductor L_2 and L_1 are tightly coupled, v_2 is negative. The current in L_r begins to decrease due to the voltage of L_2. Because L_r is comparatively small, its current will decrease much faster than that of L_1. As long as D_2 is on, the gate signal can be applied to S_2 so that S_2 can be turned on at zero voltage.

During this mode,

$$\begin{cases} v_2+v_1+V_o=o \\ v_2=v_r \end{cases} \quad (1)$$

Where

$$v_1=L_1\frac{di_1}{dt}+M\frac{di_2}{dt} \quad (2)$$

$$v_2=L_2\frac{di_2}{dt}+M\frac{di_1}{dt} \quad (3)$$

$$v_r=L_r\frac{di_r}{dt} \quad (4)$$

$$i_2=i_1-i_r \quad (5)$$

$$M=\sqrt{L_1L_2} \quad (6)$$

By substituting (2)-(6) into (1), the current slopes in three inductors can be derived as follows.

$$k_{1f}=\frac{di_1}{dt}=-\frac{V_o(L_2+L_r)}{(L_1+L_2+2M)L_r} \quad (7)$$

$$k_{2r}=\frac{di_2}{dt}=\frac{V_o(M-L_r)}{(L_1+L_2+2M)L_r} \quad (8)$$

$$k_{rf}=\frac{di_r}{dt}=-\frac{V_o(L_2+M)}{(L_1+L_2+2M)L_r} \quad (9)$$

Equations (7)-(9) show that the current in L_2 rises while the currents in L_r and L_1 decrease. Also, it can be seen that i_r decreases much faster that i_1.

Mode 4 [t_4-t_5]: at time t_4, i_r reduces to zero and S_2 begins to carry current. The current rises in opposite direction. The equivalent circuit is the same as in ***Mode 3***. When i_r reaches the current reference $i_{\min}^*$ at time t_5, S_2 is turned off. The value of $i_{\min}^*$ is set by controller to make sure that the energy stored in L_r is large enough to charge and discharge the snubber capacitors thoroughly so that ZVS conditions can be satisfied.

Mode 5 [t_5-t_6]: When S_2 is turned off, resonance occurs between the inductor L_r and the snubber capacitors (C_{r1} and C_{r2}). This mode is similar to ***Mode 2.*** C_{r1} is discharged while C_{r2} is charged. At time t_6, the voltage across C_{r1} becomes zero.

Mode 6 [t_6-t_7]: D_1 begins to conduct. During this duration, i_r and i_1 begin to increase. The conduction of D_1 makes it possible for S_1 to be turned on at zero voltage. At time t_7, i_r will be equal to zero. During this mode,

$$\begin{cases} v_2+v_1+v_o=o \\ v_r=V_{in}+v_2 \end{cases} \quad (10)$$

Substitute (2)-(6) into (10),

$$(L_1+L_2+2M)\frac{di_1}{dt}-(L_2+M)\frac{di_r}{dt}+V_o=o \quad (11)$$

$$-(L_2+M)\frac{di_1}{dt}+(L_2+L_r)\frac{di_r}{dt}=V_{in} \quad (12)$$

The current slopes in L_1, L_2 and L_r can be expressed as following equation.

$$k_{1r}=\frac{di_1}{dt}=\frac{L_2}{L_r(L_2+M)}V_{in}-\frac{V_o(L_2+L_r)}{(L_1+L_2+2M)L_r} \quad (13)$$

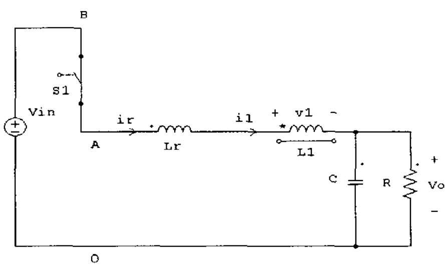
$$k_{2r}=\frac{di_2}{dt}=-\frac{M}{L_r}V_{in}+\frac{V_o(M-L_r)}{(L_1+L_2+2M)L_r} \quad (14)$$

$$k_{rr}=\frac{di_r}{dt}=\frac{V_{in}}{L_r}-\frac{V_o(L_2+M)}{(L_1+L_2+2M)L_r} \quad (15)$$

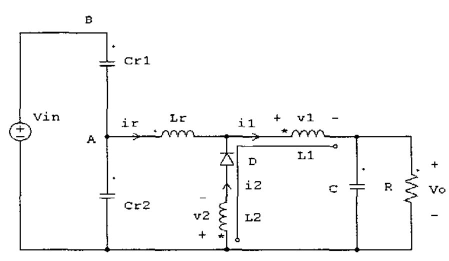
Investigation of equations (13) - (15) will find that the current in L_r rises much faster than that in L_1. At the same time, current in L_2 will decay.

Mode 7 [t_7-t_8]: i_r and i_1 continue to increase. At time t_8, i_r will be equal to i_1 so that current in inductor L_2 becomes zero.

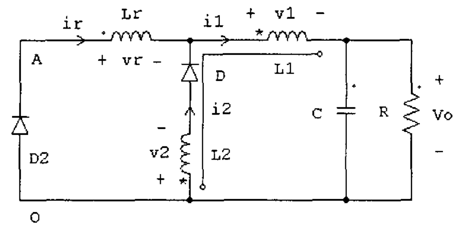
In the next switching cycle, the above seven modes repeat.



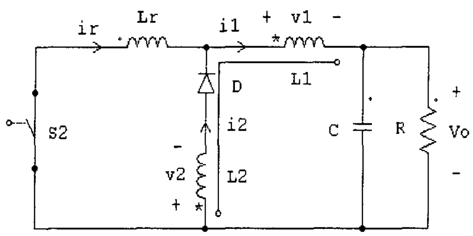
(a) Mode 1: S_1 conducts



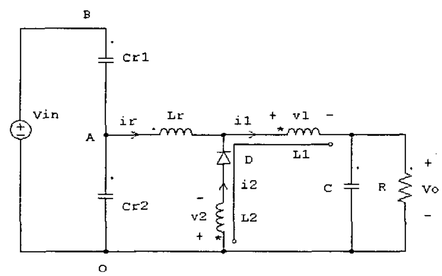
(b) Mode 2: L_r, C_{r1} and C_{r2} resonant



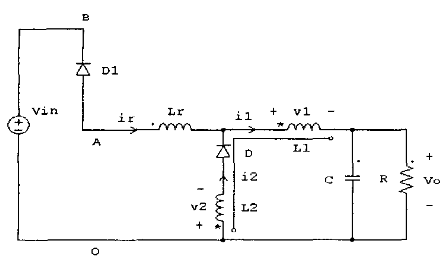
(c) Mode 3: D_2 conducts



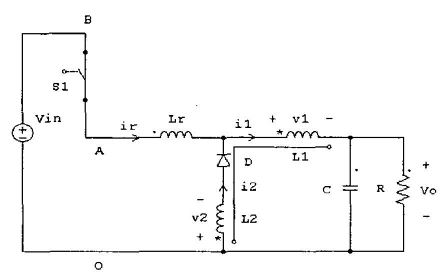
(d) Mode 4: S_2 conducts



(e) Mode 5: L_r, C_{r1} and C_{r2} resonant



(f) Mode 6: D_1 conducts



(g) Mode 7: S_1 and D conduct

Fig 5: Severn operation modes in the proposed converter

4. CONTROL STRATEGY

To achieve ZVS conditions in the proposed converter, Current Mode Control (CMC) will be adopted. The proposed ZVS Buck converter with real time CMC is shown in Fig.6.

The Zero Voltage Detector (ZVD) circuits are used to detect the zero voltage conditions of two MOSFETs. ZVD circuits ensure that MOSFETs are turned on at zero voltage. When the voltage across the MOSFET is zero, gate signal is applied to the switch.

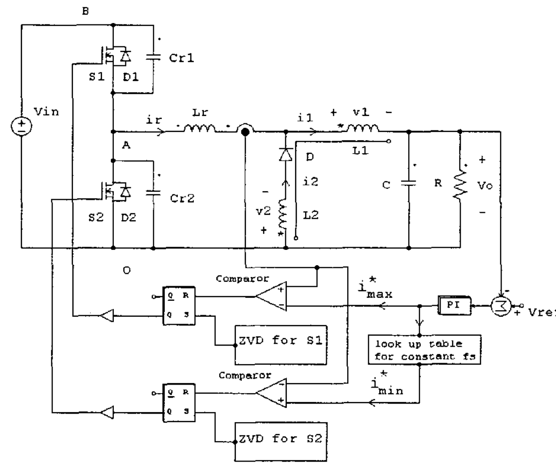


Fig.6 Peak current mode control block

The output of the voltage regulation loop, which is i_{max}^* as in Fig.6, serves as the upper boundary for the current i_r. The lower boundary i_{min}^* is designed to ensure ZVS conditions for the switches.

$$\frac{1}{2} L_r {i_{min}^*}^2 > C_r V_{in}^2 \tag{16}$$

(Here, suppose $C_{r1}=C_{r2}=C_r$)

$$i_{min}^* > \sqrt{\frac{2C_r}{L_r}} V_{in} \tag{17}$$

When current i_r reaches either the upper boundary or lower boundary, the corresponding switch will be turned off. Namely, S_1 is turned off when current i_r reaches the upper boundary. S_2 is turned off when i_r reaches the lower boundary.

5. SWITCHING FREQUENCY

Switching frequency (f_s) is another consideration of design. If the lower boundary i_{min}^* is fixed, then the switching frequency will change when the load current changes. It is shown in Fig.7. The higher the output current, the lower the switching frequency will be. Variable switching frequency makes it difficult to optimize the filter components.

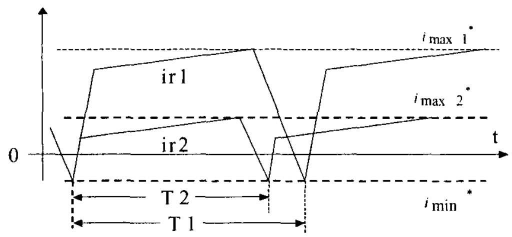


Fig.7 variable f_s operation

If the lower boundary i_{min}^* can be changed according to i_{max}^*, then the switching frequency can be kept constant during load regulation as shown in Fig.8. A look up table can be used to achieve constant switching frequency operation (Fig.6).

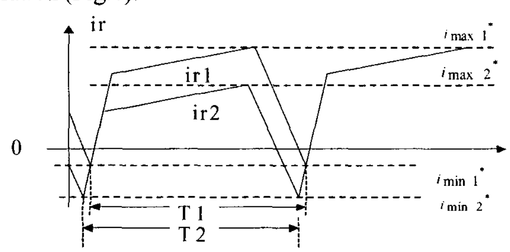


Fig.8 constant f_s operation

6. SIMULATION RESULTS

To verify the above analysis, the proposed ZVS Buck is simulated in PSPICE. The switching waveforms for two MOSFETs are shown in Fig.9, Fig.10 respectively. From the figures, the MOSFETs are turned on at zero voltage so that the turn on switching loss will be zero. During turn off stages, the voltages across the MOSFETs rise softly due to snubber capacitors. The total switching loss will be very small.

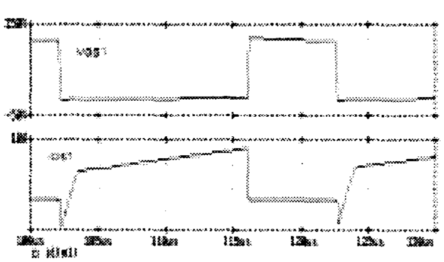


Fig.9 switching waveforms in MOSFET1
(upper: voltage, lower: current)

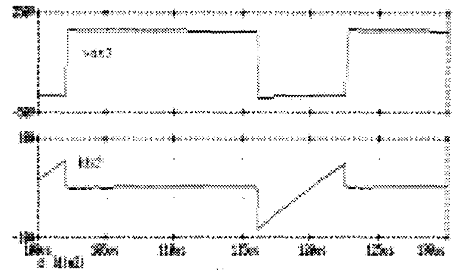


Fig.10 switching waveforms in MOSFET2
(upper: voltage, lower: current)

The currents in L_r and L_1 are shown in Fig.11. The current i_r is bi-directional while the output current i_1 has smaller ripple current. The simulation results verify the analysis in section 3.

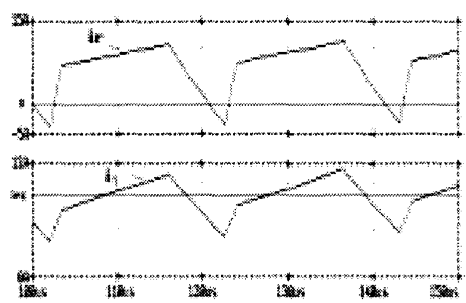


Fig.11 currents in L_r and L_1,
(Upper: Current in L_r, Lower: Current in L_1)

7. OTHER ZVS CONVERTERS

The concept of achieving ZVS with coupled inductor can be applied to other PWM converters such as Boost converter and Buck-Boost converter. Fig.12, 13 show the ZVS-Boost converter and ZVS Buck-Boost converter. These converters will be studied in the future.

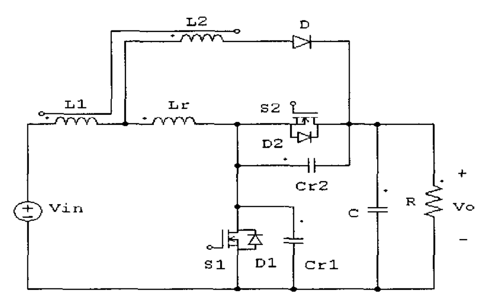


Fig.12 ZVS- Boost converter

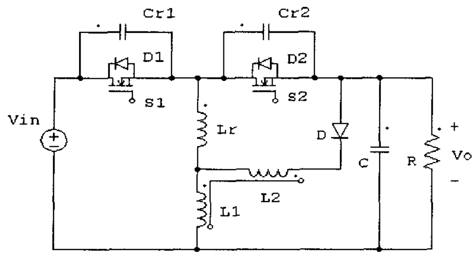


Fig.13 ZVS- Buck-Boost converter

8. CONCLUSIONS

The study shows that the novel soft switching technique using coupled inductor proposed in this paper has significantly improved the performance of the conventional ZVRT converters. The output inductor current is continuous with small ripple and at the same time ZVS conditions for the switches are satisfied. Simulation results show that ZVS conditions can be met over a wide range of load current. The turn on loss is zero while the turn off loss is very small due to snubber capacitors. As a result switching loss is almost eliminated and the converter can be operated at high switching frequency. This will result in high efficiency. The converter can also operate at fixed switching frequency. Peak current mode control is used to regulate the output voltage and to ensure the ZVS conditions. Other ZVS converters are derived using the same concept for soft switching. Further detailed studies are underway for these converters.

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