The normalized switch-rating difference of the AF and the CSR is, similar to $\Delta S_{\rm kVA}$, introduced by

$$\Delta I_{\rm sw} = \frac{I_{\rm sw}^{\rm AF} - I_{\rm sw}^{\rm CSR}}{I_{\rm sw}^{\rm CSR}} \times 100[\%]. \quad (15)$$

The switch-rating difference as a function of the firing angle is illustrated in Fig. 3(d). It is seen that the average and rms current ratings of the AF, operated with the firing angle less than 45°, are lower than the CSR current ratings. For large angles ($\alpha > 62°$), the AF current ratings are more than twice higher than the CSR ratings, due to the AF current increase associated with the increased reactive-power level. Therefore, the AF implementation for high-reactive-power compensation is not considered as a viable solution in terms of the switch current rating as well as the converter rating.

IV. Conclusion

Theoretical derivations and analytical approaches are presented for the two CSR topologies to obtain the sinusoidal supply current and the unity displacement power factor in the utility: a CSR and a PCR combined with an AF. In general, the AF rating connected with the PCR operating with a small firing angle is lower than the CSR rating. However, the kilovoltampere rating of the AF subject to a large firing angle is much higher than that of the CSR. Furthermore, the AF rating shows more sensitivity to the increase of input filter size than the CSR rating. Thus, the AF is not a viable solution in high-power applications with a large input inductor and a PCR subject to the large firing angle. The AF for the PCR with firing angle less than 45° results in lower switch ratings than the CSR. The large firing angle ($\alpha = 70°$) yields three-times-higher switch ratings of the AF than those of the CSR. The high switch ratings make the AF applications for high-reactive-power compensation very costly, along with the high AF kilovoltampere rating.

References

[1] S. Buso, L. Malesani, P. Mattavelli, and R. Veronese, "Design and fully digital control of parallel active filters for thyristor rectifiers to comply with IEC-1000-3-2 standards," *IEEE Trans. Ind. Appl.*, vol. 34, no. 3, pp. 508–517, May/Jun. 1998.

[2] J. R. Espinoza and G. Joos, "State variable decoupling and power flow control in PWM current-source rectifiers," *IEEE Trans. Ind. Electron.*, vol. 45, no. 1, pp. 78–87, Feb. 1998.

[3] T. Thomas, K. Haddad, G. Joos, and A. Jaafari, "Design and performance of active power filters," *IEEE Ind. Appl. Mag.*, vol. 4, no. 5, pp. 38–46, Sep./Oct. 1998.

[4] J. H. Marks and T. C. Green, "Rating analysis of active power filters," in *Proc. IEEE PESC*, vol. 3, 2001, pp. 1420–1425.

[5] S. Bhattacharya, T. M. Frank, D. M. Divan, and B. Banerjee, "Active filter system implementation," *IEEE Ind. Appl. Mag.*, vol. 4, no. 5, pp. 47–63, Sep./Oct. 1998.

[6] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics*, 2nd ed. New York: Wiley, 1995.

New Digital Control Method for Power Factor Correction

Wanfeng Zhang, Guang Feng, Yan-Fei Liu, and Bin Wu

***Abstract*—For conventional digital power-factor correction (PFC) control methods, the duty cycle is calculated in every switching period. One main implementation barrier for the digital control of PFC is the limited switching frequency due to the limited processor speed. A new digital PFC control method is proposed to solve this problem. Based on the input current and duty cycles of the previous half-line periods, the new digital PFC control method uses an optimization algorithm to generate all of the duty cycles in advance, which are required to achieve PFC for one half-line period. Total harmonic distortion, which is directly related to the power factor, is adopted as the objective function. The proposed new digital PFC control strategy overcomes the problem of limited switching frequency due to a limited digital signal processor (DSP) speed. The proposed algorithm can be implemented by a low-cost DSP. Simulation results show that unity power factor is achieved using the proposed method.**

***Index Terms*—Digital control, optimization, power-factor correction.**

I. Introduction

Power-factor correction (PFC) is necessary for ac-to-dc switched mode power supplies to comply with the requirements of international standards. With the development of digital technique, many control algorithms are implemented by a digital system because it has many advantages over an analog control. Digitally controlled PFC techniques have been explored by many researchers [1]–[3]. Unfortunately, all of the conventional control methods cannot take full advantage of the digital technique. In addition, the switching frequencies of the converters are limited by the speed of the digital signal processor (DSP) [4], [5].

A new digital PFC control method is proposed in this paper. Different from the conventional digital control methods in which the duty cycle is calculated at every switching cycle, the proposed digital PFC control method uses an optimization algorithm to generate all of the duty cycles in advance so as to achieve unity power factor in a half-line period. One of the significant characteristics of the proposed digital PFC control strategy is that the switching frequency is not directly dependent on the speed of the DSP. Therefore, a low-cost DSP/microprocessor could be used to control the switch operating at a high switching frequency.

II. New Digital PFC Control Method

It is noted that in ac-to-dc converters, there is a duty cycle set D to achieve unity power factor in every half-line period. For example, if a Boost PFC circuit operates at a switching frequency of $f_s = 100$ kHz and a line frequency of $f_{\rm line} = 50$ Hz, the number of duty cycles in one half-line period is 1000 ($= 100\,000/2 \times 50$). It means that

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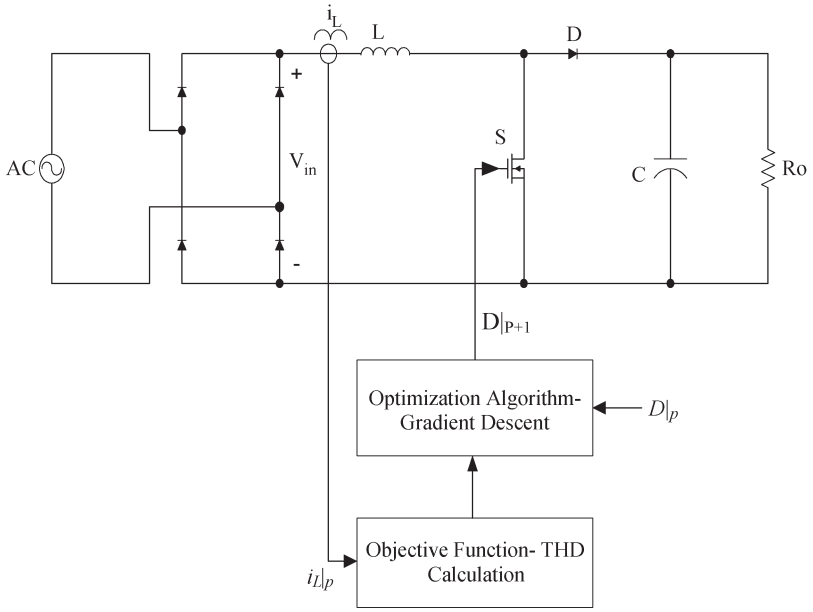

Fig. 1. Proposed new digital control PFC scheme.

in every half-line period, there are 1000 specific duty cycles, i.e., $d_1, d_2, \ldots, d_{1000}$, to achieve unity power factor. The duty cycle set, which consists of these specific duty cycles, can also achieve unity power factor. The problem lies on how these duty cycles can be determined.

A new digital PFC control method is proposed to solve this problem. One key point of the proposed control method is that all the required duty cycles for a half-line period are generated in advance. Another key point is that an optimization algorithm is used to search the required duty cycles to achieve unity power factor.

Fig. 1 illustrates the principle of the proposed new digital control PFC strategy. In Fig. 1, $i_L|_p$ is the inductor current set in the pth half-line period. If the inductor current sampling frequency is selected at 6.4 kHz and the line frequency is 50 Hz, there are 64 sampling points in one half-line period. Therefore, there are 64 sensed inductor current values, i.e., $i_L(1), i_L(2), \ldots, i_L(64)$, in the inductor current set $i_L|_p$. $D|_p$ is the duty cycle set in the pth half-line period.

In Fig. 1, the inductor current in the previous half-line periods is sensed as a discrete value and stored in the digital controller as the inductor current set $i_L|_p$, which is used to calculate the total harmonic distortion (THD). THD is used as the objective function for the optimization algorithm, because the power factor is increased when the THD is decreased. Based on the calculated objective function and the previous duty cycle set $D|_p$, the optimization algorithm, which is based on gradient descent, calculates the new duty cycle set $D|_{p+1}$ for the next half-line period to minimize the objective function (THD) and achieve a higher power factor. Once the power factor is higher than the specification requirement, the duty cycle set is "copied" from the previous one if the circuit operates under steady state.

In transient state, the calculated duty cycles are regulated by the output of the voltage loop. Fig. 2 shows the block diagram of the proposed output voltage control loop. First, the output voltage is processed via a low-pass filter to eliminate the double-line frequency ripple. Then, the feedback signal is compared with the reference voltage, and the error serves as the input of the voltage loop proportional–integral (PI) controller. The output of PI controller $K_{\rm pi}$ is the scaling factor for the duty cycle determined by the optimization algorithm. The product of multiplier is the duty cycle to control the switch S.

III. Optimization Algorithm for Minimizing THD

A. Objective Function

In a rectifier cascaded by a PFC circuit, the displacement power factor is unity. Therefore, if the distortion factor approaches 1, unity power factor is realized. The relation between the distortion factor and the THD is expressed by

$$k_{\rm distortion} = \frac{1}{\sqrt{1 + ({\rm THD})^2}}. \tag{1}$$

If the THD of the line current is minimum, the distortion factor is maximum. Then, the power factor becomes maximum. Zero THD means unity power factor. Therefore, the THD of the input current can be used as the objective function in the new digital PFC control algorithm.

The relation between the THD and the duty cycles in one half-line period is a very complicated nonlinear function. It can only be expressed as

$$({\rm THD})|_p = f(D|_p, v_{\rm in}, i_L(0), V_{\rm o}, R_{\rm o}) \tag{2}$$

where $D|_p = [d_1, d_2, \ldots, d_i, \ldots, d_n]^T$ is the duty cycle set vector in the pth half-line period. For example, if the switching frequency is 100 kHz and the line frequency is 50 Hz, there are 1000 components (duty cycles in one half-line period), i.e., $d_1, d_2, \ldots, d_{1000}$, in the duty cycle set vector D for one half-line period. $v_{\rm in}$ is the input line voltage, which is expressed as $v_{\rm in}(t) = V_{\rm pk} * \sin(2\pi f t)$, where $V_{\rm pk}$ is the peak value of the line voltage and f is the line frequency. $V_{\rm o}$ is the output voltage. $R_{\rm o}$ is the load resistor. In steady state, $V_{\rm o}$ and $V_{\rm pk}$ do not change. $i_L(0)$ is the initial inductor current in the pth half-line period, i.e., $i_L(0) = 0$. Assuming that $R_{\rm o}$ does not change in a period, which is long enough to complete the optimization routine, (2) can be simplified as

$$({\rm THD})|_p = f(D|_p) \tag{3}$$

where $({\rm THD})|_p$ is the THD with the duty cycle set $D|_p$ in the pth half-line period. It is noted from (3) that the THD is determined by the duty

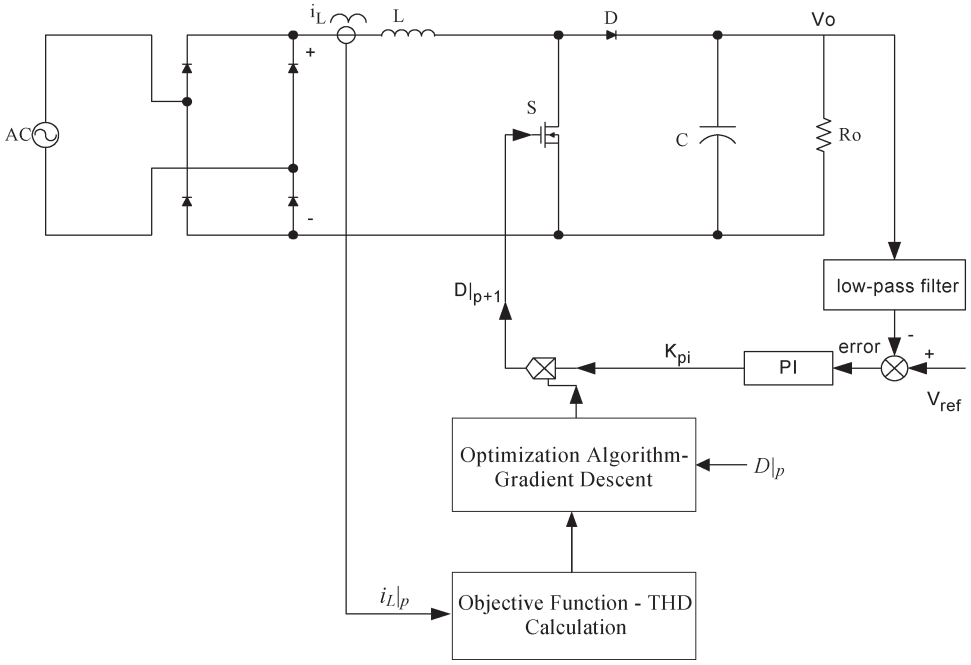

Fig. 2. Output voltage control scheme.

cycle set vector $D|_p$ in one half-line period, provided that the other variables in (2) are fixed.

It is necessary to calculate the gradient vector components of this function to implement the optimization algorithm. Unfortunately, it is too complicated to analytically perform the differentiation $\partial f/\partial d_i$ calculation. According to the secant approximation, the gradient vector component of (3) can be calculated using (4)

$$\frac{\partial f}{\partial d_i} \approx \frac{f(d_1, d_2, \ldots, d_i + \Delta d_i, \ldots, d_n) - f(d_1, d_2, \ldots, d_i, \ldots, d_n)}{\Delta d_i} \quad i = 1, 2, \ldots, n. \tag{4}$$

Equation (4) is an approximation equation for the gradient vector components calculation, provided that Δd_i is small enough. After all of the gradient vector components are calculated from (4), the objective function (THD) can be reduced by the gradient-descent optimization, and unity power factor is achieved.

B. Optimization Algorithm Based on Gradient Descent

The proposed optimization algorithm in the digitally controlled PFC circuit is based on gradient descent. The gradient of a differentiable function $f(D|_p)$, with n variables, is an n-dimensional vector expressed as

$$\nabla f(D|_p) = \left[\frac{\partial f}{\partial d_1}(D|_p), \frac{\partial f}{\partial d_2}(D|_p), \ldots, \frac{\partial f}{\partial d_n}(D|_p)\right]^T \tag{5}$$

where $f(D|_p)$ is the objective function. For a PFC implementation with a 100-kHz switching frequency and a 50-Hz line frequency, the vector determined by (5) is a 1000-dimensional vector. This vector defines the direction called gradient direction, which is the basis of this optimization algorithm. It is the direction of the steepest descent for minimization in this case.

Once the gradient direction is calculated, the gradient descent algorithm can be written in the following discrete form:

$$D|_{p+1} = D|_p + k\nabla f(D|_p) \tag{6}$$

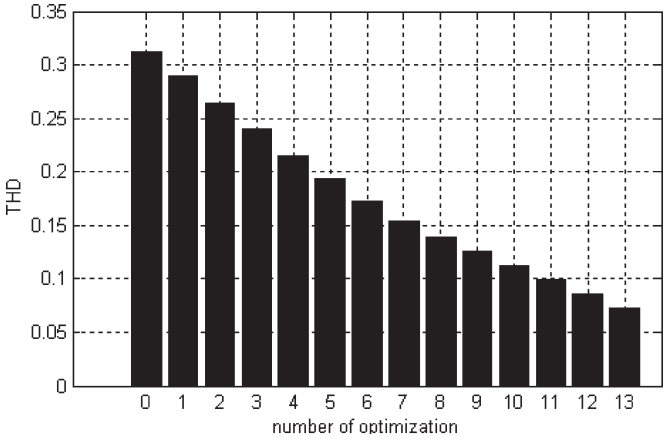

Fig. 3. THD of the input current after every optimization (full load = 1000 W).

where k is an arbitrary step size. For the digital PFC implementation, choose $k < 0$ so that the THD can be minimized in the optimization process. The gradient descent algorithm (6) takes the point with duty cycle set vector $D|_p$ to calculate the new point with duty cycle set vector $D|_{p+1}$, which determines a reduced THD compared with that of the previous half-line period. This algorithm converges if

$$\lim_{p\to\infty} \nabla f(D|_p) = 0. \tag{7}$$

IV. Simulation Results

The proposed digital PFC control method was simulated using Matlab based on the parameters of the Boost circuit, which are given as follows: $v_{\text{in}} = 220$ Vrms, $V_{\text{o}} = 400$ V, $L = 1$ mH, $C = 1100$ μF, $R_{\text{o}} = 160$ Ω, $R_{\text{L}} = 0.05$ Ω, $R_{\text{on}} = 0.27$ Ω, $f_s = 100$ kHz, and $f_{\text{line}} = 50$ Hz. R_{L} is the winding resistance of the inductor, and R_{on} is the on resistance of the MOSFET. The full load is 1000 W. The switching frequency is 100 kHz. Fig. 3 shows the THD of

the input current for full load after each optimization iteration. The THD before the optimization is 31.25%. After the first optimization iteration, the THD is reduced to 28.90%. The THD converges to 7.29% after the thirteenth optimization. The optimization improves the power factor from 0.9545 to 0.9974. The simulation result shows that the proposed optimization algorithm works well in a digital PFC control implementation.

V. Conclusion

One disadvantage of the existing digital PFC control methods is that the switching frequency is limited due to the processing time of the DSP. A new digital PFC control strategy was proposed in this paper to solve this problem. The proposed digital PFC control strategy uses an optimization algorithm to generate all of the required duty cycles for one half-line period in advance based on the input current and duty cycles in the previous half-line periods. One of the characteristics of the proposed digital PFC control method is that the switching frequency is not directly dependent on the speed of the DSP. Simulation results show that harmonic currents are reduced significantly and unity power factor can be achieved by using this method.

References

[1] M. Fu and Q. Chen, "A DSP based controller for power factor correction in a rectifier circuit," in *Proc. 16th Annu. IEEE APEC*, 2001, pp. 144–149.

[2] S. Buso and P. Mattavelli *et al.*, "Simple digital control improving dynamic performance of power factor pre-regulators," *IEEE Trans. Power Electron.*, vol. 13, no. 5, pp. 814–823, Sep. 1998.

[3] S. Bibian and H. Jin, "Digital control with improved performance for boost power factor correction circuits," in *Proc. 16th Annu. IEEE APEC*, 2001, pp. 137–143.

[4] W. Zhang, G. Feng, Y.-F. Liu, and B. Wu, "A digital power factor correction (PFC) control strategy optimized for DSP," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1474–1485, Nov. 2004.

[5] ——, "A new power factor correction (PFC) control method suitable for low cost DSP," in *Proc. IEEE Intelec*, 2002, pp. 407–414.

Performance Comparison of Capacitor-Run Induction Motors Supplied From AC Voltage Regulator and SPWM AC Chopper

K. Sundareswaran, N. Rajasekar, and V. T. Sreedevi

***Abstract*—This letter systematically investigates and compares the performance characteristics of a variable-speed capacitor-run induction motor driving a domestic fan load using an ac voltage regulator and a single pulsewidth-modulated (SPWM) ac chopper. This proposal is a significant break from the conventional conclusion since it is shown that the SPWM ac chopper is inferior to the phase angle control scheme for a capacitor-run motor load.**

***Index Terms*—AC choppers, capacitor motors, phase control.**

I. Introduction

In India, room temperature dips to 4 °C in winter and rises to 46 °C in summer, and the cost-effective way of achieving comfort during summer is through the use of domestic fans rather than air conditioners. Since the ambient temperature variation is wide as mentioned above, speed control of domestic fans is essential. The motor used for domestic fans is a capacitor start capacitor-run single-phase induction motor with squirrel cage rotor. The rotor resistance in these motors is higher and is, therefore, quite suitable for wide speed control range using stator voltage control. The commonly employed method of speed control in domestic fan motors is the use of a variable resistance in series with the motor. This scheme is very cheap, and due to this reason, it is popular even nowadays. However, this is an inefficient method of speed control due to the power loss in the series resistance. An alternative scheme is the use of a triac connected between the main supply and the fan motor, which is superior in power savings. The analysis of triac-based speed control schemes of capacitor-run motors is available in the literature [1], [2].

Voltage control with the triac-based scheme is simple, reliable, and cost effective. However, the ac voltage converter suffers from various drawbacks such as increased harmonic content and poor power factor, especially at lower output voltages. A pulsewidth-modulated (PWM) ac chopper has been suggested as an alternative to an ac voltage controller. In a PWM ac chopper, single or multiple pulses per half cycle can be employed. The ac chopper circuit employs forced commutated devices [3] or self-commutating devices [4]–[7]. System performance is further improved by using various harmonic elimination techniques in the ac chopper [5], [6]. It is shown in these works that the PWM ac chopper inherits several advantages over an ac voltage controller such as improved power factor, elimination of low-order harmonics, wide voltage control range, etc. However, in these works, an RL circuit is used as the load and comparison is performed. Performance comparison of a single-phase capacitor-run motor supplied from an ac voltage regulator and an ac chopper is not available in the literature. This letter shows that a variable-speed single-phase capacitor-run induction motor driving a residential fan exhibits improved performance characteristics when supplied from an ac voltage controller than from a single PWM (SPWM) ac chopper, quite contrary to earlier published works with RL load. Several performance characteristics are considered, and the computed and experimental results are presented to validate the claim.

II. Capacitor-Run Induction Motor Model and Results

The matrix differential equation describing the two-phase induction motor with all variables referred to the stator is taken from [1] and is given as that shown in (1) at the bottom of the next page. The variable a_s is defined as the ratio N_a/N_m, where N_a and N_m are the number of turns of the auxiliary and main windings, respectively. The independent variables are the main winding voltage V_m, auxiliary winding voltage V_a, and motor slip s. With phase angle control, the device is triggered at an angle α, the motor gets connected to supply, and the situation prevails as long the device carries current. When the device turns-off due to natural commutation, the motor gets disconnected from the supply. Thus, the motor terminal voltage depends on α, motor parameters, and slip. The ac chopper essentially consists of two switches, namely: 1) one in series with the motor and 2) one across the motor. When SPWM is used, a series switch is closed, keeping the parallel switch open; the motor terminal voltage is symmetrical about the $\pi/2$ axis and variable speed is achieved by changing the pulse width. In the next mode, the parallel switch is closed, short-circuiting motor terminals.

A typical domestic fan motor of 220 V, 55 W, and 1250 r/min is taken for analysis. Equation (1) is solved with phase angle

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