A New Duty Cycle Control Strategy for Power Factor Correction and FPGA Implementation

Wanfeng Zhang, *Member, IEEE*, Yan-Fei Liu, *Senior Member, IEEE*, and Bin Wu, *Senior Member, IEEE*

***Abstract*—The bottleneck of digital control for power factor correction (PFC) implementations is mainly due to three aspects: high calculation requirements, high cost, and limited switching frequency compared with analog implementations. A new duty cycle control strategy for boost PFC implementations is proposed in this paper. The duty cycle is determined based on the input voltage, reference output voltage, inductor current, and reference current. The duty cycle determination algorithm includes two terms, the current term and the voltage term, which can be calculated in parallel and requires only one multiplication and three additions (subtractions) operations in digital implementation. A 400-kHz switching frequency boost PFC based on field programmable gate array implementation and its test results show that the proposed new duty cycle control strategy has great potential in the next generation of high switching frequency PFC implementations, due to its lower calculation requirement, lower cost, and better performance than the conventional PFC control methods.**

***Index Terms*—Field programmable gate array (FPGA), power factor correction (PFC), switched mode power supplies (SMPS).**

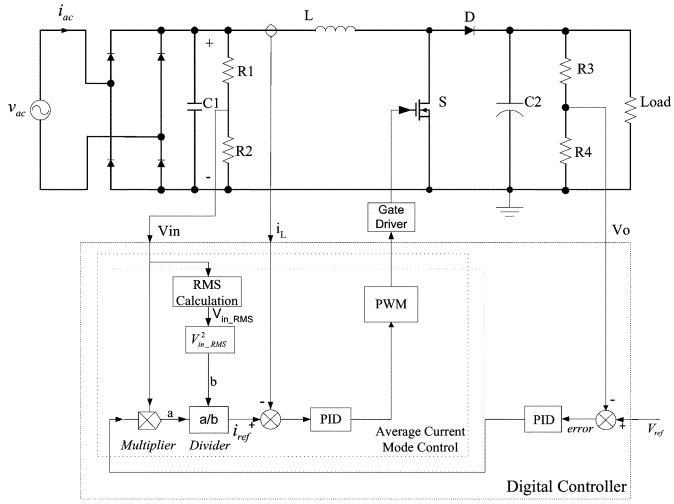

Fig. 1. Diagram of the digital control PFC implementation based on average current mode control.

I. Introduction

THE analog control has been the conventional method of power factor correction (PFC) in switched mode power supplies (SMPS). The emergence of powerful, low cost microprocessors, digital signal processors (DSP), and field programmable gate array (FPGA) have made it possible for the digital control to become a competitive option. However, all of the existing digital PFC control methods are based on conventional analog control laws. They basically implement the analog control laws in digital format. The algorithm of average current mode control in digital PFC is the same as that in analog systems. Basically, the average inductor current is forced to follow the reference current. The reference current is the programming signal, which is the multiplication of the rectified input voltage and a scaling factor (the output from the voltage controller). Hence, the input current (average inductor current) is proportional to the input voltage [1]–[4].

DSP control of a boost PFC based on average current mode control is illustrated in Fig. 1. In the outer voltage loop, the output voltage is sensed and compared with the voltage reference. The error becomes the input of the voltage proportional–integral–derivative (PID) regulator. The output of this PID controller is the scaling factor for the rectified voltage that is used as one of the inputs to the multiplier. The product of the scaling factor and the rectified voltage divided by the square of input voltage root mean square (RMS) value is the current reference, $i_{\rm ref}$. The inner current loop implements average current mode control to force the average inductor current to follow the reference current. In digital implementation, multiplication and division operations are implemented by the software. Because all the calculations, including multiplication and division, are executed in every switching period, the implementation requires a high speed digital controller.

References [5] and [6] presented a digital predictive dead-beat control that does not update the duty cycle in every switching cycle, because the DSP is not fast enough to complete all of the calculation. In the predictive dead-beat (PDB) control, the duty cycle, d_n, is calculated and updated once in every control period, which is several, or several tens of switching cycles. However, that control method works only under the ideal input situation, because input voltage is determined by a look-up table. In addition, the harmonic in the line current is increased in the Boost PFC implementation controlled by that method.

Digital current program control using another predictive algorithm was presented in [7]. In [7], the duty cycle, $d(n+1)$, was calculated based on the value of the present duty cycle, $d(n)$, and sensed inductor current, input voltage and output voltage.

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The problem is that, the duty cycle calculation requires the duty cycle value in the previous switching cycle. Therefore, if there is an error in the calculation value of $d(n)$, this error will affect the calculation value of $d(n+1)$.

Digital charge control is presented to implement PFC based on a FPGA combined with an analog to digital converter (ADC)[8], [9]. The switch turns "on," at the beginning of every switching period, and "off," when the mean value of input current reaches the reference value. The mean value of input current is the sum of the input current samples divided by the number of samples in one switching cycle. The switching frequency is 50 KHz. A very fast 12-b ADC (HI5805) is required for the integral operation to calculate the average value of the input current in order to guarantee the resolution of the duty cycles. Therefore, the cost of the control system is increased.

A digital off-line control technique, named stored-duty-ratio (SDR) control, was proposed in [10] and [11]. In that method, the duty cycles are calculated in advance based on the power balance equation of Boost topology and are stored in a memory. Because the duty cycles are calculated off-line, neither current sensing, nor input voltage sensing, nor CPU is required in that method. However, SDR control can only achieve the power factor over 0.99 in a very narrow input voltage range: 200–225 V.

A predictive algorithm aiming to reduce the computation requirement in digital control PFC implementations was proposed by the authors of this paper [12], [13]. In that method, all the duty cycles for a half-line period were calculated in advance. The proposed method in [12] can control the boost PFC operating at high switching frequency with low calculation requirement and with a low cost digital controller. However, the capability of the regulation to the step load change is not satisfactory when the load current variation is wide.

Although so many digital PFC control methods were presented in the reference papers, there are still several problems that needed to be solved for digital PFC implementations. In digital control PFC, the problems are mainly related to the following aspects: high calculation requirement in one switching cycle, high cost of the digital controller and limited switching frequency compared with analog control. It is necessary to explore new PFC control method suitable for digital implementations.

In this paper, a new duty cycle control algorithm for PFC is proposed in Section II. Calculation requirement for the proposed duty cycle control algorithm in digital implementation is presented in Section III. Digital implementation is introduced in Section IV. The FPGA implementation and test results are presented in Section V. Section VI is the comparison between the proposed duty cycle control method and the average current mode control. Section VII is the conclusion of this paper.

II. New Duty Cycle Control Algorithm for PFC

The boost topology used in PFC implementation is shown in Fig. 2. The proposed digital control PFC algorithm is derived based on the assumptions that the boost converter operates at continuous conduction mode (CCM) and that the switching frequency is much higher than the line frequency. Therefore, the input voltage, V_{in}, can be assumed as a constant within one switching cycle, T_s. Therefore, when the switch S is on or off, the boost converter is described by two equivalent circuits, as shown in Fig. 3.

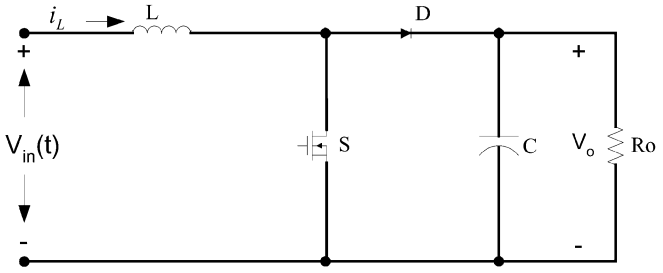

Fig. 2. Boost converter topology.

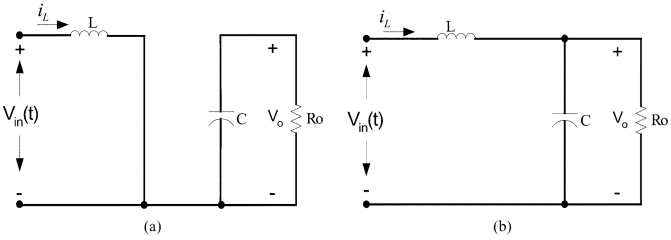

Fig. 3. Boost converter equivalent circuits.

When the switch is on, the inductor current, $i_L(t)$, can be expressed as

$$L\frac{di_L(t)}{dt} = V_{\text{in}}(t),\ \text{for}\ t(n) \le t < t(n) + d(n)\cdot T_s. \quad (1)$$

When the switch is off, the inductor current, $i_L(t)$, can be expressed as

$$L\frac{di_L(t)}{dt} = V_{\text{in}}(t) - V_o(t),\ \text{for}\ t(n) + d(n)\cdot T_s \le t < t(n+1) \quad (2)$$

where $V_{\text{in}}(t)$ is the input voltage, $V_o(t)$ is the output voltage, $t(n)$ and $t(n+1)$ are the beginning instant of nth and $(n+1)$th switching cycle, $d(n)$ is the duty cycle in nth switching cycle, and T_s is the switching period.

Because the switching frequency is much higher than the line frequency, the differential equations (1) and (2) can be expressed as

$$L\frac{i_L[t(n)+d(n)\cdot T_s] - i_L[t(n)]}{d(n)\cdot T_s} = V_{\text{in}}[t(n)] \quad (3)$$

$$L\frac{i_L[t(n+1)] - i_L[t(n)+d(n)\cdot T_s]}{[1-d(n)]\cdot T_s} = V_{\text{in}}[t(n)] - V_o[t(n)] \quad (4)$$

where $i_L[t(n)], i_L[t(n+1)]$ are the inductor current at the beginning of nth and $(n+1)$th switching cycles. The inductor current in one switching cycle is shown in Fig. 4.

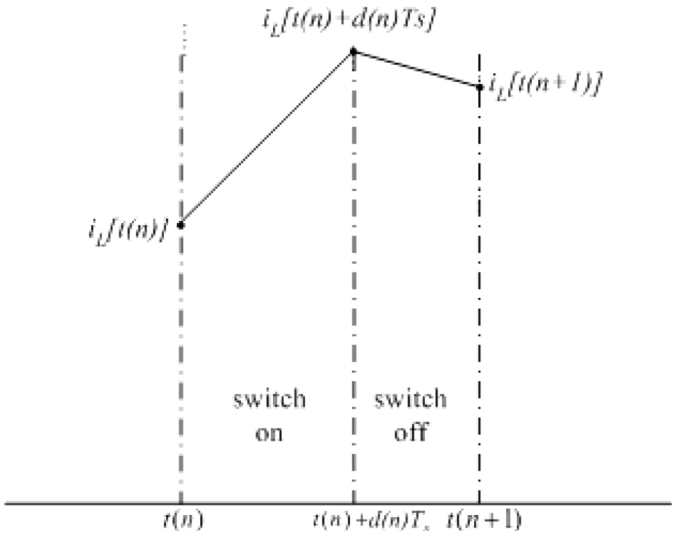

Fig. 4. Inductor current in one switching cycle.

The inductor current at the switching off instant, $t(n)+d(n)T_s$, can be derived from (3) as

$$i_L[t(n)+d(n)\cdot T_s] = i_L[t(n)] + \frac{1}{L}\cdot V_{\text{in}}[t(n)]\cdot d(n)\cdot T_s. \quad (5)$$

The inductor current at the beginning instant of $(n+1)$th switching cycle, $t(n+1)$, can be derived from (4) as

$$i_L[t(n+1)] = i_L[t(n)+d(n)\cdot T_s] + \frac{1}{L}\cdot\{V_{\text{in}}[t(n)]-V_o[t(n)]\}\cdot[1-d(n)]\cdot T_s. \quad (6)$$

Substituting (5) and (6), the inductor current at the beginning instant of $(n+1)$th switch cycle in terms of the inductor current at the beginning instant of nth switching cycle can be derived as

$$i_L[t(n+1)] = i_L[t(n)] + \frac{1}{L}\cdot V_{\text{in}}[t(n)]\cdot T_s - \frac{1}{L}\cdot V_o[t(n)]\cdot[1-d(n)]\cdot T_s. \quad (7)$$

The discrete form of (7) can be expressed as

$$i_L(n+1) = i_L(n) + \frac{V_{\text{in}}(n)\cdot T_s}{L} - \frac{V_o(n)\cdot[1-d(n)]\cdot T_s}{L}. \quad (8)$$

The above equation indicates that the inductor current at the beginning of the next switching cycle is determined by the inductor current at the beginning of present switching cycle, the input voltage, the output voltage and the duty cycle for the present switching cycle.

Equation (8) can be rewritten as

$$d(n) = \frac{L}{T_s}\frac{i_L(n+1)-i_L(n)}{V_o} + \frac{V_o - V_{\text{in}}(n)}{V_o}. \quad (9)$$

It is observed that the required duty cycle for the present switching cycle, $d(n)$, can be determined based on the boost circuit parameters, the output voltage, the input voltage and the required inductor current. Based on this observation, a new control method to achieve power factor correction can be derived.

It is noted that for a properly designed ac–dc converter with PFC, $i_L(n+1)$ is forced to follow the reference current, $i_{\text{ref}}(n+1)$, which is a rectified sinusoidal waveform, as shown in Fig. 5. V_o is controlled to follow the reference voltage, V_{ref}. Substituting $i_{\text{ref}}(n+1)$ and V_{ref} for $i_L(n+1)$ and V_o in (9), respectively, the duty cycle can be derived as

$$d(n) = \frac{L}{T_s}\frac{i_{\text{ref}}(n+1)-i_L(n)}{V_{\text{ref}}} + \frac{V_{\text{ref}} - V_{\text{in}}(n)}{V_{\text{ref}}} \quad (10)$$

where $i_L(n)$ is the sensed inductor current at the beginning of the switching cycle.

It is noted that the duty cycle generated by (10) will force the actual inductor current at the beginning of next switching cycle to follow the reference current. The difference between the reference current and the average inductor current will not impact the total harmonic distortion. Therefore, unity power factor can be achieved for the boost converter.

It is noted that there are two components in (10), expressed as

$$d(n) = d_1(n) + d_2(n). \quad (11)$$

The first component in (11), $d_1(n)$, expressed as

$$d_1(n) = \frac{[i_{\text{ref}}(n+1)-i_L(n)]\cdot\frac{L}{T_s}}{V_{\text{ref}}} \quad (12)$$

is defined as the current term. Under the steady state, the inductor current, $i_L(n+1)$, follows the reference current, $i_{\text{ref}}(n+1)$, at the end of that switching cycle. The reference current is determined as

$$i_{\text{ref}}(n+1) = k_{\text{PID}}\cdot|\sin[\omega_{\text{line}}\cdot t(n+1)]|. \quad (13)$$

k_{PID} is the peak value of the reference current, which is the output of voltage loop regulator. $|\sin(\omega_{\text{line}}\cdot t(n+1)|$ is the rectified line frequency sinusoidal waveform. It can be implemented by a look-up table in digital implementation or a resistor divider from the rectified input voltage.

Under transient state, if the load current is increased, the output voltage is reduced. The error between the reference voltage and the feedback voltage is increased. Then, the output of the voltage loop PID regulator, K_{pid}, is increased. Hence, the reference current is increased, which results in the current term, d_1, being increased. Eventually, the duty cycle is increased to force the output voltage to follow the reference voltage again. If the load current is decreased, the opposite process occurs. Therefore, $d_1(n)$ guarantees the output voltage to be regulated to follow the reference voltage under the transient state of load change.

The second component in (10), $d_2(n)$, expressed as

$$d_2(n) = 1 - \frac{V_{\text{in}}(n)}{V_{\text{ref}}} \quad (14)$$

is determined by the input and output voltage equilibrium of boost topology. Therefore, d_2 is defined as the voltage term. In

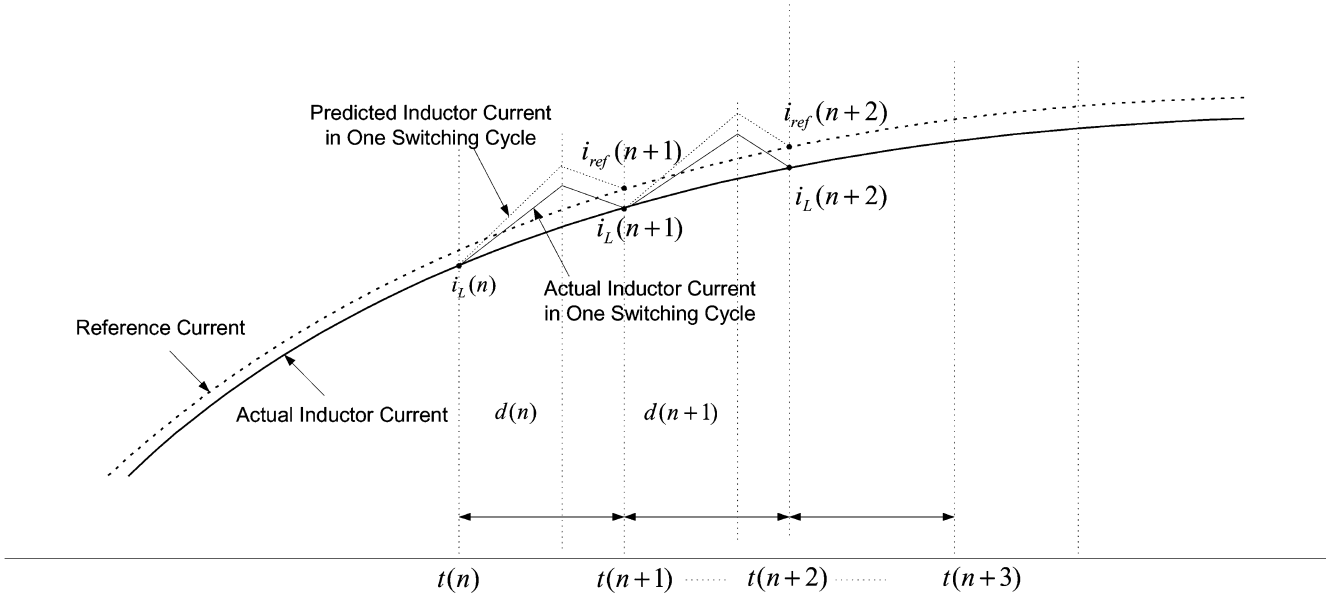

Fig. 5. Inductor current controlled by the calculated duty cycles.

(14), $V_{\rm in}(n)$ is the instantaneous input voltage value sensed by the input voltage feed-forward. It is observed from (14) that, if the input voltage is increased under the transient state, $d_2(n)$ is decreased instantaneously. Therefore, the duty cycle is decreased without delay to regulate the output voltage for input voltage change.

Substitute (13) into (10), the proposed PFC control algorithm can be expressed as

$$d(n) = \frac{k_{\rm PID} \cdot |\sin[\omega_{\rm line} \cdot t(n+1)]| - i_L(n)}{K_c} + \frac{V_{\rm ref} - V_{\rm in}(n)}{V_{\rm ref}} \quad (15)$$

where $K_c = T_s \cdot V_{\rm ref}/L$ is a constant. It can be used to simplify the proposed PFC control algorithm in the implementation.

The duty cycle in (10), $d(n)$, is generated based on: 1) the actual inductor current, $i_L(n)$, which is sensed at the beginning of the present switching cycle, $t(n)$ and 2) the desired inductor current, $i_{\rm ref}(n+1)$, which is the reference current value at the beginning of the next switching cycle, $t(n+1)$. The inductor current is controlled by $d(n)$ to follow the reference current. At $t(n+1)$, the inductor current $i_L(n+1)$ may not be exactly the same as, but very close to, the reference current $i_{\rm ref}(n+1)$. Because the reference current is sinusoidal, the actual inductor current will also be sinusoidal to achieve unity power factor.

The block diagram of the proposed duty cycle control for PFC implementation is shown in Fig. 6. In the figure, the voltage term block implements the calculation of (14) and the current term block implements the calculation of (12). It is observed that, the voltage term and the current term can be calculated in parallel. With this duty cycle control algorithm, (15), the inductor current of the Boost converter will follow the reference current and the output voltage of the Boost converter will follow the reference voltage.

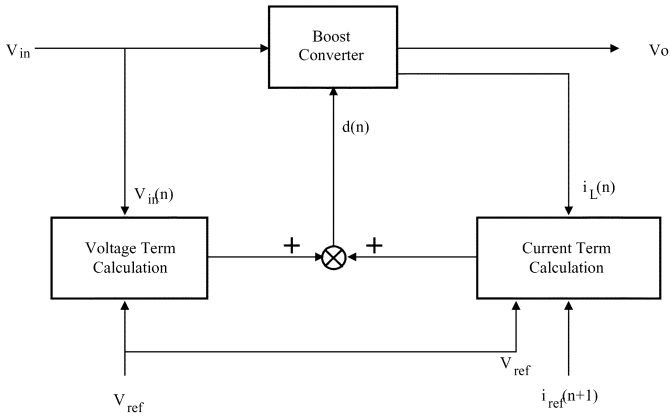

Fig. 6. Diagram of the proposed duty cycle control algorithm.

III. Calculation Requirement for the Proposed Duty Cycle Control

In the digital implementation of the proposed duty cycle calculation algorithm, (15) can be simplified as

$$d(n) = \frac{k_{\rm PID} \cdot |\sin[\omega_{\rm line} \cdot t(n+1)]| - i_L(n)}{K_c} + 1 - \frac{V_{\rm in}(n)}{V_{\rm ref}} \quad (16)$$

where K_c and $V_{\rm ref}$ are constants. It is observed from (16), that only one multiplication and three additions (or subtractions) are required in order to implement the proposed duty cycle control algorithm. Therefore, the digital implementation of the proposed PFC control algorithm is very simple. A low cost DSP, microprocessor, FPGA or an ASIC can be used to implement PFC operating at high switching frequency because of its low calculation requirement.

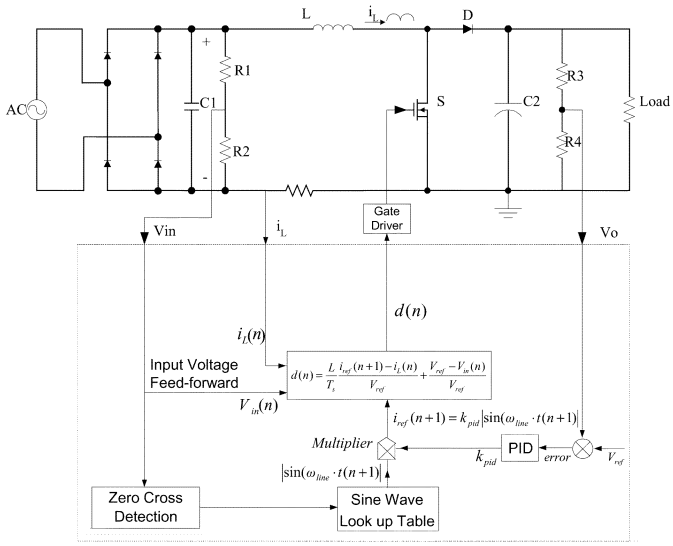

Fig. 7. Diagram of digital implementation of proposed duty cycle control.

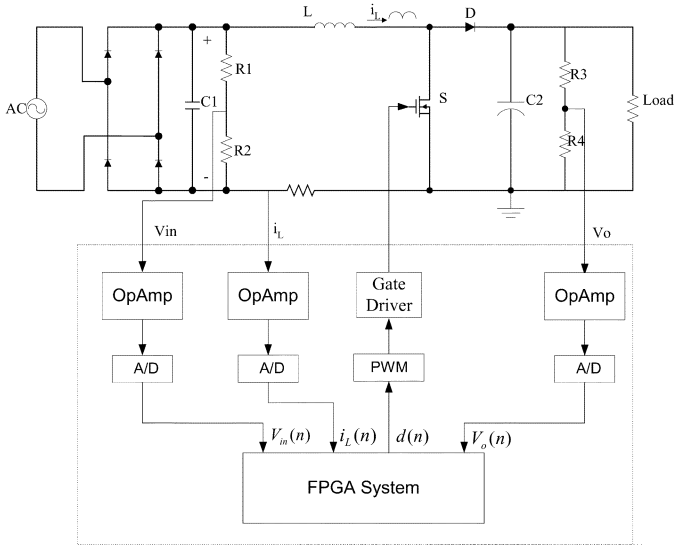

Fig. 8. Block diagram of FPGA implementation.

IV. Digital Implementation

The block diagram of the digital controlled boost PFC based on the duty cycle control algorithm is shown in Fig. 7. The zero cross detector and sine wave look-up table are used to generate a rectified sinusoidal waveform with unity peak value. The output of the sinusoidal waveform look-up table is multiplied by the output of the voltage loop regulator, $K_{\rm pid}$. The output of the multiplier is a rectified sinusoidal waveform, with peak value determined by the output of voltage loop regulator, $K_{\rm pid}$, and the waveform shape determined by the look-up table. It serves as the reference value for the inductor current. The duty cycle is calculated by the proposed duty cycle control algorithm based on the input voltage, reference voltage, inductor current and reference current. The output of the digital control system is the gate signal for the switch, S.

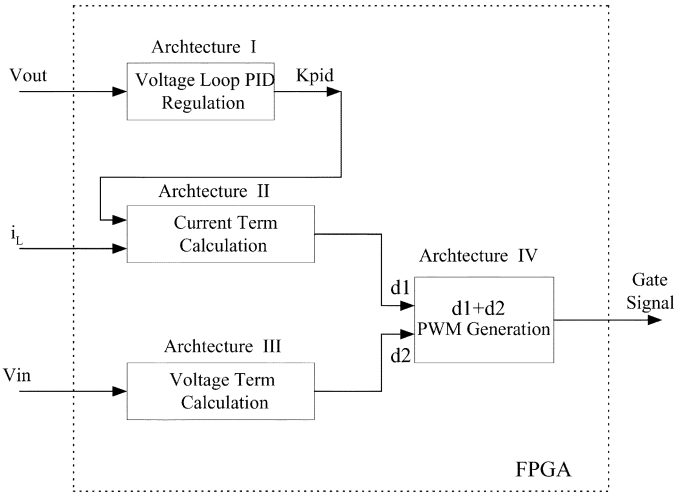

Fig. 9. VHDL implementation diagram.

V. Experimental Results of FPGA Implementation

The proposed control method was verified by both DSP and FPGA implementation. The experimental results of DSP implementation were presented in [14]. In order to demonstrate that the proposed control strategy can be implemented by an ASIC with much lower gate counts and simpler configuration, an FPGA implementation of the proposed control method is also presented, as well as experimental results, in this paper. The experimental results illustrate that low THD is achieved under both steady state and transient conditions. The FPGA's clock frequency is 50 MHz and the switching frequency is 400 KHz.

The block diagram of FPGA implementation for the proposed duty cycle control PFC is shown in Fig. 8. The input voltage, inductor current and output voltage are sensed and sent to the A/D converters via operating amplifiers (OpAmp). A 10-b A/D converter, AD 9215, is used in the designed system. The typical input signal range of AD9215 is 2 V (peak to peak value). Hence, the input range for unipolar signal is 1 V. The FPGA is Xlinx Spartan IIE XC2S200E. The clock frequency is 50 MHz. The PWM signal with the calculated duty cycle is sent to the switch through a gate drive circuit.

The VHDL implementation of the proposed duty cycle control in FPGA is shown in Fig. 9. The architecture II for current term calculation and architecture III for voltage term calculation are processed in parallel concurrently. In the prototype, the 50-MHz FPGA chip was used to implement the proposed control method to achieve 400-kHz switching frequency in ac–dc converter with PFC. Only about 15 000 gates are used in the FPGA. This means that a mixed signal ASIC solution based on the proposed duty cycle control can achieve higher switching frequency with lower cost, than the other digital solutions.

The operating parameters for the prototype of FPGA implementation are chosen as following: rated input voltage $V_{\rm in} = 55$ V(RMS), output voltage $V_{\rm out} = 100$ V, rated output power $P_{\rm load} = 300$ W, switching frequency $f_{\rm sw} = 400$ kHz and line frequency $f_{\rm line} = 60$ Hz. The Boost inductor value is 100 μH and the output capacitor is 1100 μF. The experimental results are presented in the following subsections.

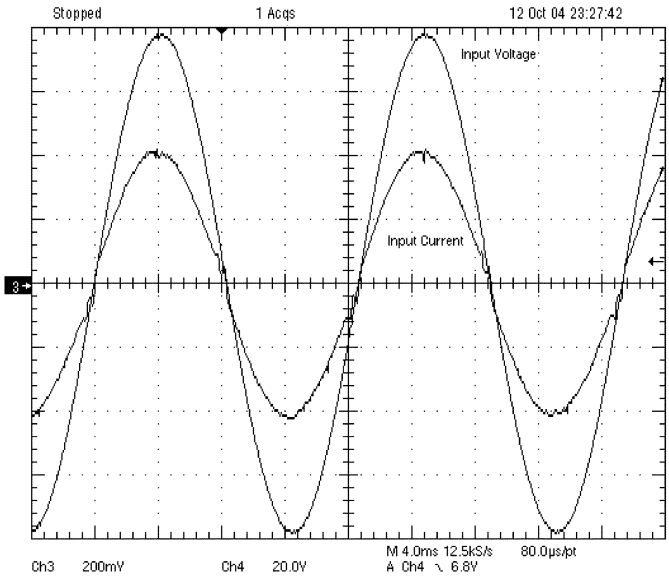

Fig. 10. Input voltage and current waveforms; $I_o = 3$ A, $L = 100$ μH, THD=4.7%, PF=0.999, Voltage: 20 V/div, Current: 4 A/div.

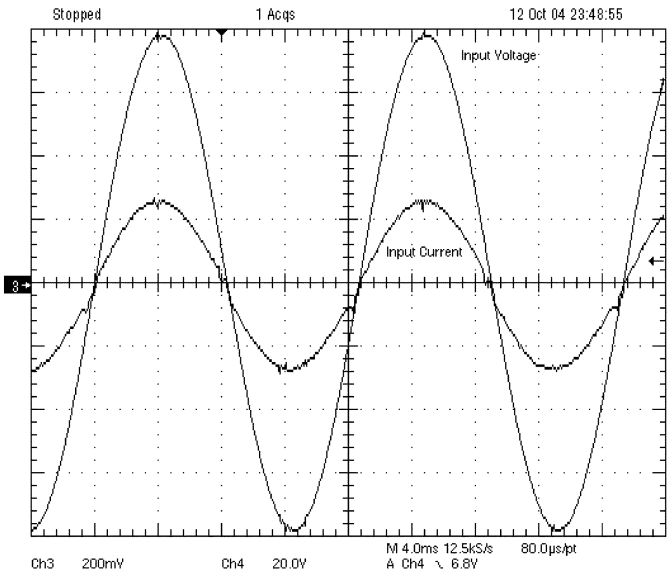

Fig. 11. Input voltage and current waveforms; $I_o = 2$ A, $L = 100$ μH, THD=7.3%, PF=0.997, Voltage: 20 V/div, Current: 4 A/div.

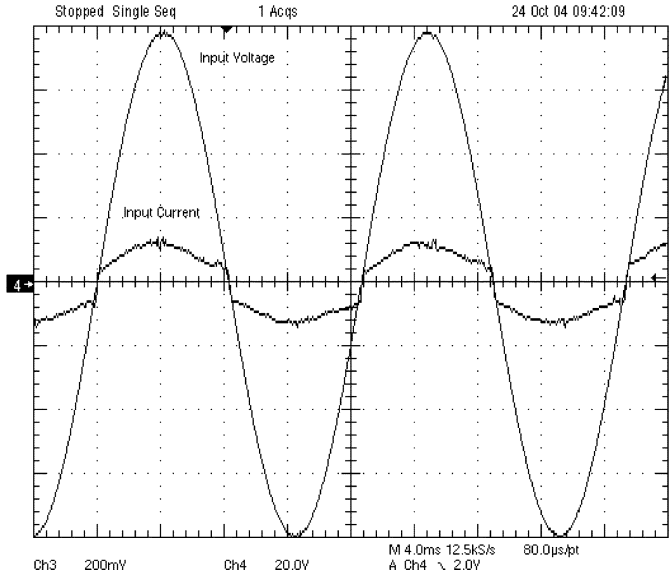

Fig. 12. Input voltage and current waveforms; $I_o = 1$ A, $L = 100$ μH, THD=14.5%, PF=0.990, Voltage: 20 V/div, Current: 4 A/div.

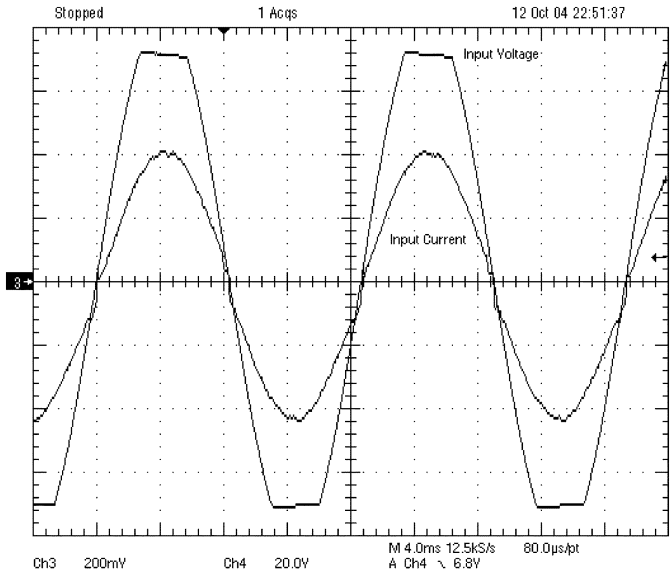

Fig. 13. Input current waveform for distorted input voltage; input current THD=4.9%, Voltage: 20 V/div, Current: 4 A/div.

A. Test Results Under Steady State Condition

The input current and voltage waveforms for the full load ($I_o = 3$ A) under the steady state are shown in Fig. 10. The power factor under this condition is 0.999 and THD is 4.7%. The input current and voltage waveforms for the load current, $I_o = 2$ A, is shown in Fig. 11. The power factor under this condition is 0.997 and THD is 7.3%. The input current and voltage waveforms for the load current, $I_o = 1$ A, is shown in Fig. 12. The power factor under this condition is 0.990 and THD is 14.5%.

Test results show that the proposed PFC control method can achieve near unity power factor under the steady state with a 100-μH inductor. The input current waveform for the load current, $I_o = 1$ A, has some distortion in the zero crossing region. This is because there is no enough noise margin in the sensed inductor current under low load condition in this prototype. This can be improved by a proper design of the current sense circuit before the A/D converter.

B. Test Results Under Distorted Input Voltage

In the digital implementation of the proposed PFC control strategy based on a look-up table, the input current will remain sinusoidal even when the input voltage is distorted. The input current waveforms under the distorted input voltage condition are shown in Fig. 13. In the test, the input voltage is 55 V and clipped at 85% peak value. Under this condition, the measured THD of input current is 4.9% and the power factor is 0.999. Test results show that sinusoidal input current waveform can be achieved under non-sinusoidal input voltage condition.

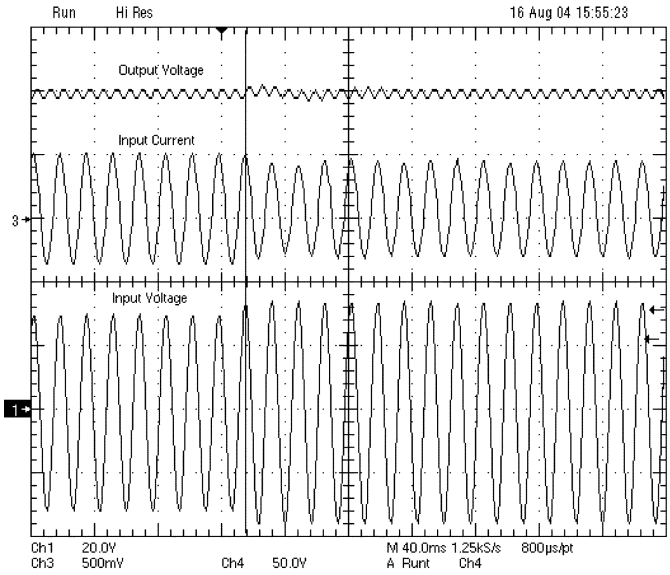

Fig. 14. Input current & output voltage for step input voltage change; V_{in} changed from 55 to 65 V, output voltage overshoot: 1 V, Input voltage: 50 V/div, Output voltage: 20 V/div, Current: 10 A/div.

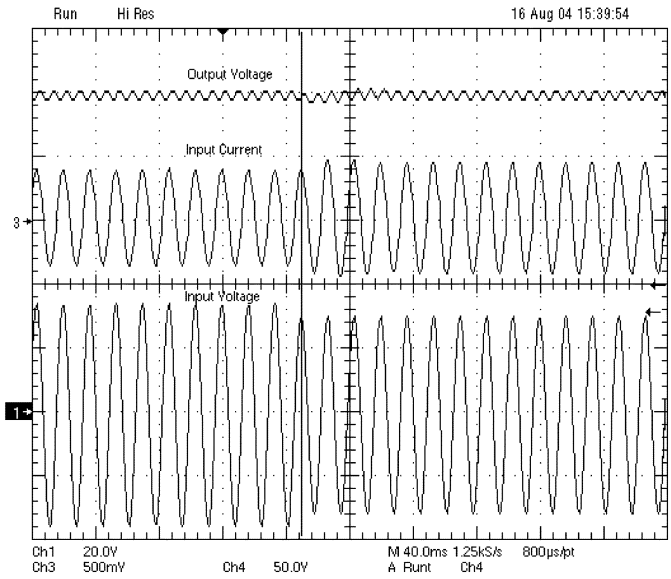

Fig. 15. Input current & output voltage for step input voltage change; V_{in} changed from 65 to 55 V, output voltage drop: 1 V, Input voltage: 50 V/div, Output voltage: 20 V/div, Current: 10 A/div.

C. Test Results Under Transient State

The dynamic performance under the transient state for step input voltage change is shown in Figs. 14 and 15, respectively. When the input voltage is changed from 55 to 65 V as shown in Fig. 14, the output voltage overshoot in the transient state is about 1 V. When the input voltage is reduced from 65 to 55 V as shown in Fig. 15, the output voltage drop in the transient state is about 1 V. It is noted that the input current still maintains sinusoidal waveform during the transient period.

The transient responses when the load current is changed from 2 to 3 A and from 3 to 2 A are shown in Figs. 16 and 17, respectively. Again, the input current can maintain sinusoidal waveform during the load transient condition.

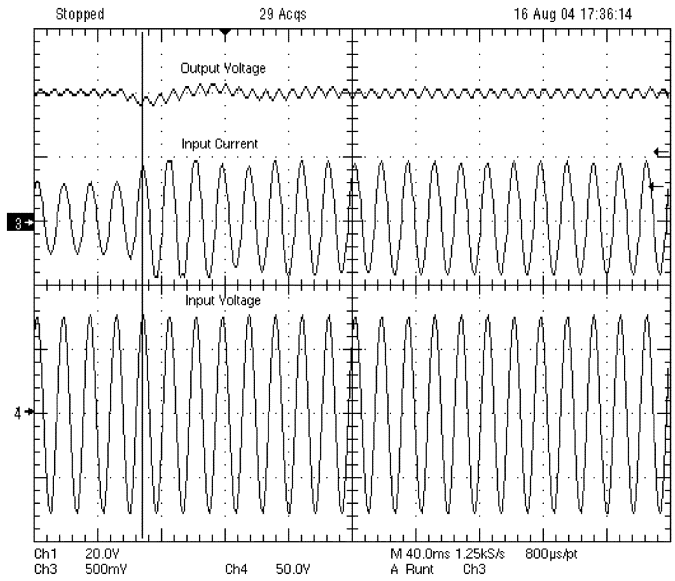

Fig. 16. Input current & output voltage waveforms in load transient state; I_o changed from 2 to 3 A, output voltage drop 2.3 V, Input voltage: 50 V/div, Output voltage: 20 V/div, Current: 10 A/div.

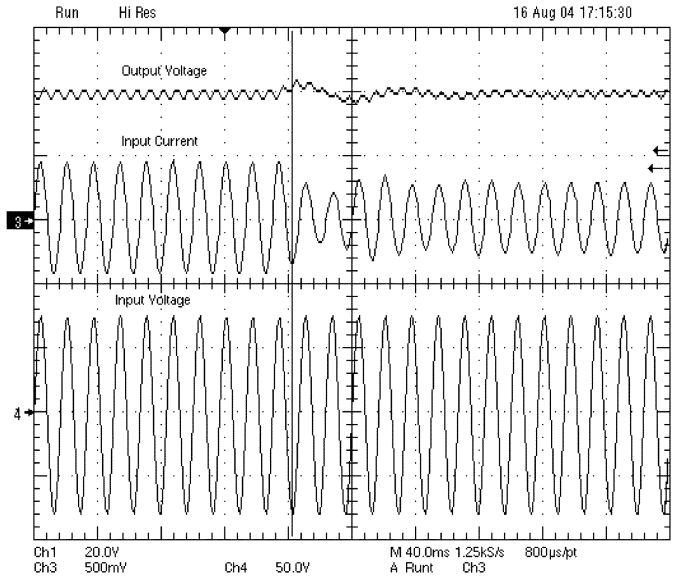

Fig. 17. Input current output voltage waveforms in load transient state; I_o changed from 3 to 2 A, output voltage overshoot 2.5 V, Input voltage: 50 V/div, Output voltage: 20 V/div, Current: 10 A/div.

VI. Comparison Between Proposed Duty Cycle Control and Conventional Average Current Mode Control

A typical digital implementation of conventional average current mode control for PFC is shown in Fig. 1. In Fig. 1, the output voltage regulation is achieved by the outer loop. The average current mode control is implemented by the inner current loop. The current reference is derived from the output of voltage loop, the rectified input voltage signal and the inverse of the input voltage RMS square. Under the steady state, the output voltage follows the reference voltage and the input current follows the reference current, which is sinusoidal waveform if there is no distortion in the input voltage.

Under load current transient state, if the load is increased, the output voltage is dropped. The error between the reference voltage and the feedback voltage is increased. Then, the output of voltage loop PID regulator is increased. Hence, the reference current is increased. After current loop regulation, the duty cycle is increased to force the output voltage to follow the reference voltage again. If load is decreased, the opposite process occurs. Under input voltage transient state, if the input voltage is increased, the output voltage is increased instantaneously. The RMS value and RMS square of the input voltage is increased after a time delay due to the filter in the implementation. Then the reference current is decreased. After current loop regulation, the duty cycle is decreased to force the output voltage decrease and follow the reference voltage again. If the input voltage decreased, the opposite process occurs.

The digital implementation of duty cycle control for PFC is shown in Fig. 7. In Fig. 7, the output voltage is regulated by outer loop, which is the same as average current mode control. The duty cycle control is implemented inside of the voltage loop. Different from the average current mode control, the proposed duty cycle control does not need division operation and the second PID regulator for current regulation. Actually, only one multiplication is needed to produce the current reference. Under the steady state, the output voltage follows the reference voltage and the input current follows the reference current, which is a sinusoidal waveform.

Under load transient state, if the load is increased, the output voltage is dropped. The error between the reference voltage and the feedback voltage is increased. Then, the output of voltage loop PID regulator, $K_{\rm pid}$, is increased. Hence, the reference current is increased, which results in that the duty cycle is increased. Therefore, the output voltage is forced to follow the reference voltage again. If load is decreased, the opposite process occurs.

Under the input transient state, if the input voltage is increased, duty cycle is decreased instantaneously, according to control strategy (16), with no time delay to regulate the output voltage to follow the reference voltage. This is different from the input transient state based on average current mode control, in which there is time delay from the input voltage change to the duty cycle change. Therefore, the proposed duty cycle control can achieve better dynamic performance for input change transient than average current mode control. If the input voltage decreased, the opposite process occurs. This can be observed from the experimental measurement shown in Figs. 14 and 15.

The performance comparison between proposed duty cycle control method and conventional average current mode control is summarized in Table I. First, both proposed duty cycle control method and average current mode control can achieve near unity power factor under the steady state with sinusoidal input voltage. Second, the advantage of proposed duty cycle control method with look-up table is that it can achieve sinusoidal input current waveform even under distorted input voltage condition. Third, the proposed duty cycle control method and the average current mode control can achieve the same dynamic performance of output voltage to load current change. However, the proposed duty cycle control method can achieve faster dynamic performance of output voltage to input change than the average current mode control.

TABLE I
PERFORMANCE COMPARISON BETWEEN THE PROPOSED DUTY CYCLE CONTROL AND CURRENT MODE CONTROL

	Proposed Duty Cycle Control	Average Current Mode Control
Steady State with Sinusoidal Input	Sinusoidal Input Current	Sinusoidal Input Current
Steady State with Distorted Input	Sinusoidal Input Current	Distorted Input Current
Dynamic Response for Load Change	Same	Same
Dynamic Response for Input Change	Faster than Average Current Mode Control	Slower than proposed Duty Cycle Control

In FPGA implementations, about 43 100 gates are required to implement the average current mode control and about 15 500 gates are required to implement the proposed duty cycle control. Therefore, the gates required for duty cycle control is much less than the gates required for average current mode control. It is expected that the cost of the ASIC implementation based on the proposed duty cycle control is lower than that based on average current mode control.

VII. CONCLUSION

A new duty cycle control strategy for the boost PFC implementation is proposed in this paper. The duty cycle is determined by a control algorithm based on the input voltage, reference output voltage, inductor current, and reference current. The proposed duty cycle control method requires only one multiplication and three additions (subtractions) operations for digital implementation, so that the proposed PFC control method can be implemented by a low cost DSP, FPGA, or an ASIC to achieve a high switching frequency. The proposed duty cycle control is simpler than the average current mode control for digital PFC implementation.

A prototype of FPGA implementations was built to verify the proposed duty cycle control. The switching frequency of FPGA control Boost PFC is 400 kHz. Test results show that the proposed method can achieve unity power factor under both the steady and transient states. The digital PFC implementation based on duty cycle control offers the following advantages: 1) high switching frequency, 2) low calculation requirement, and 3) low cost digital implementation. Therefore, the proposed duty cycle control strategy has great potential in next generation of high switching frequency PFC implementations.

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