# Optimal Design of Current Source Gate Driver for a Buck Voltage Regulator Based on a New Analytical Loss Model

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***Abstract* - The superior advantages of a new current-source resonant driver are verified thoroughly by the analytical analysis, simulation and experimental results. A new accurate analytical loss model of the power MOSFET driven by a current-source resonant gate driver is developed. Closed-formed analytical equations are derived to investigate the switching characteristics due to the parasitic inductance. The modeling and simulation results prove that compared to a voltage driver, a current-source resonant driver significantly reduces the propagation impact of the common source inductance during the switching transition at very high switching frequency, which leads to a significant reduction of the switching transition time and the switching loss. Based on the proposed loss model, a general method to optimize the new resonant driver is proposed and employed in the development of a 12V synchronous buck voltage regulator (VR) prototype at 1MHz switching frequency. The level-shift circuit and digital implementation of complex programmable logic device (CPLD) are also presented. The analytical modeling matches the simulation results and experimental results very well. Through the optimal design, a significant efficiency improvement is achieved. More importantly, compared to other state of the art VR approaches, the current-source driver is very promising from the standpoints of both performance and cost-effectiveness.**

## I. INTRODUCTION

In order to meet the strict transient requirements of future microprocessors and achieve very high power density, the switching frequency of a Voltage Regulator (VR) will move into the megahertz (MHz) range in the next few years.

However, an increase in switching frequency could lead to poor efficiency due to excessive switching loss and gate drive loss, which are proportional to switching frequency, and consequently degrade VRs' overall performance. More importantly, it has been noticed that the parasitic inductance, especially, the common source inductance has a serious propagation effect during the switching transition and thus results in high switching loss in a high frequency synchronous buck VR [1]. In order to understand the parasitic effect thoroughly, accurate analytical models considering the common source inductance and the loop inductance are developed in [2]-[3]. It should be noted that the common source inductance can be reduced but could not be eliminated completely. So methods to reduce the significant switching loss, due to the negative effect of the common source inductance, of a high frequency buck VR have become a very critical issue.

In the last fifteen years, resonant gate drive circuits have originally been proposed with the objective of recovering gate energy lost in a conventional gate driver [4]-[7]. An assessment of resonant drive techniques for use in low power dc/dc converters is presented in [8] and the mathematical model is built to estimate the power loss of the drive circuit in [9]. However, these investigations are generally emphasizing gate energy savings by the resonant driver and concentrating on the drive topologies, but ignore the potential switching loss savings that are much more dominant in a high frequency buck VR.

Recently, several new current-source resonant gate drivers with continuous current [10]-[11] and with discontinuous current [12] are proposed, which are able to reduce the switching loss significantly by using a constant current to charge and discharge the input capacitor of a power MOSFET during the switching transition to achieve fast switching speed. However, there are still several important issues need to be explored. Firstly, the effect of the parasitic inductance on the resonant driver has not been investigated analytically and the switching behaviour of a power MOSFET with a current-source resonant driver has not been presented in the known literature. Secondly, the potential switching loss saving by a resonant driver considering the parasitic inductance at high frequency over a conventional voltage driver is not addressed clearly. Thirdly, a general method for the purpose of optimal design of a resonant driver should be proposed to achieve maximum improvement of the efficiency for a high frequency synchronous buck VR.

The objective of this paper is to solve the above problems and demonstrate the superior advantages of the new resonant driver for high frequency VR application. At first, the paper develops a new analytical loss model of the power MOSFET driven by a current-source resonant gate driver. Closed-formed analytical equations are derived to investigate switching characteristics due to the parasitic inductance. The comparison between a voltage driver and a resonant driver is presented concentrating on the common source inductance in detail. The modeling and simulation results prove that a current-source resonant driver can significantly reduce the propagation impact of the common source inductance on the switching transition, which leads to a significant reduction of the switching transition time and the switching loss. Based on the proposed

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loss model, a generalized method to optimize the new current-source resonant gate driver is proposed and employed in the development of a 12V synchronous buck VR prototype at 1MHz switching frequency. The level-shift circuit for the resonant driver and the implementation of the complex programmable logic device (CPLD) are also presented. The analytical modeling matches the simulation results and the experimental results very well. Through the optimal design, a significant improvement of the efficiency is achieved. At 1.5V output, a VR with the current-source gate driver achieves 86.6% efficiency at 20A (up 3.9% from the conventional gate driver). At 30A load current, the efficiency is 83.6% (up 6.7% from the conventional driver).

## II. Proposed MOSFET Loss Model with Current Source Driver

The MOSFET switching loss models can be classified into (1) a physical-based model using physical parameters of the device, (2) a behaviour model provided by device vendor supplies, and (3) an analytical model (also called a mathematical model). The physical-based model and the behaviour model are convenient using simulation software, but it is difficult to use simulation for the purpose of design and optimization directly. It should be stressed that the piecewise loss model by linearizing the switching waveforms is no longer valid due to the parasitic inductance at high frequency. Therefore, we need a new analytical loss model to predict the optimal design solution for a current-source driver.

### A. Circuit and Basic Assumption

Figure 1 shows a basic converter circuit including a MOSFET in series with a diode $D_1$, with dc input voltage $V_D$ and an inductive load. The simplified equivalent circuit for the switching transition is shown in Figure 2, where MOFET $M_1$ is represented with a typical capacitance model, the clamped inductive load is replaced by a constant current-source and the current-source gate driver is simplified as a current source ($I_G$) since the charge and discharge current is kept constant during the switching transition. $L_D$ is the switching loop inductance including the packaging inductance and any unclamped portion of the load inductance. $L_S$ is the common source inductance, which is shared by the main current path and the gate diver loop. The critical MOSFET parameters are as follows: 1) the gate-to-source capacitance $C_{GS}$, the gate-to-drain capacitance $C_{GD}$, the drain-to-source capacitance $C_{DS}$; 2) the gate equivalent series resistance (ESR) $R_G$ (external and internal); 3) the threshold voltage $V_{th}$; 4) transconductance $g_{fs}$.

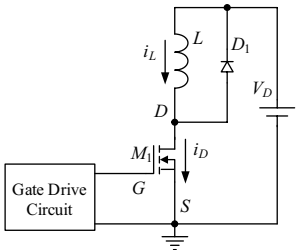



Figure 1 Circuit with a clamped inductive load

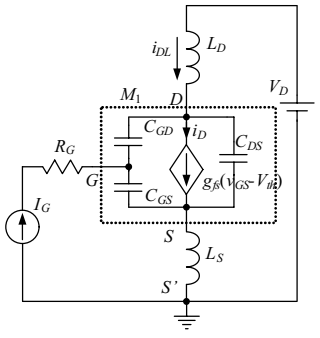



Figure 2 Equivalent circuit of MOSFET switching transition

For purpose of transient analysis, we make the following simplifying assumptions:

(1) $i_D=g_{fs}(v_{GS}-V_{th})$ and MOSFET is ACTIVE, provided $v_{GS}>V_{th}$ and $v_{DS}>i_D R_{DS(on)}$;

(2) For $v_{GS}<V_{th}$, $i_D=0$, and MOSET is OFF;

(3) When $g_{fs}(v_{GS}-V_{th})> v_{DS}/R_{DS(on)}$, the MOSFET is fully ON.

### B. Analytical Modeling of Main Switching Transition

During the main switching transition period, the MOSFET enters its active state and the linear transfer characteristics is assumed as given in (1), where $i_D(t)$ is the instantaneous switching current of the MOSFET and $v_{GS}(t)$ is the instantaneous gate-to-source voltage of the MOSFET:

$$i_D(t) = g_{fs}(v_{GS}(t) - V_{th}) \tag{1}$$

According the equivalent circuit in Figure 2, the circuit equations take the form

$$I_G = C_{GD}\frac{dv_{GD}}{dt} + C_{GS}\frac{dv_{GS}}{dt} \tag{2}$$

and

$$v_{GD} = v_{GS} - v_{DS} \tag{3}$$

So

$$I_G = (C_{GS} + C_{GD})\frac{dv_{GS}}{dt} - C_{GD}\frac{dv_{DS}}{dt} \tag{4}$$

From (4), $dv_{DS}/dt$ is solved as

$$\frac{dv_{DS}}{dt} = \frac{C_{GS} + C_{GD}}{C_{GD}} \cdot \frac{dv_{GS}}{dt} - \frac{I_G}{C_{GD}} \tag{5}$$

So $d^2v_{DS}/dt^2$ and $d^3v_{DS}/dt^3$ are respectively

$$\frac{d^2v_{DS}}{dt^2} = \frac{C_{GS} + C_{GD}}{C_{GD}} \cdot \frac{d^2v_{GS}}{dt^2} \tag{6}$$

$$\frac{d^3v_{DS}}{dt^3} = \frac{C_{GS} + C_{GD}}{C_{GD}} \cdot \frac{d^3v_{GS}}{dt^3} \tag{7}$$

During the switching interval, the change of the switching loop current $i_{DL}$ induces a voltage across the parasitic inductance. The drain-to-source voltage $v_{DS}$ is given as

$$v_{DS} = V_D - (L_D + L_s)\frac{di_{DL}}{dt} \tag{8}$$

And

$$i_{DL} = C_{GS}\frac{dv_{GS}}{dt} + C_{DS}\frac{dv_{DS}}{dt} + g_{fs}(v_{GS} - V_{th}) - I_G \tag{9}$$

Substituting (9) to (8) yields (10) and then substituting (6) to (10) yields (11)

$$v_{DS} = V_D - (L_D + L_s)(C_{GS}\frac{d^2v_{GS}}{dt^2} + C_{DS}\frac{d^2v_{DS}}{dt^2} + g_{fs}\frac{dv_{GS}}{dt}) \tag{10}$$

$$v_{DS} = V_D - (L_D + L_s)(g_{fs}\frac{dv_{GS}}{dt} + \frac{C_{GS}C_{GD} + C_{DS}C_{GD} + C_{DS}C_{GS}}{C_{GD}} \cdot \frac{d^2v_{GS}}{dt^2}) \tag{11}$$

Differentiating (11) yields

$$\frac{dv_{DS}}{dt} = -(L_D + L_s)(g_{fs}\frac{d^2v_{GS}}{dt^2} + \frac{C_{GS}C_{GD} + C_{DS}C_{GD} + C_{DS}C_{GS}}{C_{GD}} \cdot \frac{d^3v_{GS}}{dt^3}) \quad (12)$$

Substituting (5) into (12), Equation (13) is derived

$$A\frac{d^3v_{GS}(t)}{dt^3} + B\frac{d^2v_{GS}(t)}{dt^2} + C\frac{dv_{GS}(t)}{dt} = I_G, \quad (13)$$

where parameters $A$, $B$ and $C$ are represented in terms of the device parameters ($C_{GS}$, $C_{GD}$, $C_{DS}$, $g_{fs}$ and $R_G$) and the equivalent circuit parameters ($L_D$ and $L_S$) as $A=(L_D+L_s)(C_{GS}C_{GD}+C_{DS}C_{GD}+C_{DS}C_{GS})$, $B=g_{fs}(L_D+L_s)C_{GD}$ and $C=C_{GS}+C_{GD}$.

For turn-on transition, the initial condition for Equation (13) is $v_{GS}(0)=V_{th}$. Then Equation (13) solves to give either sinusoidal or exponential solutions, depending on the relative magnitudes of $B^2$ and $AC$.

When $B^2-4AC<0$, sinusoidal solution occurs and $v_{GS}(t)$ takes the form:

$$v_{GS}(t) = (\frac{B^2}{2C^2\cdot\sqrt{4AC-B^2}} - \frac{\sqrt{4AC-B^2}}{2C^2})\cdot I_G\cdot\exp(-\frac{t}{T_1})\cdot Sin(\omega_1 t) + \frac{B}{C^2}\cdot I_G\cdot\exp(-\frac{t}{T_2})\cdot Cos(\omega_1 t) + \frac{I_G\cdot t}{C} - \frac{B}{C^2}\cdot I_G + V_{th} \quad (14)$$

where $T_1=\frac{2A}{B}$, $\omega_1=\frac{\sqrt{4AC-B^2}}{2A}$.

When $B^2-4AC>0$, exponential solution occurs. Then $v_{GS}(t)$ takes the form

$$v_{GS}(t) = -\frac{(\sqrt{B^2-4AC}+B)\cdot I_G\cdot A\cdot\exp(-\frac{t}{T_2})}{(\sqrt{B^2-4AC}-B)\cdot C\cdot\sqrt{B^2-4AC}} + \frac{(\sqrt{B^2-4AC}-B)\cdot I_G\cdot A\cdot\exp(-\frac{t}{T_3})}{(\sqrt{B^2-4AC}+B)\cdot C\cdot\sqrt{B^2-4AC}} + \frac{I_G\cdot t}{C} - \frac{B\cdot I_G}{C^2} + V_{th}, \quad (15)$$

where $T_2=\frac{2A}{B-\sqrt{B^2-4AC}}$, $T_3=\frac{2A}{B+\sqrt{B^2-4AC}}$.

Then, by substituting $v_{GS}(t)$ to (1) and (11), $i_D(t)$ and $v_{DS}(t)$ of the MOSFET can be calculated respectively. The turn-off transition is similar to the turn-on transition except for the initial condition becomes $v_{GS}(0)=V_{th}+\frac{I_L}{g_{fs}}$.

## III. Analytical Modeling and Simulation Results

The modeling results in Section II are presented in this section. The turn-on and turn-off transients are divided into several intervals, during which the gate-to-source voltage $v_{GS}(t)$, the drain current $i_D(t)$ and the drain voltage $v_{DS}(t)$ can be calculated analytically with corresponding boundary conditions and constraints. Once the instantaneous waveforms of $v_{GS}(t)$, $i_D(t)$ and $v_{DS}(t)$ are solved, the switching transition time and the switching loss can be easily obtained.

In the experimental prototype, MOSFET Si7860 from Vishay is used and the circuit specifications and the device parameters are listed in Table I. In this case, since $B^2$ is more than $4AC$ depending on the above parameters, the exponential solution occurs as Equation (15).

TABLE I: Circuit Specifications and Device Parameters in Analytical Modeling

| $V_D$=12V, $I_L$=20A, $f_s$=1MHz | | | | | | |
|---|---|---|---|---|---|---|
| $C_{GS}$ (pF) | $C_{GD}$ (pF) | $C_{DS}$ (pF) | $V_{th}$ (V) | $g_{fs}$ (S) | $R_G$: current driven (Ω) | $R_G$: voltage driven (Ω) (external and internal) |
| 1600 | 200 | 500 | 1.8 | 60 | 1 | 1.5 ohm |

Figure 3 shows the switching loss comparison between the above model using Mathcad software and the simulation results based on Si7860AD SPICE model provided by Vishay. It is noted that the modeling results are in good agreement with the simulation results.

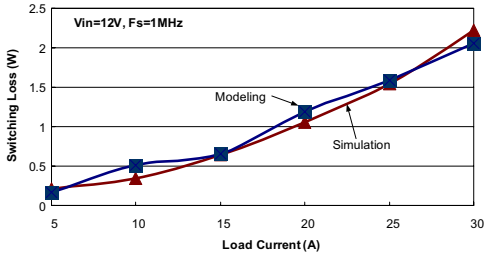


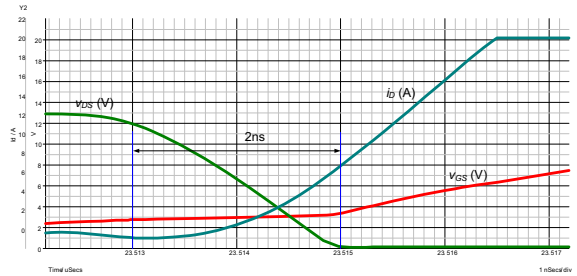

Figure 3 Switching loss comparison between modeling and simulation

For comparison, Figure 4 shows the simulation waveforms of the switching transition between of the resonant driver and the conventional driver with the same parasitic inductance of $L_s$=0.5nH and $L_D$=2nH. It is observed that the turn-on transition time of the resonant driver is reduced to 2ns [see Figure 4(a)] compared to 8.8ns [see Figure 4(c)] of the voltage driver (a reduction of 77%) and similarly, the turn-off transition time of the resonant driver is reduced to 4.6ns [see Figure 4(b)] compared to 10.8ns [see Figure 4(d)] of the voltage driver (a reduction of 57%). Accordingly, from calculation, the turn-on loss is reduced from 0.65W to 0.1W (a reduction of 84.6%) and the turn-off loss is reduced 2.1W to 1.16W (a reduction of 44.8%), which is a significant reduction. So the total switching loss saving is 1.49W (a reduction of 54.2%).

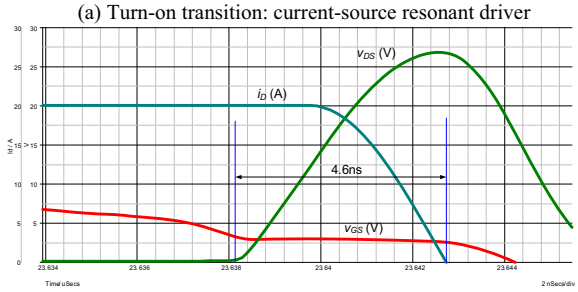
Figure 5 shows the gate charge current during the turn-on transition and turn-off transition of the conventional driver respectively when the common source inductance is not zero.

It is noted that the common source inductance has a significant negative impact on the switching transition of the conventional driver.

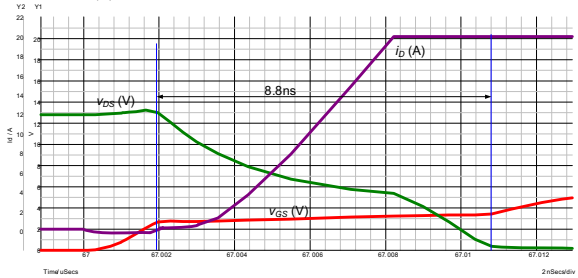
It is observed from Figure 5(a) that during turn-on transition, before the actual gate-to-source voltage $v_{GS}$ reaches the miller plateau voltage, the drain current $i_d$ still remain zero and the gate charging current is about 3A. However, as soon as $i_d$ starts to rise, the induced voltage $v_{Ls}$ ($v_{Ls}=L_s\cdot di_d/dt$) over the common source inductance $L_s$ occurs due to the rise of the drain current, which is against the gate drive voltage $v_{GS}'$. Since $v_{GS}=v_{GS}'-L_s\cdot di_d/dt$, the actual gate-to-source voltage $v_{GS}$ is reduced significantly. As a result, the gate charging current $i_G$ is reduced to as low as 10mA, which increases the turn-on transition time and the turn-on loss dramatically.



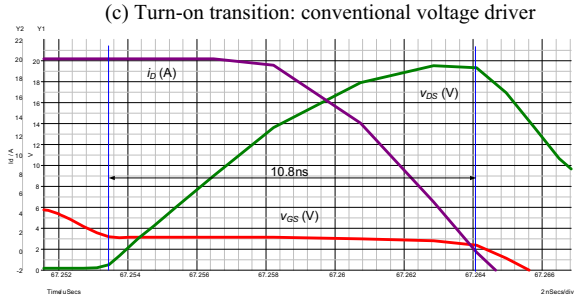

(a) Turn-on transition: current-source resonant driver




(b) Turn-off transition: current-source resonant driver




(c) Turn-on transition: conventional voltage driver



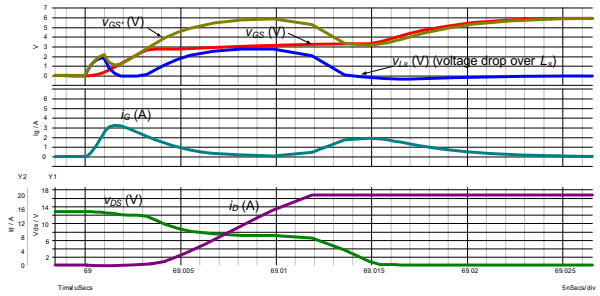

(d) Turn-off transition: conventional voltage driver

Figure 4 Simulation comparison: the gate-to-source voltage $v_{GS}$, the drain-to-source voltage $v_{DS}$, the drain current $i_D$ ($V_{in}$=12V, $I_o$=20A, $f_s$=1MHz, $L_s$=0.5nH, $L_D$=2nH, $R_G$=1.5ohm)

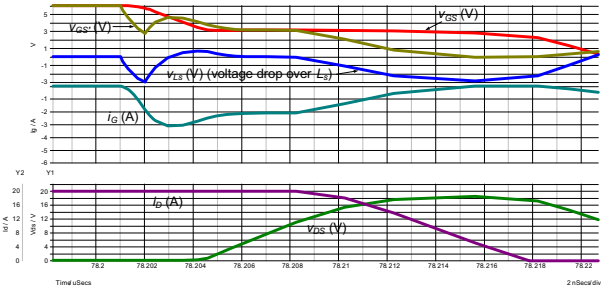
It is observed from Figure 5(b) that during turn-off transition, before the actual gate-to-source voltage $v_{GS}$ declines to the miller plateau voltage, the drain current $i_d$ still remains as the load current and the gate discharging current is around 3A. But, as soon as the drain current begins to decrease, the induced voltage $v_{Ls}$ over $L_s$ occurs, which is also against the gate drive voltage. This also results in the reduction of the gate discharging current to as low as 15mA and thus increases the turn-off transition time and the turn-off loss significantly.

As a conclusion, for both of the turn-on transition and the turn-off transition, the voltage $v_{Ls}$ induced over common source inductance is always against the gate drive voltage $v_{GS'}$, and thus decreases the actual gate-to-source voltage $v_{GS}$ and the gate charge current $i_G$, which consequently slows down the turn-on speed and the turn-off speed of the MOSFET and increases the switching transition time and the switching loss dramatically.

However, as for a current-source resonant driver, the great advantage is that the common source inductance is absorbed by the resonant inductor to ensure the constant drive current during the switching transition. Therefore, the propagation impact of the common source inductance on the switching transition is eliminated, which leads to a significant reduction of the switching transition time and the switching loss.




(a) Turn-on transition: conventional voltage driver




(b) Turn-off transition: conventional voltage driver

Figure 5 Simulation of delay effect of the common source inductance on the conventional driver ($V_{in}$=12V, $I_o$=20A, $f_s$=1MHz, $L_s$=1nH, $L_D$=2nH)

## IV. A Current-Source Resonant Gate Driver

Figure 6 shows the resonant driver under investigation, which is proposed in [10]. Figure 7 shows the key waveforms.

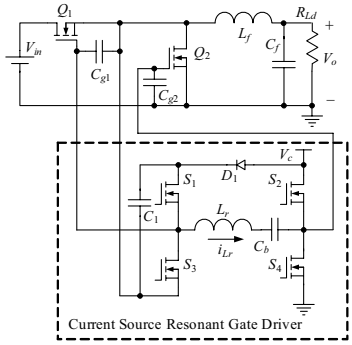



Figure 6 Synchronous buck converter with the proposed current source resonant gate driver

The advantages of this circuit are highlighted as follows: 1) fast switching of the power MOSFET, which reduces the switching time and the switching loss significantly; 2) gate energy recovery; 3) reduced dead time; 4) zero-voltage-switching (ZVS) of the drive switches ($S_1$- $S_4$); 5) high *Cdv/dt* immunity.

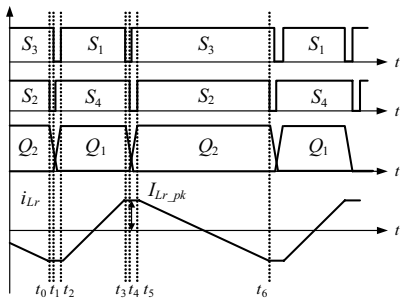



Figure 7 Key waveforms

## V. Proposed Optimization Method

In order to achieve design optimization, the loss analysis of the resonant gate driver is given. The total power loss of the proposed resonant driver includes: (1) the resistive loss and the gate drive loss of switches $S_1$-$S_4$; (2) the loss of the resonant inductor; (3) the resistive loss caused by the internal gate mesh resistance of the power MOSFETs. The detail loss analysis was presented in [10].

As seen from the principle of operation in Figure 7, the peak current $I_{Lr\_pk}$ of the resonant inductor $L_r$ is regarded as the current source magnitude $I_G$. So the higher $I_{Lr\_pk}$ is, the shorter of switching transition is, thus more switching loss can be saved. On the other hand, higher $I_{Lr\_pk}$ will result in a larger RMS value of the inductor circulating current $i_{Lr}$ since the waveform of $i_{Lr}$ is triangular, which increases the resistive circulating loss in the drive circuit and decreases the gate energy recovery efficiency. Therefore it is critical to decide $I_{Lr\_pk}$ (i.e., $I_G$) properly so that the maximum loss saving can be achieved.

The general method proposed here is to find the optimal solution on the basis of the object function that adds the switching loss and the resonant drive circuit loss together. The object function should be a U-shape curve as function of the drive current $I_G$, and the optimization solution is simply located at the lowest point of the curve. It is noted that the analytical loss model proposed in Section II is used to calculate the switching loss since the piecewise loss model is no longer valid due to the parasitic inductance at high frequency. The demonstration of the optimization methodology is employed to the new resonant gate driver. The specifications are: $V_{in}$=12V; $V_o$=1.5V; $I_o$=30A; $V_c$=8V; $f_s$=1MHz; $Q_1$: Si7860DP; $Q_2$: Si7336ADP.

First, the switching loss of the control FET as function of drive current $I_G$ is given in Equation (16)

$$P_{Q1} = \int_0^{t_{sw(on)\_Q1}} v_{ds(on)\_Q1} \cdot i_{d(on)\_Q1} dt \cdot f_s + \int_0^{t_{sw(off)\_Q1}} v_{ds(off)\_Q1} \cdot i_{d(off)\_Q1} dt \cdot f_s \quad (16)$$

where $v_{ds(on)\_Q1}$ and $v_{ds(off)\_Q1}$ are the drain-to-source voltages during turn-on interval and turn-off interval respectively; $i_{(on)\_Q1}$ and $i_{d(off)\_Q1}$ are the drain currents at turn-on interval and turn-off interval respectively; $t_{sw(on)\_Q1}$ is the turn-on switching transition time and $t_{sw(off)\_Q1}$ is the turn-off switching transition time. In Figure 8, the switching loss $P_{switching}$ as function of driven current $I_G$ shows that the switching loss reduces when $I_G$ increases.

Secondly, the total loss of the resonant gate drive circuit as function of drive current $I_G$ is calculated [10]. In Figure 8, the loss of the total gate drive circuit $P_{circuit}(I_G)$ as function of drive current $I_G$ illustrates that the resonant drive circuit loss increases when $I_G$ increases.

Thirdly, in order to find the optimized gate drive current, the objective function is established by adding the switching loss and the resonant driver circuit loss together as

$$F(I_G) = P_{circuit}(I_G) + P_{switching}(I_G) \quad (17)$$

In Figure 8, the objective function $F(I_G)$ with the drive current $I_G$ is a U-shaped curve. Therefore, the optimization solution can be found at the lowest point of the curve, and accordingly, the gate drive current $I_G$ is chosen as 1.2A. Finally, from the selected gate drive current, the calculated resonant inductor value from Equation (18) is 1.5uH,

$$L_r = \frac{(V_{in} + 2V_c) \cdot D \cdot (1-D)}{2 \cdot I_G \cdot f_s} \quad (18)$$

where $V_{in}$=12V, $f_s$=1MHz, $V_o$=1.5V, $V_c$=8V and $I_G$=1.2A.

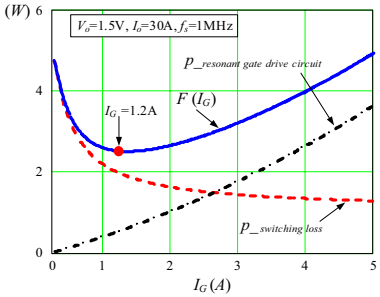



Figure 8 Objective function $F(I_G)$ as function of current $I_G$

Figure 9 illustrates the loss breakdown comparison based on the analytical loss model between the above optimized resonant driver and the conventional diver. At $V_o$=1.5V and $I_o$=20A, the turn-on loss is reduced by 0.55W and the turn-off loss is reduced by 0.94W. The total loss reduction is 1.66W, which is 5.5% (1.66W/1.5V/20A) of the output power.

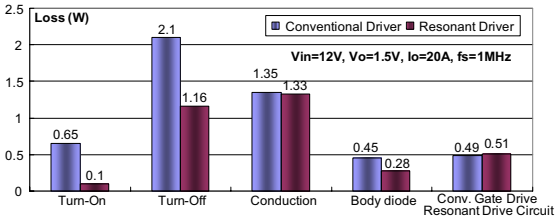



Figure 9 Loss breakdown: resonant gate driver and conventional gate driver

## VI. Hardware Implementation

### A. Bootstrap and Level-shift Circuit

Figure 10 gives the complete schematic of the level-shift drive circuit. It should be pointed out that in order to maintain high efficiency and minimize power dissipation; the level shifters should not draw any current during the on-time of the control switch. Figure 11 shows the schematic of the digital

logic circuit using Quartus II software to achieve the desired control signals for the drive switches. The CPLD MAX II from Altera is used to achieve the programmable dead time function based on the input PWM signal.

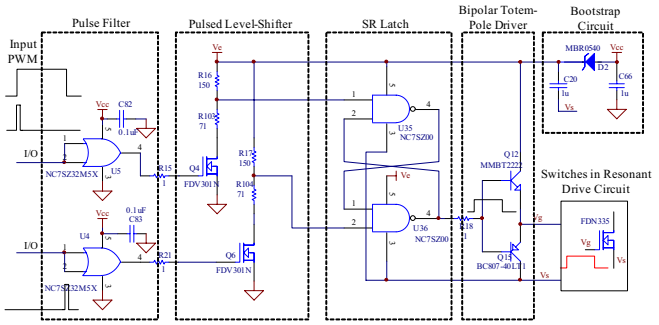



Figure 10 Schematic of the level-shift drive circuit

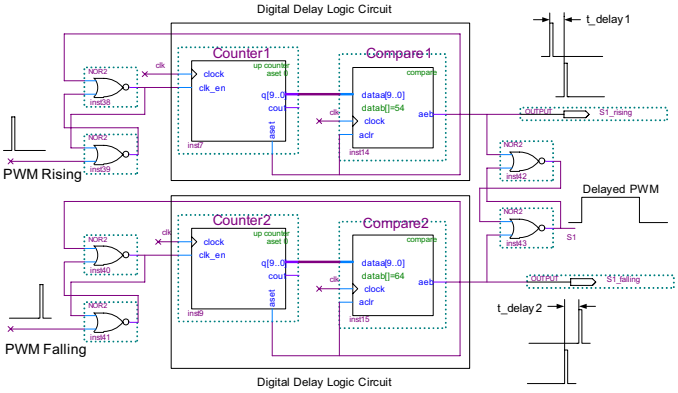



Figure 11 Schematic of the logic circuit in Quartus II software

## VII. Experimental Verification And Discussions

A 1MHz synchronous buck converter with the new resonant driver was built to verify the modeling results and demonstrate the superior advantages. The specifications are as follows: input voltage $V_{in}$=12V; output voltage $V_o$=1.5V; output current $I_o$=30A; switching frequency $f_s$=1MHz; resonant driver voltage $V_c$=8V. The PCB uses six-layer 2 oz copper. The components used in the circuit are listed as follows: Control FET $Q_1$: Si7860DP; Synchronous FET $Q_2$: Si7336ADP; Drive switches $S_1$-$S_4$: FDN335N; Output filter inductance: $L_f$=330nH; Resonant inductor: $L_r$=1.5uH.

Figure 12 shows the gate drive signal $v_{gs\_Q1}$ of the control FET $Q_1$ and $v_{gs\_Q2}$ of the synchronous FET $Q_2$. The crossover level of these two gate signals is less than the threshold voltage of the switches so that the dead time can be minimized significantly and the shoot-through can also be avoided. It is observed that $v_{gs\_Q1}$ is very smooth and no miller plateau is observed as the miller charge is removed very fast with the constant charging current. Moreover the rise time and fall time of $v_{gs\_Q1}$ is less than 15ns, which means very fast switching speed.

Figure 13 shows the drain-source voltage $v_{ds\_Q2}$ and the gate signal $v_{gs\_Q2}$ of the synchronous FET. It can bee seen from $v_{ds\_Q2}$ that the body diode conduction time is very small, which reduces the conduction loss and the reverse recovery loss of the body diode significantly.

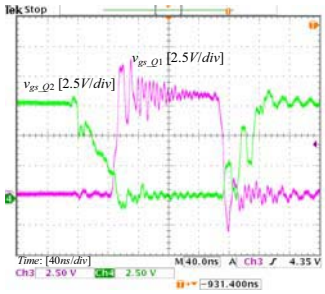



Figure 12 The gate signals $v_{gs\_Q1}$ and $v_{gs\_Q2}$

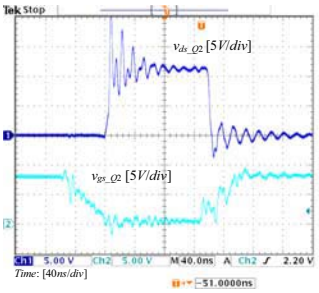



Figure 13 The drain-source voltage $v_{ds\_Q2}$ and the gate signal $v_{gs\_Q2}$

In order to illustrate efficiency improvement by the resonant driver, a benchmark of a synchronous buck converter with the conventional gate driver was built. A Predictive Gate Drive UCC 27222 from Texas Instruments was used as the conventional voltage driver.

Figure 14 shows the measured efficiency comparison for the resonant gate driver and the conventional gate driver at 1.5V output. It is observed that at 20A, the efficiency is improved from 82.7% to 86.6% (an improvement of 3.9%) and at 30A, the efficiency is improved from 76.9% to 83.6% (an improvement of 6.7%).

Figure 15 shows the measured efficiency for the resonant gate driver at different output voltages and load currents. It is observed that at 1.0V/ 20A, the efficiency is 83.5% and it is even higher than 82.7% (see Figure 14) of the conventional driver at 1.5V/20A, which means that we can reduce the output voltage from 1.5V to 1.0V by the resonant gate driver without penalizing the efficiency.

The efficiency comparison of different approaches of 12V VRs at the switching frequency of 1MHz is listed in Table II. Compared to the tapped-inductor buck converter [13], the resonant driver improves the efficiency from 84% to 87% (an improvement of 3%). Compared to the soft-switching phase-shift buck converter [15], the resonant driver improves the efficiency from 82% to 86% (an improvement of 4%). The resonant driver achieves almost the same efficiency as the self-driven soft-switching buck-derived multiphase converter in [16]. But in terms of power density and cost, the current-source driver approach has significant advantages over the self-driven soft-switching buck converter which requires an additional bulk transformer. Furthermore, it should be emphasized that the current-source driver does not change the multiphase buck architecture of today's VRs featuring lower cost and simple control while improving the efficiency in a very cost-effective manner. However, other buck derived approaches requiring additional magnetic components not only reduce the power density significantly, but also increase the cost and the complexity of the circuits and control scheme. In particular, it should also be mentioned that an efficiency improvement of 1.6% at 1.5V/ 20A is also achieved over the Toshiba synchronous buck Multi Chip Module using semiconductor integration approach to minimize the parasitic inductances [14].

TABLE II: EFFICIENCY COMPARION BETWEEN THE RESONANT DRIVER AND DIFFERENT STATE OF THE ART VR APPROACHES

| Input voltage: 12V and switching frequency: 1MHz | | | |
|---|---|---|---|
| VR Topologies | Efficiency | Current/ Phase | Output voltage |
| Tapped-inductor buck converter [13] | 84% | 12.5A | 1.5V |
| Toshiba buck Multi Chip Module (TB7001FL) [14] | 85% | 20A | 1.5V |
| Proposed resonant driver (Figure 15) | 87% | 12.5A | 1.5V |
| | 86.6% | 20A | 1.5V |
| Soft-switching phase-shift buck converter [15] | 82% | 17.5A | 1.3V |
| Self-driven soft-switching multiphase converter [16] | 84.7% | 25A | 1.3V |
| Proposed resonant driver (Figure 15) | 86% | 17.5A | 1.3V |
| | 84.3% | 25A | 1.3V |

Figure 16 shows the measured efficiency and the analytical efficiency based on the loss model. It can be seen that the modeling results matches the experimental result very well.

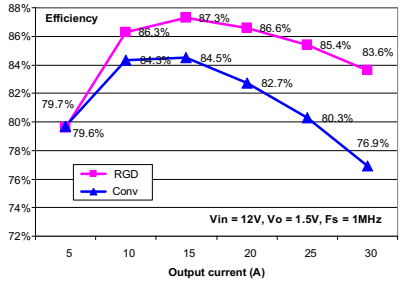



Figure 14 Efficiency comparison at 1.5V / 30A condition: top, resonant gate driver (RGD); bottom: conventional driver (Conv.)

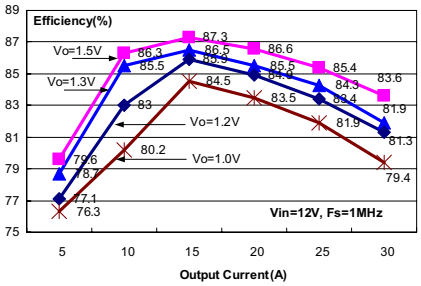



Figure 15 Efficiency with different output voltages and currents with the resonant driver

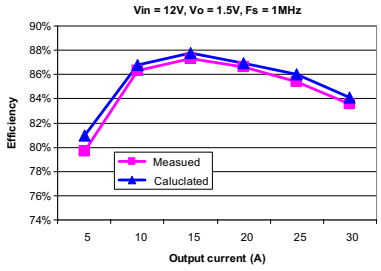



Figure 16 Loss model verification with experimental results

## VIII. CONCLUSION

In this paper, an accurate analytical loss model of a power MOSFET with a current-source resonant driver is developed and the impact of the parasitic inductance is investigated. The superior advantages of a new resonant driver are verified thoroughly by the analytical analysis, simulation and experimental results. Compared to a voltage driver, the resonant driver uses a constant current source to drive the MOSFET gate and therefore, absorbs the parasitic common source inductance. As a result, the switching transition time can be greatly reduced, which leads to a significant reduction of the switching loss. Based on the proposed loss model, a general method to optimize the new resonant gate driver is proposed. A 12V synchronous buck converter with the resonant driver operating at 1 MHz was built to verify the analysis and prove the significant loss saving. The analytical results of the loss model match the simulation results and the experimental results very well and the loss model can be used to optimize a resonant driver at high frequency.

The current-source resonant driver achieves a significant efficiency improvement over the voltage driver. More importantly, compared to other state of the art VR approaches, the resonant driver approach is very promising from the standpoints of both performance and cost-effectiveness.

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