# Switching Loss Analysis Considering Parasitic Loop Inductance with Current Source Drivers for Buck Converters

Zhiliang Zhang (*Member IEEE*)
Aero-Power Sci-tech Center
College of Automation Engineering
Nanjing University of Aeronautics & Astronautics
Nanjing, Jiangsu, P.R.China
Email: zlzhang@nuaa.edu.cn

Jizhen Fu (*Student Member, IEEE*), Yan-Fei Liu (*Senior, Member IEEE*) and P.C. Sen (*Life Fellow IEEE*)
Department of Electrical and Computer Engineering
Queen's University, Kingston, Ontario, Canada, K7L 3N6
jizhen.fu@queensu.ca, yanfei.liu@queensu.ca and senp@post.queensu.ca

***Abstract*— In this paper, the switching loop inductance was investigated on the Current Source Drivers (CSDs). The analytical model was developed to predict the switching losses. It is noted that although the CSDs can reduce the switching transition time and switching loss greatly, the switching loop inductance still has the current holding effect on the CSDs. This results in high turn off loss for the control MOSFET in a buck converter. Thus, an improved layout was proposed to achieve minimum switching loop inductance. The experimental results verified the significant switching loss reduction owing to the proposed layout of a buck converter with 12V input, 1.3V output and 1MHz.**

## I. INTRODUCTION

Voltage Regulators (VRs) with MHz switching frequencies can significantly reduce the size of the output inductances and capacitances, and improve the dynamic response during the transient events. However, the major concern of the high frequency application is excessive frequency-dependent losses including the switching loss, the gate drive loss and the body diode loss etc.

Resonant gate driver technique was proposed to recover large MOSFET drive loss at high frequency (>1MHz), especially for synchronous rectifier (SR) [1]-[4]. Actually, in a buck VR, the switching losses, especially turn off losses, are the dominant loss among the total loss breakdown due to the parasitic inductances. The effect of the common source inductance was investigated thoroughly to predict the switching loss accurately [5]. In order to reduce the switching loss, Current Source Drivers (CSDs) were proposed in [6]-[7] to reduce the switching transition time and switching loss by a constant drive current. Hybrid gate driver scheme proposed in [8] uses the CSD to reduce the high turn off loss of the control MOSFET, while drives the SR with a conventional voltage driver for the purpose of simplicity. In order to achieve optimal design, the loss model on the CSD was proposed in [9] and the current diversion problem was investigated in [10]. However, the effect of the switching loop inductances on the CSD has not been investigated carefully and analytically.

In this paper, the effect of the switching loop inductance is investigated on the CSDs. Through the mathematical modeling and simulation, it is concluded that the switching loop inductance still has the currents hold effect and thus, increases the switching loss significantly. Therefore, in order to improve the performance of the CSD, the switching loop inductance should also be minimized. Thus, an improved layout was proposed for the buck converter with the CSD.

## II. IMPACT OF LOOP PARASITIC INDUCTANCE ON THE CSDS

In order to investigate the impact of the switching loop parasitics on the CSD, the basic clamp circuit as shown in Fig. 1 is used including a MOSFET in series with a diode $D_1$, dc input voltage $V_D$ and an inductive load.

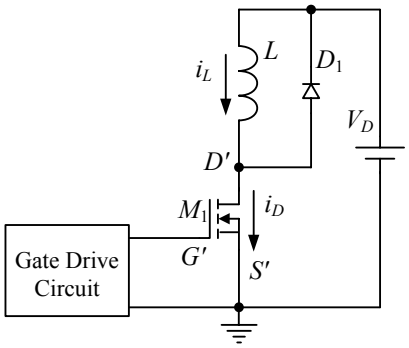



Fig. 1 Circuit with a clamped inductive load

The simplified equivalent circuit for the switching transition is shown in Fig. 2, where MOFET $M_1$ is represented with a typical capacitance model, the clamped inductive load is replaced by a constant current source $I_L$ and the CSD is simplified as a current source ($I_G$). $L_D$ is the switching loop inductance including the packaging

inductance and any unclamped portion of the load inductance. $L_S$ is the common source inductance.

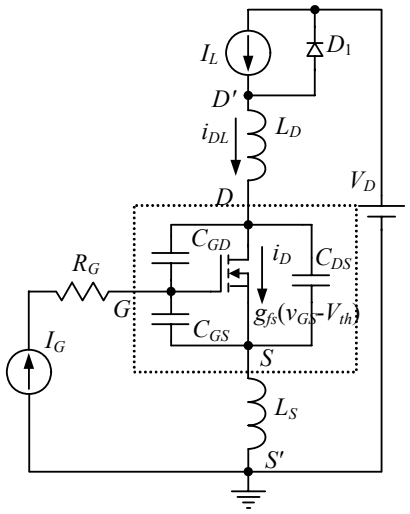



Fig. 2 Equivalent circuit of MOSFET switching transition

In order to simply the transient analysis, the following assumptions are made:

(1) $i_D=g_{fs}(v_{GS}-V_{th})$ and MOSFET is ACTIVE, provided $v_{GS}>V_{th}$ and $v_{DS}>i_DR_{DS(on)}$;

(2) For $v_{GS}<V_{th}$, $i_D=0$, and MOSET is OFF;

(3) When $g_{fs}(v_{GS}-V_{th})> v_{DS}/R_{DS(on)}$, the MOSFET is fully ON.

During the switching transition period, the MOSFET enters its active state and the linear transfer characteristics is assumed as given in (1) [11], where $i_D(t)$ is the instantaneous switching current and $v_{GS}(t)$ is the instantaneous gate-to-source voltage of the MOSFET:

$$i_D(t) = g_{fs}(v_{GS}(t) - V_{th}) \tag{1}$$

According the equivalent circuit in Fig. 2, the circuit equations take the form

$$I_G = C_{GD}\frac{dv_{GD}}{dt} + C_{GS}\frac{dv_{GS}}{dt} \tag{2}$$

And

$$v_{GD} = v_{GS} - v_{DS} \tag{3}$$

So

$$I_G = (C_{GS} + C_{GD})\frac{dv_{GS}}{dt} - C_{GD}\frac{dv_{DS}}{dt} \tag{4}$$

From(4), $dv_{DS}/dt$ is solved as

$$\frac{dv_{DS}}{dt} = \frac{C_{GS}+C_{GD}}{C_{GD}}\cdot\frac{dv_{GS}}{dt} - \frac{I_G}{C_{GD}} \tag{5}$$

So $d^2v_{DS}/dt^2$ and $d^3v_{DS}/dt^3$ are respectively

$$\frac{d^2v_{DS}}{dt^2} = \frac{C_{GS}+C_{GD}}{C_{GD}}\cdot\frac{d^2v_{GS}}{dt^2} \tag{6}$$

$$\frac{d^3v_{DS}}{dt^3} = \frac{C_{GS}+C_{GD}}{C_{GD}}\cdot\frac{d^3v_{GS}}{dt^3} \tag{7}$$

During the switching interval, the change of the switching loop current $i_{DL}$ induces a voltage across the parasitic inductance. The drain-to-source voltage $v_{DS}$ is given as

$$\begin{aligned} v_{DS} &= V_D - L_D\frac{di_{DL}}{dt} - L_s\frac{d(i_{DL}+I_G)}{dt} \\ &= V_D - (L_D+L_s)\frac{di_{DL}}{dt} \end{aligned} \tag{8}$$

And

$$i_{DL} = C_{GS}\frac{dv_{GS}}{dt} + C_{DS}\frac{dv_{DS}}{dt} + g_{fs}(v_{GS}-V_{th}) - I_G \tag{9}$$

Substituting (9) to (8) yields

$$\begin{aligned} v_{DS} = V_D - (L_D+L_s)(C_{GS}\frac{d^2v_{GS}}{dt^2} + \\ C_{DS}\frac{d^2v_{DS}}{dt^2} + g_{fs}\frac{dv_{GS}}{dt}) \end{aligned} \tag{10}$$

Substituting (6) to (10) yields

$$\begin{aligned} v_{DS} &= V_D - (L_D+L_s) \\ &(\frac{C_{GS}C_{GD}+C_{DS}C_{GD}+C_{DS}C_{GS}}{C_{GD}}\cdot\frac{d^2v_{GS}}{dt^2} + g_{fs}\frac{dv_{GS}}{dt}) \end{aligned} \tag{11}$$

Differentiating (11) yields

$$\begin{aligned} \frac{dv_{DS}}{dt} &= -(L_D+L_s) \\ &(\frac{C_{GS}C_{GD}+C_{DS}C_{GD}+C_{DS}C_{GS}}{C_{GD}}\cdot\frac{d^3v_{GS}}{dt^3} + g_{fs}\frac{d^2v_{GS}}{dt^2}) \end{aligned} \tag{12}$$

Substituting (5) into (12), (13) is derived

$$A\frac{d^3v_{GS}(t)}{dt^3} + B\frac{d^2v_{GS}(t)}{dt^2} + C\frac{dv_{GS}(t)}{dt} = I_G \tag{13}$$

where parameters $A$, $B$ and $C$ are represented in terms of the device parameters ($C_{GS}$, $C_{GD}$, $C_{DS}$, $g_{fs}$ and $R_G$) and the equivalent circuit parameters ($L_D$ and $L_S$) as $A = (L_D+L_s)(C_{GS}C_{GD}+C_{DS}C_{GD}+C_{DS}C_{GS})$, $B = g_{fs}(L_D+L_s)C_{GD}$ and $C = C_{GS}+C_{GD}$.

For turn-on transition, the initial condition for (13) is $v_{GS}(0)=V_{th}$. Then (13) solves to give either sinusoidal or exponential solutions, depending on the relative magnitudes of $B^2$ and $AC$.

When $B^2 - 4AC < 0$, sinusoidal solution occurs and $v_{GS}(t)$ takes the form:

$$\begin{aligned} v_{GS}(t) &= (\frac{B^2}{2C^2\cdot\sqrt{4AC-B^2}} - \frac{\sqrt{4AC-B^2}}{2C^2})\cdot \\ &I_G\cdot\exp(-\frac{t}{T_1})\cdot Sin(\omega_1 t) + \frac{B}{C^2}\cdot I_G\cdot\exp(-\frac{t}{T_2})\cdot Cos(\omega_1 t) \\ &+\frac{I_G\cdot t}{C} - \frac{B}{C^2}\cdot I_G + V_{th} \end{aligned} \tag{14}$$

where $T_1 = \frac{2A}{B}$, $\omega_1 = \frac{\sqrt{4AC - B^2}}{2A}$.

When $B^2 - 4AC > 0$, exponential solution occurs. Then $v_{GS}(t)$ takes the form

$$v_{GS}(t) = -\frac{(\sqrt{B^2 - 4AC} + B) \cdot I_G \cdot A \cdot \exp(-\frac{t}{T_2})}{(\sqrt{B^2 - 4AC} - B) \cdot C \cdot \sqrt{B^2 - 4AC}} + \frac{(\sqrt{B^2 - 4AC} - B) \cdot I_G \cdot A \cdot \exp(-\frac{t}{T_3})}{(\sqrt{B^2 - 4AC} + B) \cdot C \cdot \sqrt{B^2 - 4AC}} + \frac{I_G \cdot t}{C} - \frac{B \cdot I_G}{C^2} + V_{th}, \quad (15)$$

where $T_2 = \frac{2A}{B - \sqrt{B^2 - 4AC}}$ and $T_3 = \frac{2A}{B + \sqrt{B^2 - 4AC}}$.

Then, by substituting $v_{GS}(t)$ to (1) and (11), $i_D(t)$ and $v_{DS}(t)$ of the MOSFET can be calculated respectively. Therefore, the turn on loss is

$$P_{turn\_on} = \int_0^{t_{sw(on)\_Q1}} v_{DS}(t) \cdot i_D(t) dt \cdot f_s \quad (16)$$

The turn-off transition is similar to the turn-on transition except for the initial condition becomes $v_{GS}(0) = V_{th} + \frac{I_L}{g_{fs}}$.

The turn off loss is

$$P_{turn\_off} = \int_0^{t_{sw(off)\_Q1}} v_{DS}(t) \cdot i_D(t) dt \cdot f_s \quad (17)$$

From (16) and (17), the switching loss is

$$P_{switching} = P_{turn\_off} + P_{turn\_on} \quad (18)$$

Fig. 3 shows the simulated the waveforms of the turn off transition with different switching loop inductances. It is observed that the drain-to-source current $i_D$ with 4nH has a slower decay rate with longer turn off time as it is held by the loop inductances. As a result, the switching loss (turn off loss) is increased with higher loop inductance. The peak value of $p_{loss}$ is increased from 490W to 690W (an increase of 40%) with longer turn off time.

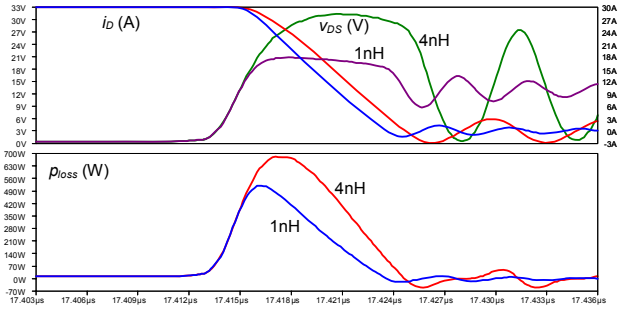



Fig. 3 Turn off transition comparison with $L_D$=4nH and $L_D$=1nH

## III. Improved Layout to Minimize the Parasitic Effects

From Section II, the switching loop inductances increase the switching transition time and hold the drain current of the MOSFET. This leads to higher switching loss. Particularly, this problem becomes more serious in a high frequency buck converter since the switching loss (especially turn off loss) is the dominant loss.

Fig. 4 shows the synchronous buck converter with the loop parasitic inductance $L_{d1}$, $L_{s1}$, $L_{d2}$ and $L_{s2}$. The basic idea is to reduce the switching loop inductance, and thus high turn off losses. As shown in Fig. 5, the input decoupling capacitance $C_{in}$ is rearranged compared to Fig. 4. In this way, the parasitic inductances $L_{d1}$ and $L_{GND}$ can be significantly reduced. Based on this concept, two different layouts of the buck converter were implemented in the experimental test.

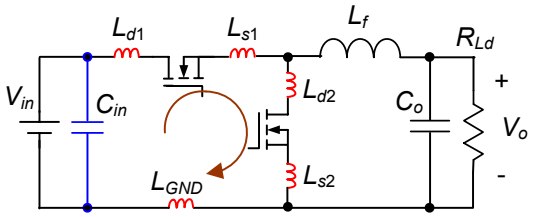



Fig. 4 Buck converter with the loop parasitics

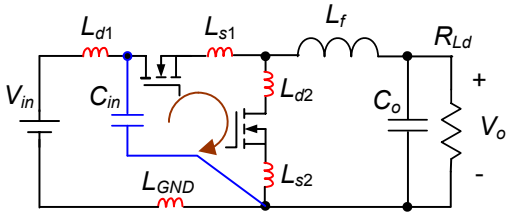



Fig. 5 Buck converter with rearranged input decoupling capacitance to reduce the loop parasitics

## IV. Experimental Results and Discussion

In order to verify the efficiency improvement of the proposed layout arrangement, a 1MHz synchronous buck converter was built with the CSD as shown in Fig. 6. In order to reduce the dominant loss (the switching loss) in the buck converter in a cost-effective manner, a new hybrid gate drive scheme as shown in Fig. 6 is proposed for a buck converter. For the control MOSFET $Q_1$, the high side CSD proposed in [12] is used to achieve the switching loss reduction. For the SR $Q_2$, the conventional voltage source driver is used for low cost and simplicity, which is the bipolar totem-pole drive structure. PWM_SR is the signal fed into the bipolar totem-pole pair.

The specifications are as follows: input voltage $V_{in}$=12 V; output voltage $V_o$=1.3V; output current $I_o$=30A; switching frequency $f_s$=1 MHz; gate driver voltage $V_c$=5V. The PCB uses six-layer with 4 oz copper. The components used in the circuit are: $Q_1$: Si7860DP; $Q_2$: IRF6691; output filter inductance: $L_f$=300nH; current-source inductor: $L_r$=18nH (SMT 1812SMS-18N, Coilcraft); drive switches $S_1$-$S_4$: FDN335.

Photos of the prototype are illustrated in Fig. 7. The driver was built using discrete components and an Altera Max II EPM240 CPLD was used to generate the driver gate signals as illustrated in Fig. 7 (a). Surface mount (SMT) air core was used for the inductor as illustrated in Fig. 7 (b).

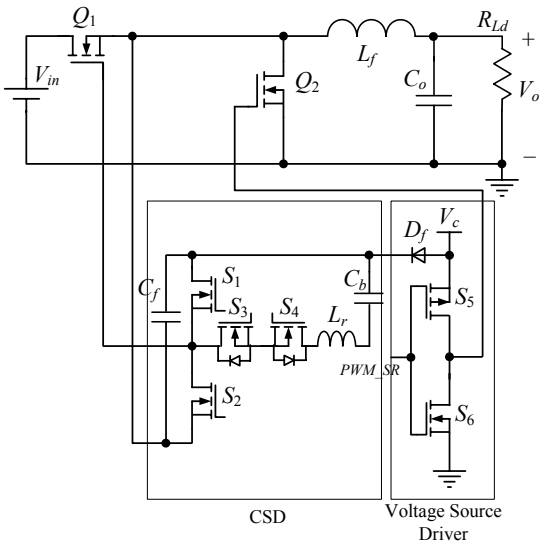
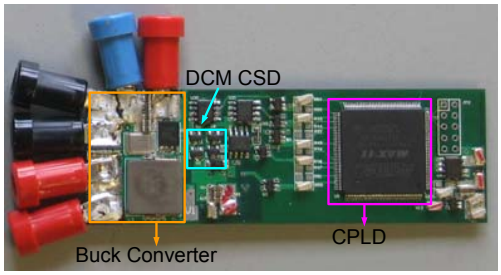
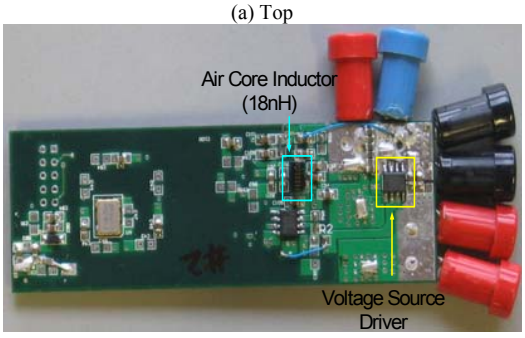



Fig. 6 Buck VR with hybrid driver scheme




(a) Top




(b) Bottom

Fig. 7 Photos of the synchronous buck prototype with the hybrid gate driver

Fig. 8 shows the original power stage layout of the buck converter. The switching loop is highlighted in blue and the loop inductance is 10.5nH@1MHz measured with Agilent 4395A Analyzer. The power stage layout was rearranged to have much smaller switching loop as shown in Fig. 9. The measured loop inductance is only 3.7nH@1MHz, a reduction of 65%. The major difference between layout #1 an #2 is that input decoupling capacitances reduce the ground trace inductance and provide the transient energy, therefore, the negative impact of the switching loop inductance is reduced greatly. This is very important for the CSD to reduce the high switching losses.

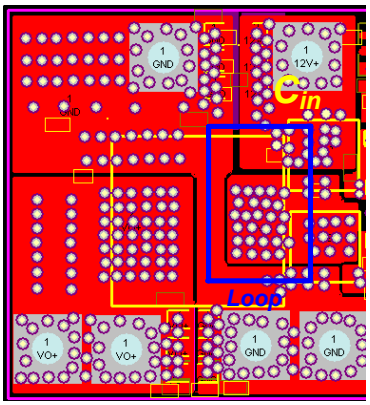



Fig. 8 Buck stage: #1

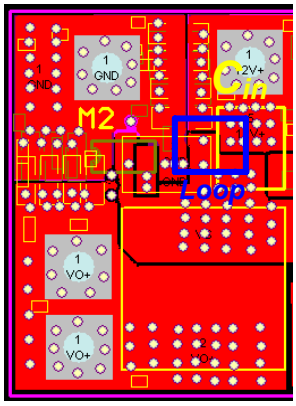



Fig. 9 Buck stage: #2

Fig. 10 and Fig. 11 illustrate the drain-to-source voltages of the SR MOSFET for layout #1 and #2 respectively. It is noted that compared to the layout #1, the layout #2 with reduced loop inductance alleviates the oscillation of the drain-to-source voltage greatly, which results from the parasitic inductance and reverse recovery of the SR body diode.

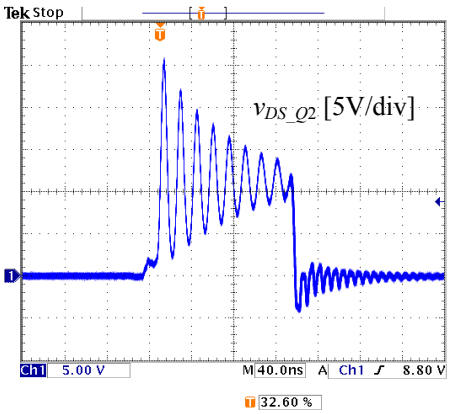



Fig. 10 Drain-to-source voltage at $I_o$=30A: Buck #1

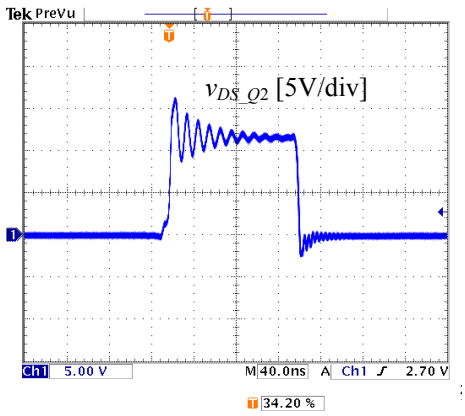



Fig. 11 Drain-to-source voltage at $I_o$=30A: Buck #2

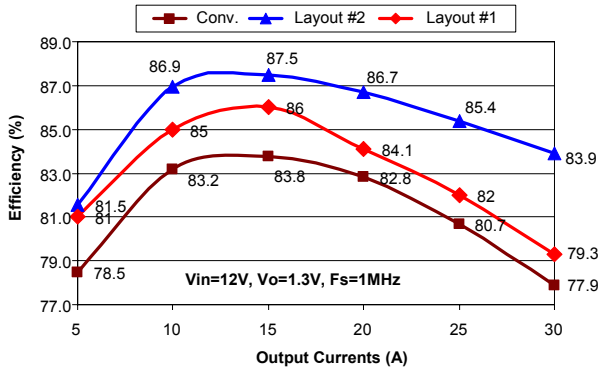



Fig. 12 Efficiency comparison: top: Buck #2; mid: Buck #1; bottom: conventional voltage driver (Conv.)

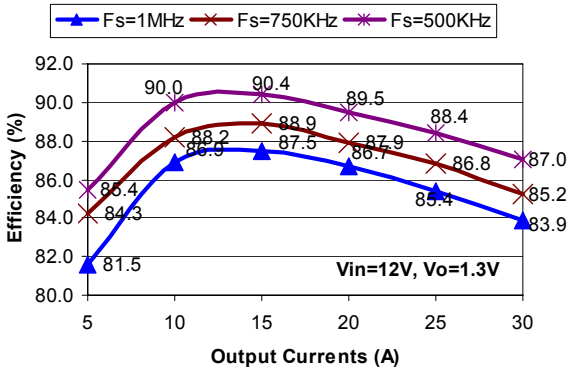



Fig. 13 Efficiency with different currents and switching frequencies at $V_o$=1.3V

Fig. 12 shows the measured efficiency comparison for two different layouts at 1.3V output. It is observed that at 20A, the efficiency is improved from 84.1% to 86.7% (an improvement of 2.6%) and at 30A, the efficiency is improved from 79.3% to 83.9% (an improvement of 4.6%). Higher efficiency improvement is achieved when the load current increases. This is because the switching loop inductance has stronger current holding effect with the higher load current. It is also noted the CSD with the layout #2 achieves higher efficiency than the conventional voltage gate driver. In the test, the predictive gate drive UCC 27222 from Texas Instruments was used as the conventional voltage driver.

Fig. 13 shows the measured efficiency for the CSD at different load currents and $V_o$=1.3V when the switching frequency changes. It is observed that at the load current of 30A, when the switching frequency changes from 1MHz to 500KHz, the efficiency is improved from 83.9% to 87%.

## V. Conclusion

In this paper, the switching loop inductance was investigated on the CSDs and the analytical model was developed to predict the switching losses accurately. The CSDs can reduce the effect of the common source inductance to expedite the switching speed and switching loss. However, the switching loop inductance still has the current holding effect on the CSDs. This will weaken the effectiveness of the CSDs in the sense of the switching loss reduction. Therefore, the switching loop inductance should also be minimized.

Based on this conclusion, an improved layout was proposed here to achieve minimum switching loop inductances compared to the original buck layout. The experimental results verified the efficiency improvement.

## References


[1] D. Maksimovic, "A MOS gate drive with resonant transitions," in *Proc. IEEE Power Electronics Specialists Conference (PESC)*, 1991, pp. 527-532.

[2] L. Huber, K. Hsu, M. M. Jovanovic, D. J. Solley, G. Gurov and R. M. Porter, "1.8-MHz, 48-V resonant VRM: analysis, design, and performance evaluation," *IEEE Trans. Power Electron.*, Vol. 21, No. 1, pp.79-88, Jan. 2006.

[3] J. R. Warren, K. A. Rosowski and D. J. Perreault, "Transistor selection and design of a VHF DC-DC power converter," *IEEE Trans. Power Electron.*, Vol. 23, No. 1, pp.27 – 37, Jan. 2008.

[4] G. Spiazzi, P. Mattavelli and L. Rossetto, "Effects of parasitic components in high-frequency resonant drivers for synchronous rectification MOSFETs," *IEEE Trans. Power Electron.*, Vol. 23, No. 4, pp. 2082-2092, Jul. 2008.

[5] Y. Ren, M. Xu, J. Zhou and F. C. Lee, "Analytical loss model of power MOSFET," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 310 - 319, Mar. 2004.

[6] W. Eberle, Z. Zhang, Y. F. Liu and P. C. Sen, "A current source gate driver achieving switching loss savings and gate energy recovery at 1-MHz," *IEEE Trans. Power Electron.*, Vol. 23, No. 2, pp. 678-691, Mar. 2008.

[7] Z. Yang, S. Ye and Y. F. Liu, "A new resonant gate drive circuit for synchronous buck converter," *IEEE Trans. Power Electron.*, Vol. 22, No. 4, pp.1311-1320, July 2007.

[8] Z. Zhang, W. Eberle, Z. Yang, Y. F. Liu and P.C. Sen, "A new hybrid gate drive scheme for buck voltage regulators," in *Proc. IEEE Power Electronics Society Conference (PESC)*, June, 2008, pp.2498-2503.

[9] Z. Zhang, W. Eberle, Z. Yang, Y. F. Liu and P.C. Sen, "Optimal design of resonant gate driver for buck converter based on a new analytical loss model," *IEEE Trans. Power Electron.*, Vol. 23, No. 2, pp.653-666, Mar. 2008.

[10] J. Fu, Z. Zhang, Y. F. Liu and P. C. Sen, "A high efficiency current source driver with negative gate voltage for buck voltage regulators," IEEE Energy Conversion Congress and Exposition (ECCE 2009), Sep., San Jose, U. S..

[11] Duncan A. Grant and John Gowar, "Power MOSFET theory and applications," A Wiley- Interscience Publication, Feb. 1989, pp. 97-143.

[12] Z. Zhang, J. Fu, Y. F. Liu and P. C. Sen, "A new discontinuous current-source driver for high frequency power MOSFETs," *IEEE Energy Conversion Congress and Exposition* (*ECCE* 2009), Sep., pp. 1655-1662.