Letters

Switching Loss Analysis Considering Parasitic Loop Inductance With Current Source Drivers for Buck Converters

Zhiliang Zhang, Jizhen Fu, Yan-Fei Liu, and Paresh C. Sen

***Abstract*—In this letter, the switching loop inductance was investigated on the current-source drivers (CSDs). The analytical model was developed to predict the switching losses. It is noted that although the CSDs can greatly reduce the switching transition time and switching loss, the switching loop inductance still causes the current holding effect on the CSDs. This results in high turn-off loss for the control MOSFET in a buck converter. An improved layout was proposed to achieve minimum switching loop inductance. The experimental results verified the significant switching loss reduction owing to the proposed layout of a 1-MHz buck converter with 12-V input, and 1.3-V and 30-A output.**

***Index Terms*—Buck converter, current-source driver (CSD), power MOSFET, resonant gate driver, voltage regulator (VR), voltage regulator module (VRM).**

I. Introduction

ACCORDING to Intel microprocessor's road map in [1], the microprocessors operate at extremely low voltages (<1 V) and high currents (>100 A) with the continuous increase of the operating speed and transistors within the chips. For example, for Dual-Core Intel Xeon Processor 7000/7100 series processor, the VRM/EVRD 11.0 is required as follows: 1) a maximum continuous load current of 130 A; b) a maximum load current of 150-A peak; and 3) a maximum current slew rate of 1200 A/μs at the lands of the processor.

In the point-of-load regulation system, a dedicated dc/dc converter, known as a voltage regulator module (VRM), is used to deliver a highly accurate supply voltage to the microprocessor. To increase power density and dynamic response, high switching frequency (>1 MHz) of VRMs is strongly desired. Unfortunately, higher switching frequency normally results in higher frequency-dependent loss. In buck VRMs, conventional voltage-source gate drivers are used for the MOSFETs. When the switching frequency is over 1 MHz, the excessive gate drive loss becomes a penalty. Therefore, resonant gate driver technique was proposed to recover large MOSFET drive loss at high frequency (>1 MHz), especially for synchronous rectifier (SR) [2]–[5]. Furthermore, in megahertz buck converters with the conventional voltage drivers, the switching loss, especially turn-off losses, is the dominant loss among the total loss breakdown due to the parasitic inductance. For example, in a 1-MHz, 12-V, input and 20-A output buck converter with the conventional voltage driver (Control FET: Si7860DP; SR FET: Si7336ADP), the switching loss is as much as 2.7 W (55.1% of the total loss) [6].

In order to reduce the switching transition time and thus the switching loss, current-source drivers (CSDs) were proposed in [7]–[9]. In order to achieve optimal design, the simple loss model of the CSD was proposed in [10] and applied to a full-bridge topology CSD with a discontinuous current. The switching behavior with the conventional voltage drivers considering the common source inductance (CSI) and the switching loop inductance was studied in [11] and [12]. The current diversion problem caused by the CSI was investigated in [13] and [14], and the improved circuits were proposed to enhance the effectiveness of the CSDs. However, the effect of the switching loop inductance on the CSD, which is important to the CSD performance in a practical design, has not been carefully and analytically investigated.

The objective of this letter is to investigate the effect of the switching loop inductance on the CSDs. Through the mathematical modeling and simulation, it is observed that the switching loop inductance still causes the currents hold effect and thus significantly increases the switching loss. In order to improve the performance of the CSD, the switching loop inductance should also be minimized in practical design. Therefore, an improved layout was proposed for the buck converter with the CSD.

II. Impact of Loop Parasitic Inductance on the CSDs

In order to investigate the impact of the switching loop inductance on the CSD, the basic clamp circuit shown in Fig. 1 is used including a MOSFET in series with a diode D_1, dc input voltage V_D, and an inductive load.

The simplified equivalent circuit for the switching transition is shown in Fig. 2, where MOSFET M_1 is represented with a typical capacitance model, the clamped inductive load is replaced

Manuscript received June 14, 2010; revised October 8, 2010; accepted November 20, 2010. Date of current version August 3, 2011. This work was supported by Natural Science Foundation of China under Grant 51007036 and by Delta Power Electronics Science and Education Development Fund. Recommended for publication by Associate Editor A. E. Andersen.

Z. Zhang is with the Aero-Power Sci-Tech Center, College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China (e-mail zlzhang@nuaa.edu.cn).

Y. -F. Liu, P. C. Sen, and J. Fu are with the Department of Electrical and Computer Engineering Queen's University, Kingston, ON K7 L 3N6, Canada (e-mail: jizhen.fu@queensu.ca; yanfei.liu@queensu.ca; senp@post.queensu.ca).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2010.2096476

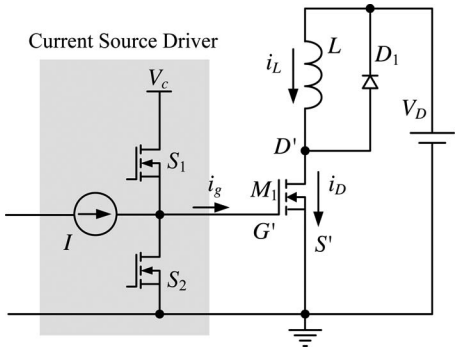

Fig. 1. CSD with a clamped inductive load

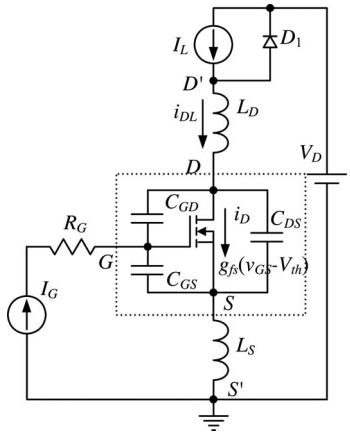

Fig. 2. Clamped inductive load circuit with the parasitic components and CSD. (a) $L_D = 2$ H. (b) $L_D = 4$ nH.

by a constant current source I_L, and the CSD is simplified as a current source (I_G). L_D is the switching loop inductance including the packaging inductance and any unclamped portion of the load inductance; L_S is the CSI.

A. Analytical Modeling of Main Switching Transition

The key point of the modeling is to find the relationship between the switching loss and the loop inductance. The switching loss happens when the MOSFET enters its active state and the linear transfer characteristics is assumed as given in (1) [15], where $i_D(t)$ is the instantaneous switching current and $v_{GS}(t)$ is the instantaneous gate-to-source voltage of the MOSFET

$$i_D(t) = g_{f_s}(v_{GS}(t) - V_{\rm th}). \tag{1}$$

According the equivalent circuit in Fig. 2, the circuit equations take the form

$$I_G = C_{GD}\frac{dv_{GD}}{dt} + C_{GS}\frac{dv_{GS}}{dt} \tag{2}$$

$$v_{GD} = v_{GS} - v_{DS} \tag{3}$$

$$v_{DS} = V_D - L_D\frac{di_{DL}}{dt} - L_s\frac{d(i_{DL}+I_G)}{dt} = V_D - (L_D + L_s)\frac{di_{DL}}{dt} \tag{4}$$

$$i_{DL} = C_{GS}\frac{dv_{GS}}{dt} + C_{DS}\frac{dv_{DS}}{dt} + g_{f_s}(v_{GS} - V_{\rm th}) - I_G. \tag{5}$$

From (2), (3), (4), and (5), the following is derived:

$$A\frac{d^3v_{GS}(t)}{dt^3} + B\frac{d^2v_{GS}(t)}{dt^2} + C\frac{dv_{GS}(t)}{dt} = I_G \tag{6}$$

where $A = (L_D + L_s)(C_{GS}C_{GD} + C_{DS}C_{GD} + C_{DS}C_{GS})$, $B = g_{f_s}(L_D + L_s)C_{GD}$, and $C = C_{GS} + C_{GD}$. From (6), $v_{GS}(t)$ can be derived to be as a function of L_D and L_S. It is either a sinusoidal or exponential solution, depending on the relative magnitudes of B^2 and AC.

By substituting $v_{GS}(t)$ to (1) and (4), $i_D(t)$ and $v_{DS}(t)$ of the MOSFET can be calculated, respectively, and then the switching loss can be predicted. It should be noted that $v_{GS}(t)$, $i_D(t)$, and $v_{DS}(t)$ are all function of the parasitic inductance L_D, and therefore, the switching loss is also a function of L_D.

B. Analytical Modeling Results

The modeling results are presented in the following section. The turn-on and turn-off transients are divided into several intervals, during which the gate-to-source voltage $v_{GS}(t)$, the drain current $i_D(t)$, and the drain voltage $v_{DS}(t)$ can be calculated analytically with corresponding boundary conditions and constraints. Once the instantaneous waveforms of $v_{GS}(t)$, $i_D(t)$, and $v_{DS}(t)$ are solved, the switching transition time and the switching loss can be obtained.

The circuit specifications and the device parameters are listed in Table I, where MOSFET Si7860 from Vishay is used. The estimated values of the parasitic inductance are $L_s = 2$ nH and $L_D = 2$ nH by Maxwell simulation software from Ansoft [16].

Fig. 3 shows the calculated modeling results of the turn-off transition comparison with different loop inductance using the Mathcad software. As seen from Fig. 3(a) and (b), it is observed that the drain-to-source current i_D with $L_D = 2$ nH has a slower decay rate and thus longer turn-off time as it is held by the loop inductance. The turn-off time increases from 4 ns [seen in Fig. 3(a)] to 6.5 ns [seen in Fig. 3(b)] when L_D increases from 2 to 4 nH. As a result, the turn-off loss is increased from 0.82 to 1.38 W (an increase of 68%) with longer turn-off time. Therefore, the turn off loss is increased with higher loop inductance.

III. Improved Layout to Minimize the Parasitic Effects

From Section II, the switching loop inductance increases the switching transition time and holds the switching current. This leads to higher switching loss. Particularly, this problem becomes more serious in a synchronous buck converter, where the switching loss (especially the turn-off loss) is dominant.

Fig. 4 shows the synchronous buck converter with the loop parasitic inductance L_{d1}, L_{s1}, L_{d2}, and L_{s2}. $C_{\rm in}$ is the input decoupling capacitance. The basic idea is to reduce the switching loop inductance, and thus reduce the high turn-off loss. In order to reduce the loop inductance in Fig. 4, $C_{\rm in}$ is rearranged as

TABLE I
CIRCUIT SPECIFICATIONS AND DEVICE PARAMETERS IN ANALYTICAL MODELING

V_D=12V, I_L=20A, f_s=1MHz						
C_{GS} (pF)	C_{GD} (pF)	C_{DS} (pF)	V_{th} (V)	g_{fs} (S)	R_G: current driven (Ω)	R_G: voltage driven (Ω) (external and internal)
1600	200	500	1.8	60	1	1.5

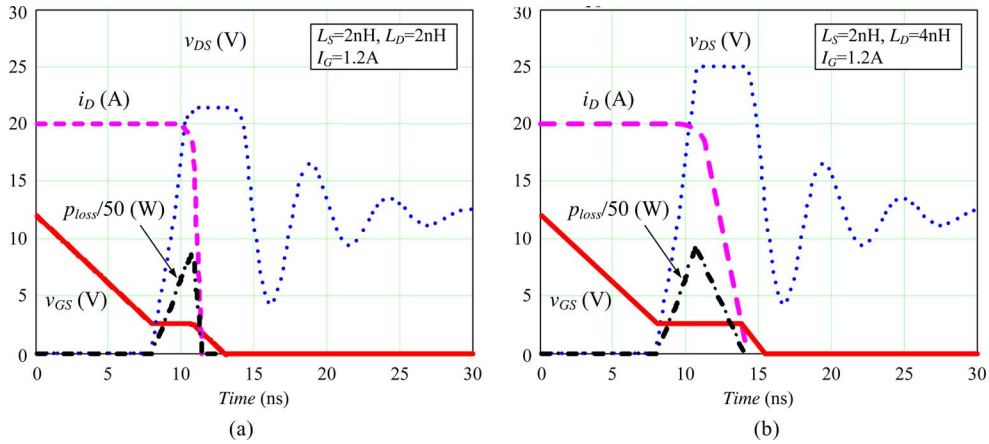

Fig. 3. Turn-off transition comparison.

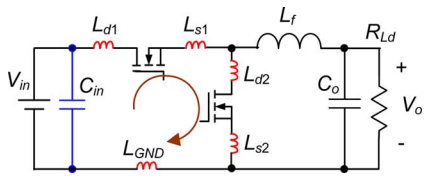

Fig. 4. Buck converter with the loop parasitic inductance.

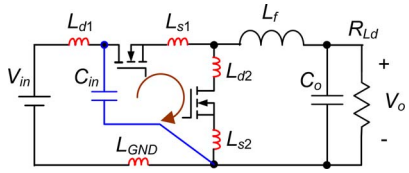

Fig. 5. Buck converter with rearranged input decoupling capacitance to reduce the loop parasitic inductance.

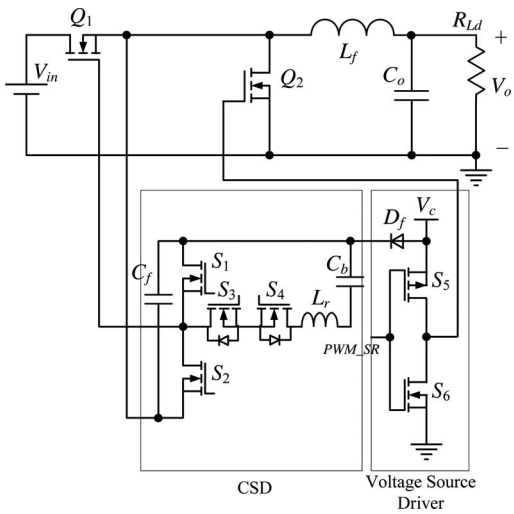

Fig. 6. Buck VR with hybrid driver scheme.

shown in Fig. 5. In this way, the parasitic inductance L_{d1} and L_{GND} can be significantly reduced. Based on this concept, two different layouts of the buck converter were implemented in the experimental test.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

In order to verify the efficiency improvement of the proposed layout arrangement, a 1-MHz synchronous buck converter with the CSD, as shown in Fig. 6, was built. For the control MOSFET Q_1, the high-side CSD proposed in [17] is used to achieve the switching loss reduction. The specifications are as follows: $V_{\mathrm{in}} = 12$ V; $V_o = 1.3$ V; $I_o = 30$ A; $f_s = 1$ MHz; and $V_c = 5$ V. The PCB uses six layers with 4 oz copper. The components used are: Q_1: Si7860DP; Q_2: IRF6691; $L_f = 300$ nH; $L_r = 18$ nH (SMT 1812SMS-18 N, Coilcraft); and $S_1 - S_4$: FDN335. The implementation of the bootstrap with level-shift circuit and CPLD can be found in [18].

Fig. 7 shows the original power stage layout (#1) of the buck converter, referring to Fig. 4. The switching loop is highlighted in white and the loop inductance is 10.5 nH at 1 MHz measured with Agilent 4395 A Analyzer. For comparison, Fig. 8 shows the rearranged power stage layout (#2) with much smaller switching loop, referring to Fig. 5. The measured loop inductance is only 3.7 nH at 1 MHz, a reduction of 65%. The major layout difference between #1 and #2 is that the input decoupling capacitances reduce the ground trace inductance significantly and provide the transient energy. Therefore, the negative impact of the switching loop inductance is greatly reduced, which is important for the CSD to reduce the high switching losses.

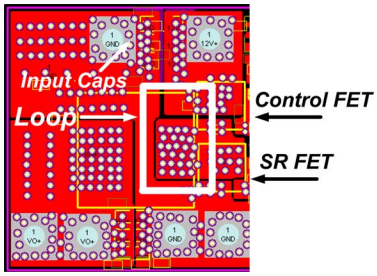

Fig. 7. Buck stage layout: #1, referring to Fig. 4.

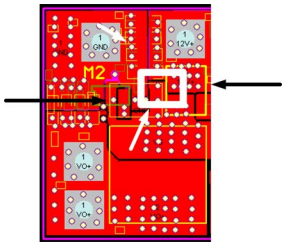

Fig. 8. Buck stage layout: #2, referring to Fig. 5.

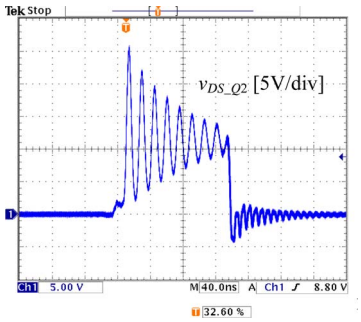

Fig. 9. Drain-to-source voltage at $I_o = 30$ A: #1

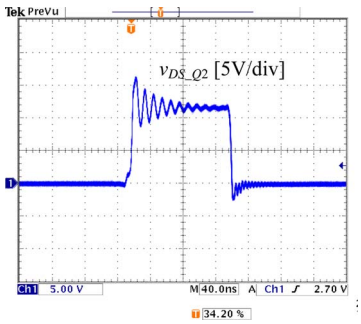

Fig. 10. Drain-to-source voltage at $I_o = 30$ A: #2.

Figs. 9 and 10 illustrate the drain-to-source voltages of the SR MOSFET for layouts #1 and #2, respectively. It is noted that compared to layout #1, layout #2 with reduced loop inductance alleviates the oscillation of the drain-to-source voltage greatly, which results from the parasitic inductance and reverse recovery of the SR body diode.

Fig. 11 shows the measured efficiency comparison between these two different layouts at 1.3-V output. It is observed that at 20 A, the efficiency is improved from 84.1% to 86.7% (an improvement of 2.6%), and at 30 A, the efficiency is improved from

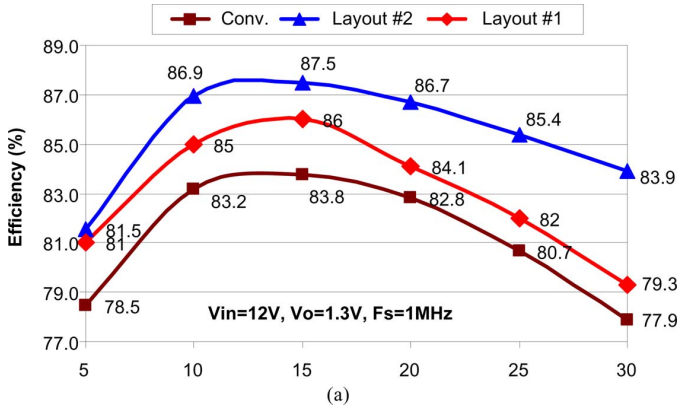

Fig. 11. Efficiency comparison: top: buck #2; mid: buck #1; and bottom: conventional voltage driver (Conv.)

79.3% to 83.9% (an improvement of 4.6%). Higher efficiency improvement is achieved when the load current increases. This is because the switching loop inductance causes stronger current holding effect in higher load current condition. It is also noted that both the layouts with the CSD achieve higher efficiency over the conventional voltage driver. In the test, the predictive gate drive UCC 27222 from Texas Instruments was used as the conventional gate driver.

V. Conclusion

The CSDs can alleviate the effect of the CSI to expedite the switching speed and reduce the switching loss. However, through analytical modeling on the CSDs, it is noticed that the switching loop inductance still causes the current holding effect on the CSDs. This will weaken the effectiveness of the CSDs of the switching loss reduction. Therefore, in a practical design of the CSDs, the switching loop inductance should also be minimized to improve the performance of the switching loss reduction. An improved layout was proposed to achieve minimum switching loop inductance compared to the original buck layout. A 65% reduction of the loop inductance is achieved. The experimental results verified the efficiency improvement.

References

[1] *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.1,* Design Guidelines, Sep. 2009.
[2] D. Maksimovic, "A MOS gate drive with resonant transitions," in *Proc. IEEE Power Electron. Spec. Conf.*, 1991, pp. 527–532.
[3] H. Fujita, "A resonant gate-drive circuit capable of high-frequency, and high-efficiency operation," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 962–969, Apr. 2010.
[4] G. Spiazzi, P. Mattavelli, and L. Rossetto, "Effects of parasitic components in high-frequency resonant drivers for synchronous rectification MOSFETs," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 2082–2092, Jul. 2008.
[5] Z. Zhang, E. Meyer, Y. F. Liu, and P. C. Sen, "A 1-MHz, 12-V ZVS non-isolated full-bridge VRM with gate energy recovery," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 624–636, Mar. 2010.
[6] Z. Zhang, W. Eberle, Y. F. Liu, and P. C. Sen, "A new hybrid gate drive scheme for buck voltage regulators," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 2498–2503.
[7] W. Eberle, Z. Zhang, Y. F. Liu, and P. C. Sen, "A current source gate driver achieving switching loss savings and gate energy recovery at

1-MHz," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 678–691, Mar. 2008.

[8] Z. Yang, S. Ye, and Y. F. Liu, "A new resonant gate drive circuit for synchronous buck converter," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1311–1320, Jul. 2007.

[9] Z. Zhang, W. Eberle, P. Lin, Y. F. Liu, and P. C. Sen, "A 1-MHz high efficiency 12 V buck voltage regulator with a new current-source gate driver," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2817–2827, Nov. 2008.

[10] W. Eberle, Z. Zhang, Y. F. Liu, and P. C. Sen, "A practical switching loss model for buck voltage regulators," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 700–713, Mar. 2009.

[11] Y. Ren, M. Xu, J. Zhou, and F. C. Lee, "Analytical loss model of power MOSFET," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 310–319, Mar. 2004.

[12] Y. Xiao, H. Shah, T. P. Chow, and R. J. Gutmann, "Analytical modeling, and experimental evaluation of interconnect parasitic inductance on MOSFET switching characteristics," in *Proc. IEEE Appl. Power Electron. Conf.*, 2004, vol. 1, pp. 516–521.

[13] J. Fu, Z. Zhang, Y. F. Liu, P. C. Sen, and L. Ge, "A new high efficiency current source driver with bipolar gate voltage," *IEEE Trans. Power Electron.*, to be published.

[14] X. Zhou, Z. Liang, and A. Huang, "A new resonant gate driver for switching loss reduction of high side switch in buck converter," in *Proc. IEEE Appl. Power Electron. Conf.*, 2010, pp. 1477–1481.

[15] D. A. Grant and J. Gowar, *Power MOSFET: Ttheory And Applications*. New York: Wiley- Interscience, Feb. 1989, pp. 97–143.

[16] F. Hirtenfelder, *Theory by Maxwell Solutions by Ansoft*. Pittsburgh, PA: Application Note, Ansoft Corporation, 2008.

[17] Z. Zhang, J. Fu, Y. F. Liu, and P. C. Sen, "Discontinuous-current-source drivers for high-frequency power MOSFETs," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1863–1876, Jul. 2010.

[18] Z. Zhang, W. Eberle, Z. Yang, Y. F. Liu, and P. C. Sen, "Optimal design of resonant gate driver for buck converter based on a new analytical loss model," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 653–666, Mar. 2008.