An Interleaving and Load Sharing Method for Multiphase LLC Converters

Zhiyuan Hu, Yajie Qiu, Yan-Fei Liu, and P. C. Sen
Department of Electrical and Computer Engineering
Queen's University, Kingston, Canada
zhiyuan.hu@queensu.ca, yajie.qiu@queensu.ca, yanfei.liu@queensu.ca, senp@queensu.ca

***Abstract*—Interleaving frequency-controlled LLC resonant converters will encounter load-sharing problem due to the tolerance of the resonant components. In this paper, full-wave and half-wave switch-controlled capacitors (SCCs) are used in LLC stages to solve this problem. By using resonant capacitance as a control variable, the output current can be modulated even when all the LLC stages are synchronized at the same switching frequency. A design procedure is developed. A 600W prototype is built to verify the feasibility.**

I. INTRODUCTION

Today's power converters are required to deliver more power and achieve high efficiency in a wide load range. These requirements are sometimes contradictive, because when a power supply is designed for a higher capacity, the light-load efficiency is likely to suffer. To solve this problem, interleaving and phase-shedding techniques can be employed, and they have the following advantages: (a) using the interleaving technique, the load capacity of a power supply can be expanded by adding parallel phases while the design of each phase can be optimized for a lower power level; (b) using the phase-shedding technique, at light load, unneeded phases can be shut down, thus the light-load efficiency can be improved; (c) in the heavy load condition, the multiple phases can split the total current, thus mitigate the I^2R loss; (d) the interleaving technique can reduce the ripple current in the output capacitor, thus reduce the required capacitor size.

The above discussed techniques and the benefits are promising to the popular LLC resonant topology [1-4], which has been widely adopted in flat-panel TVs, laptop adapters, server computers, and so on. However the key problem is the load sharing: when interleaved, all the LLC stages must operate at the same switching frequency for current ripple cancellation; whereas due to the components' tolerances, individual LLC stages may have different resonant frequencies, thus the output currents will be different. Simulation results in Section IV will show that the commonly seen component tolerances can cause drastic current imbalance.

Previous studies on multiphase LLCs all had limitations. The topologies in [5, 6] are multiphase LLCs but not interleaved. The studies in [7-10] did not consider the load sharing problem caused by to the component tolerances. The load sharing method in [11] needs an additional power stage to regulate the output voltage and does not work for more than two phases interleaved. The structure in [12] divides down the input voltage by the number of phases, therefore cannot expand the load capacity; and it also has difficulties with phase shedding. Similarly, the topology in [13] also has difficulties to realize phase shedding.

In this paper, a switch-controlled capacitor (SCC) [14] is used in each LLC stage (SCC-LLC) to modulate the resonant capacitance, thus the resonant frequency becomes a control variable. As a result, when all the phases are operating at the same switching frequency, individual phases will still have independent regulation. This advantage enables a simple structure for interleaving compared to those in [12, 13], thus load sharing and phase shedding are easy to implement. Also, the system's load capacity can be expanded by paralleling an arbitrary number of phases. In the following sections, Section II describes the improved driving schemes of SCC; Section III compares two candidate operation schemes of SCC-LLC; Section IV provides analysis and the design method of the preferred operation scheme; and Section V shows the experimental results.

II. THE IMPROVED DRIVING SCHEMES FOR FULL-WAVE AND HALF-WAVE SCCS

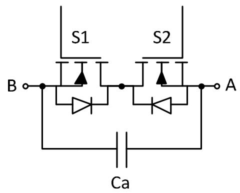
The concept of switch-controlled capacitor (SCC) was introduced in [14], in which the body diodes of the MOSFETs carry current for half of the switching period in the worst case. An improved driving scheme is proposed in this paper to prevent the MOSFET body diodes from carrying current, shown in Fig. 1 and Fig.2.

Fig. 1 shows the structure and waveforms of a full-wave SCC. The operation is described as follows: When a sinusoidal current, I_{AB}, is applied to a SCC, the current zero-crossing points are at angles $0, \pi, 2\pi \ldots$ by definition. For a positive half-cycle where the current flows from A to B, S_2 is turned on to prevent body diode from carrying current; the gating signal of S_1 is synchronized at $2n\pi$ ($n \in N$), and it turns off S_1 at angle $2n\pi+\alpha$, where $\pi/2<\alpha<\pi$. The current then flows from A to B via C_a and charges C_a until the angle $(2n+1)\pi$. At the angle $(2n+1)\pi$, the current reverses the direction, and begins to discharge C_a. After C_a is fully discharged, and the negative current is about to flow from B to A via S_1's body diode, S_1 is turned on again to prevent the body diode from carrying current. Then S_1 remains on until angle $(2n+2)\pi + \alpha$, which is α angle past the next sync point $(2n+2)\pi$. S_2 controls the negative half-cycle and has a symmetrical operation, except the sync points are at $(2n+1)\pi$. The equivalent capacitance of the full-wave SCC, C_{SC_FW}, is modulated by the angle α, given in (1) [14].

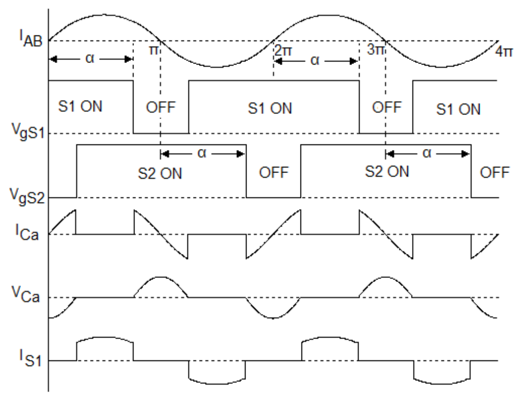
Fig. 2 shows the structure and waveforms of a half-wave SCC. The control scheme is similar to that of the full-wave SCC, except only a half wave can be modulated. The control angle α is from 0 to π. The equivalent capacitance of the half-wave SCC, C_{SC_HW}, is given in [15], and is rewritten in (2) after rearrangement.

$$C_{SC\_FW} = \frac{C_a}{2-(2\alpha - \sin 2\alpha)/\pi} \tag{1}$$

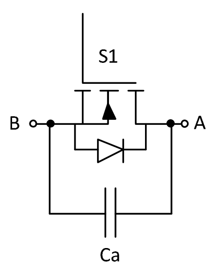
$$C_{SC\_HW} = \frac{2C_a}{2-(2\alpha - \sin 2\alpha)/\pi} \tag{2}$$



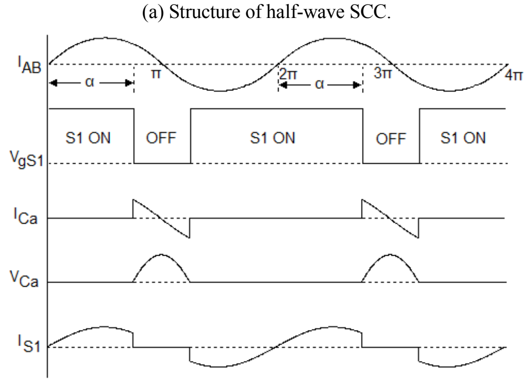
(a) Structure of full-wave SCC.



(b) Waveforms of full-wave SCC.
Figure 1 Structure and waveforms of full-wave SCC.



(a) Structure of half-wave SCC.



(b) Waveforms of half-wave SCC.
Figure 2 Structure and waveforms of half-wave SCC.

The full-wave SCC is more effective in modulating the equivalent capacitance, because the voltage of C_a is modulated in both half-cycles. However it requires isolated driving, which adds cost and takes more PCB area. On the contrary, the half-wave SCC uses only one MOSFET and does not require isolated driving; however the voltage of C_a is unipolar, thus the resonant current waveforms of the two half-cycles may be asymmetrical.

III. Constant Switching Frequency and Variable Switching Frequency SCC-LLCs

The proposed SCC-LLC is shown in Fig.3. A full-wave or a half-wave SCC is connected in series with the resonant tank in order to modulate the equivalent resonant capacitance, C_r, calculated in (3).

$$C_r = \frac{C_{SC} C_s}{C_{SC} + C_s} \tag{3}$$

The load sharing mechanism is described as follows: when the controller detects that one phase is driving more current than other phases, it slightly increases the control angle α of the corresponding phase, thus increasing the resonant capacitance C_r, and lowering the resonant frequency, and therefore reduces the output current until it reaches the balanced point.

All previous applications of SCC were operating at a constant switching frequency [15-20]; however, this is not necessary for the purpose of interleaving. The switching frequency can be either fixed or variable, as long as all the phases are operating at the same switching frequency. Therefore, there are two candidate operation schemes: (a) full-wave SCC with constant switching frequency; (b) half-wave SCC with variable switching frequency. In Scheme (a), the modulation of the entire gain range is accomplished by modulating the resonant frequency using a full-wave SCC. In Scheme (b), the output voltage is regulated by the switching frequency same as conventional LLCs, and a half-wave SCC is only used for load sharing. Because the component tolerances to be compensated are of small values, very little asymmetrical effect will be induced by the half-wave SCC. For completeness, there are also (c) full-wave SCC with variable switching frequency; and (d) half-wave SCC with constant switching frequency. However, full-wave SCC is an overkill for compensating the component tolerance only, and it adds to the cost; whereas half-wave SCC is not desirable to regulate the full output range due to its asymmetrical effect mentioned in Section II. Therefore, Scheme (c) and (d) are excluded.

The difference between Scheme (a) and (b) is the pure resonant frequency modulation (FrM) against primarily switching frequency modulation (FsM) supplemented by FrM. The following analysis compares the two approaches.

Using the Fundamental Harmonic Approximation (FHA) method, the gain of the LLC resonant tank can be expressed in (4), where L_p is the parallel inductance, K is the inductance ratio, L_p/L_r; R_L is the load resistance, N is the transformer turns ratio, ω_s is the switching frequency in radians, and ω_r is the resonant frequency in radians.

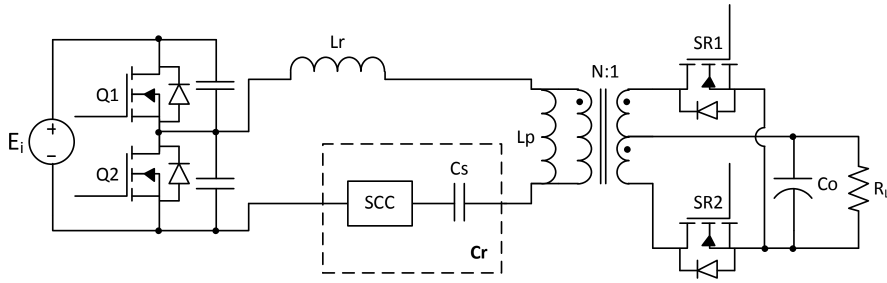


Figure 3 Topology of the proposed SCC-LLC.

$$M = \frac{K}{\sqrt{\left[\left(\frac{\omega_r}{\omega_s}\right)^2 - K - 1\right]^2 + \frac{\pi^4 \omega_s^2 L_p^2}{64 N^4 R_L^2}\left[\left(\frac{\omega_r}{\omega_s}\right)^2 - 1\right]^2}} \qquad (4)$$

For a given set of values of L_p, K, R_L and N, gain curves resulted from FrM and FsM are plotted using (4), respectively, shown in Fig. 4. In the plots, the variable resonant frequency is normalized at the switching frequency, and the variable switching frequency is normalized at the resonant frequency. It is illustrated that the FsM is able to achieve a higher peak gain within a narrower frequency variation range than FrM. The narrow frequency variation range of FsM indicates lower RMS current and thus higher efficiency. This phenomenon can be understood from the impedance point of view: the FsM modulates the impedance of all the resonant components; whereas the FrM only modulates the impedance of the resonant capacitance, thus is less effective.

Taking into consideration that the half-wave SCC also has lower cost and less conduction loss in the SCC MOSFET, it is apparent that FsM is the preferred control method when possible. Therefore, the half-wave SCC controlled LLC with variable switching frequency operation (*h*SCC-LLC) is a more advantageous solution than the full-wave SCC controlled LLC with constant switching frequency operation (*f*SCC-LLC), except when the constant switching frequency is a desired feature.

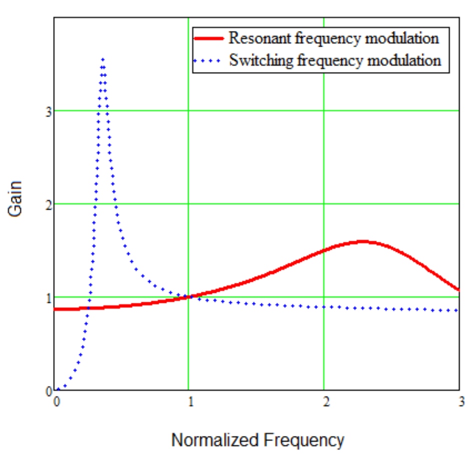


Figure 4 Comparison of switching frequency modulation and resonant frequency modulation.

IV. Analysis and Design Method of *h*SCC-LLC

The *h*SCC-LLC uses the switching frequency to regulate the output voltage, therefore the design procedure is the same as in conventional LLCs, which is available in many literatures [4, 21-23]. The extra work is to determine the SCC capacitor value C_a. This section studies the load sharing characteristics of *h*SCC-LLC, and then provides a design method of the half-wave SCC.

A. Load Sharing Characteristics of hSCC-LLC

Owing to the components' tolerances, the resonant tanks of the interleaved phases will slightly vary one from another, resulting in different output-current-versus-switching-frequency curves. A set of such curves are obtained from simulation and plotted in Fig. 5. In the simulation, *±7%* tolerances are assumed for inductors, and ±*5%* tolerances are assumed for capacitors. The simulated LLC converter has 300V-400V input and 12V output with a transformer turns ratio of *20:1*. C_s is *40nF*, L_r is *12µH*, and L_p is *86µH*. From the simulation results, the following properties are observed:

1. The output currents vary drastically when different tolerance values are applied. For example, at *160 kHz* switching frequency, the output current can range from *200A* to *0A*.

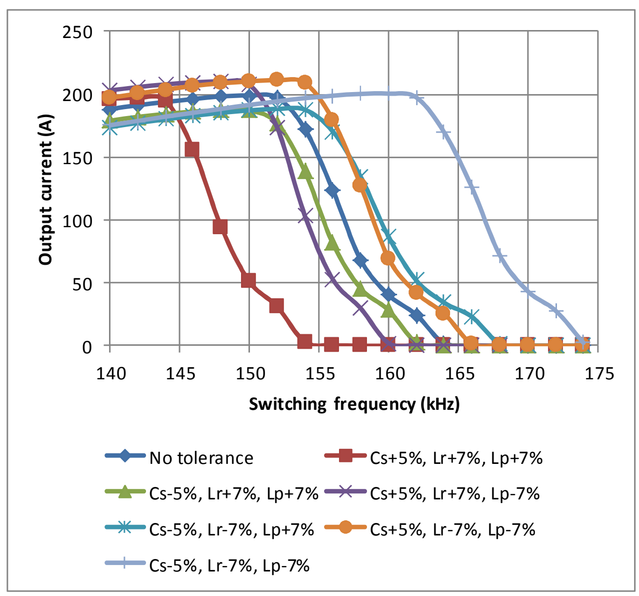


Figure 5 Output current VS. Switching frequency curves at different tolerances. Input voltage is 400V. Output voltage is 12V. Transformer turns ratio is 20:1.

2. Reduced resonant tank values cause higher resonant frequency, thus the output-current-versus-switching-frequency curve is shifted towards higher frequency. Therefore in an interleaved LLC converter, such a phase is a stronger phase, which provides more output current than designed. The worst-case condition is that all of L_p, L_r, and C_s are at their minimum values (C_s-5%, L_r-7%, L_p-7% in this example). Because SCC can only reduce the resonant capacitance value, it cannot reduce the output current of a stronger phase. Therefore, the strongest phase becomes the reference phase, and all other phases should increase their output currents to match it.

3. Increased resonant tank values cause lower resonant frequency, thus the output-current-versus-switching-frequency curve is shifted towards lower frequency. Such a LLC stage is a weaker phase in an interleaved LLC converter, which outputs less current than designed. SCC should be used in such phases to increase the output current and match the reference phase. The worst-case condition is that all of L_p, L_r, and C_s are at their maximum values (C_s+5%, L_r+7%, L_p+7% in this example).

4. The peak output current may be also changed by the component tolerances. The worst case happens when C_s is at the minimum value and L_p is at the maximum value (C_s-5%, L_r-7%, L_p+7% and C_s-5%, L_r+7%, L_p+7% in this example), where the peak output current is about *5%* below the *no tolerance* condition.

Simulations are also carried out for *300V* input condition and *18:1* turns ratio, respectively. Despite different frequency ranges and peak output currents, the above observed properties are the same.

Therefore, still referring to Fig. 5, the worst-case requirement for the SCC is to reduce the equivalent resonant capacitance of the weakest phase (the leftmost curve) so as to shift it to a higher frequency and match the strongest phase (the rightmost curve). The result is that both LLC phases have the same output current and operate at the same switching frequency range as the strongest phase.

Simulations are performed to find the required C_r that can compensate the worst-case tolerances and achieve load balance. C_r is expressed as a reduction from C_s. The result is shown in Fig. 6. The following characteristics are observed:

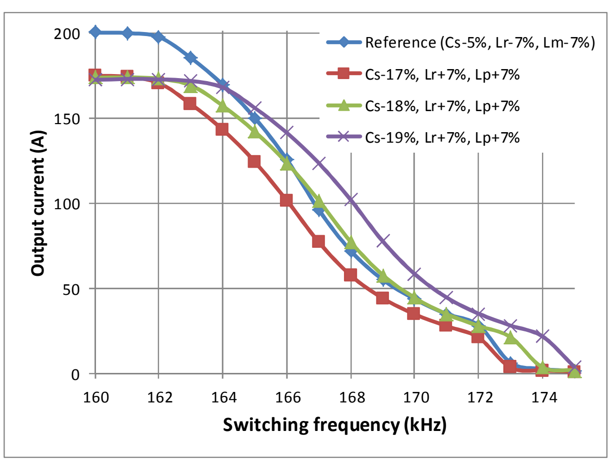


Figure 6 Output current VS. Switching frequency curves after compensation. Input voltage is 400V. Output voltage is 12V. Transformer turns ratio is 20:1.

1. A narrow reduction range of *17%* to *19%* from C_s is sufficient to achieve load balance. At light-medium load, a reduction between *17%* and *18%* is selected. At heavy load, a reduction between *18%* and *19%* is selected.

2. The peak output currents resulted from SCC compensation are about *14%* lower than the reference phase. This effect must be taken into consideration when design an interleaved LLC converter. Sufficient margin is needed in case of the worst-case tolerance.

The simulation is repeated for *300V* input condition and *18:1* turns ratio, respectively. The resulted C_r and the reduction percentage of peak output current are almost the same as *400V*, *20:1* turns ratio condition. Therefore, the worst-case for SCC modulation is independent from input condition and turns ratio.

The above studies identified the worst-case C_r to achieve load balance, and revealed that the peak output current will reduce as a result of SCC modulation. Mathematical methods are needed to assist the SCC design.

B. Derivation of Worst-case Resonant Capacitance

The output current can be expressed by the load resistance R_L, derived from (4), in (5).

$$R_L = \frac{\pi^2(\omega_r+\omega_s)(\omega_r-\omega_s)\omega_s L_p M}{8N^2\sqrt{\begin{aligned}&2\omega_r^2K\omega_s^2M^2+2\omega_r^2\omega_s^2M^2-\omega_r^4M^2\\&-\omega_s^4M^2-K^2\omega_s^4M^2-2K\omega_s^4M^2+K^2\omega_s^4\end{aligned}}} \tag{5}$$

Using a, b, and c to stand for the ratios of the actual component values and the ideal values of L_p, L_r, and C_s, respectively, then the inductance ratio becomes:

$$K=\frac{L_p}{L_r}=\frac{aL_{p0}}{bL_{r0}}=\frac{a}{b}K_0 \tag{6}$$

where subscript *0* stands for ideal values without tolerances.

And the resonant frequency becomes:

$$\omega_r=\frac{1}{\sqrt{L_rC_s}}=\frac{1}{\sqrt{bL_{r0}\cdot cC_{s0}}}=\frac{1}{\sqrt{bc}}\omega_{r0} \tag{7}$$

Substitute (6), (7), and $\omega_s=\omega_n\cdot\omega_{r0}$ into (5), then R_L can be expressed as a function of a, b, and c:

$$R_L(a,b,c)=\frac{\pi^2\omega_{r0}\omega_n aL_{p0}M\left(1-\omega_n^2bc\right)}{8N^2\sqrt{\begin{aligned}&2aK_0\omega_n^2M^2c-M^2-\omega_n^4M^2b^2c^2\\&+2\omega_n^2M^2bc-a^2K_0^2\omega_n^4M^2c^2\\&-2aK_0\omega_n^4M^2bc^2+a^2K_0^2\omega_n^4c^2\end{aligned}}} \tag{8}$$

where ω_n is the switching frequency normalized at resonant frequency ω_{r0}.

When properly compensated, the load resistance of the strongest phase and the weakest phase are equal, meaning that the output currents are equal. The equation is written in (9), where q is the ratio of the required C_r and C_{s0} of the weakest phase in order to match the load current of the strongest phase. As shown in Fig. 6, the required q value slightly varies in different load conditions; the minimum value of q, q_{min}, is the worst case for the SCC modulation.

$$R_L(a_{\min}, b_{\min}, c_{\min}) = R_L(a_{\max}, b_{\max}, q) \tag{9}$$

The expression of q is rather long and is inaccurate when predicting the minimum value, due to the inherent inaccuracy of the FHA. Instead, a visual assisted method is proposed to find an accurate estimation of q_{min}. It is described as follows:

Use (8) to plot curves of load resistances as a function of normalized switching frequency, shown in Fig. 7. The valley point of each curve is the minimum load resistance of the phase. The lower the minimum load resistance, the higher the peak output current. On the left-side of the valley point is the ZCS region which should be avoided. On the right-side of the valley point is the ZVS operation region, where all the interleaved LLC phases should match to the strongest phase.

Four curves are drawn in Fig. 7: the solid line is from the strongest phase (*reference*), $R_L(a_{min},b_{min},c_{min})$; the dash line is from the weakest phase, $R_L(a_{max},b_{max},c_{max})$; the dash-dot line is from the weakest phase after compensation, $R_L(a_{max},b_{max},q)$. By varying q, *0.81* is found to be the *best match* of the right-side curves, which equals to a *-19%* reduction from C_{s0}, in accordance with that suggested by Fig. 6. Because the variation range of q is only a few percent as is shown in Fig. 6, the *best match* is also a good estimation of the q_{min}. The dot line is resulted from $q=0.67$, which is a mathematically valid solution from (9); however the resulted curve largely deviates from the *reference* curve; therefore it is invalid in practice. The visual assisted method can exclude these otherwise mathematically correct solutions and prevents q_{min} from being unnecessarily small, and thus can achieve an optimal design.

The peak output current reduction in percentage suggested by Fig. 7 are also in good accordance with simulation, though the absolute values are not accurate. The *best match* curve's peak output current is *14%* less than that of the *reference*

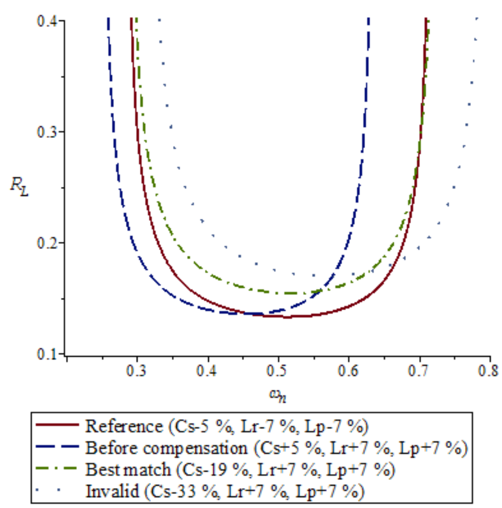


Figure 7 Load resistance VS. Normalized switching frequency. Plotted using (8). Input voltage is 400V. Output voltage is 12V. Turns ratio is 20:1.

curve, which is the exact percentage suggested by Fig. 6. Repeating the calculation at *300V* input condition yields the same conclusion.

Therefore, the visual assisted method can accurately predict the value of q_{min} and the percentage of peak output current reduction. The peak current reduction should be considered when designing the LLC resonant tank, and the q_{min} is used to determine the SCC capacitor value, C_a, as discussed below.

C. Design of half-wave SCC Capacitor

The SCC is in series with C_s, therefore the equivalent resonant capacitance is derived by substituting (2) into (3):

$$C_r = \frac{2C_a C_s \pi}{2C_a\pi + 2C_s\pi - 2C_s\alpha + C_s \sin(2\alpha)} \tag{10}$$

The control angle α is from 0 to π, which regulates the resonant capacitance from $C_{r,min}$ to $C_{r,max}$. $C_{r,max}$ occurs at $\alpha=\pi$ and $C_s=C_{s0}{\cdot}c_{max}$, where the SCC MOSFET is always turned on, thus $C_{r,max}=C_{s0}{\cdot}c_{max}$. $C_{r,min}$ occurs at $\alpha=0$. It must not be larger than $q_{min}C_{s0}$ so that it has sufficient capacity to balance load current in the worst case. Setting $C_{r,min}$ smaller than $q_{min}C_{s0}$ is acceptable, but the peak voltage of C_a will be higher, and thus a higher voltage rating and $R_{ds(on)}$ of the SCC MOSFET. Therefore, the optimal design is to achieve $C_{r,min}= q_{min}C_{s0}$ when $\alpha=0$ and $C_s=C_{s0}{\cdot}c_{max}$.

Substituting $C_r=q_{min}C_{s0}$, $\alpha=0$, and $C_s= C_{s0}{\cdot}c_{max}$ into (10) gives (11):

$$q_{\min} C_{s0} = \frac{C_a C_{s0} c_{\max}}{C_a + C_{s0} c_{\max}} \tag{11}$$

Then solving (11) gives the expression of C_a:

$$C_{a0} = C_{s0} \frac{c_{\max} q_{\min}}{c_{\max} - q_{\min}} \tag{12}$$

where C_{a0} stands for the ideal value of C_a. Considering C_a also has tolerance, the implemented C_a value should be:

$$C_a \le \frac{C_{a0}}{e_{\max}} \tag{13}$$

where e_{max} is the maximum ratio of actual and ideal C_a due to the tolerance.

D. Design Procedure of hSCC-LLC

The design method discussed in this section is summarized as follows.

1. Design LLC stages using conventional methods. The design should leave sufficient margin considering that the SCC modulation will reduce the peak output current. Then identify the tolerances of the resonant components.

2. Use (8) to plot load resistance curves of the strongest phase and the weakest phase, and tune q of the weakest phase to match the strongest phase in the ZVS region. The resultant q is considered to be q_{min}. The percentage of peak output current reduction can be also measured from the plots.

3. Use (12) and (13) to determine the C_a value.

V. EXPERIMENTAL RESULTS

A 600W two-phase interleaved *h*SCC-LLC is implemented to verify the feasibility and the advantages of the proposed method. The system block diagram is shown in Fig. 8. The parameters are in Table 1.

Table 1 Prototype parameters

Switching frequency	200kHz
Input Voltage	400V nominal/300V minimum
Output Voltage	12V
Output Power	300W × 2
Transformer Turns Ratio	20:1, Center tapped
Magnetizing Inductance	87μH(Phase1) 85μH(Phase2)
Resonant Inductance	12μH(Phase1) 14μH(Phase2)
Series Capacitors	36nF±5%
SCC Capacitors	30nF±3% or 155nF±5%
Output Capacitance	1790μF (100μF× 8, 330μF× 3)
Half-bridge MOSFET	IPB60R190C6
SCC MOSFET	BSC060N10NS3G(100V,6mΩ)
SR MOSFET	BSC011N03LS

The resonant inductances are implemented with the transformers' leakage and are intentionally made non-identical in order to test the load sharing performance. Because Phase 1's inductances are made smaller, it is the stronger phase of the two; therefore only Phase 2 needs a half-wave SCC to modulate the output current to match Phase 1. Two values of SCC capacitors are tested in the circuit in order to show comparison of the asymmetrical effect and the peak SCC voltage. The two LLC phases have a 90˚ phase shift for ripple cancellation.

A Microchip DSC dsPIC33FJ32GS606 is used to implement the digital controller. The SCC's PWM is synchronized with the primary current's zero-crossing points using the External PWM Reset (XPRES) function, which resets the digital PWM once it receives a signal from the zero-crossing detection circuit. A small logic circuit is designed to turn on the SCC MOSFET when the SCC voltage returns to zero.

Fig. 9 shows the operation of the half-wave SCC. The SCC MOSFET is turned on as soon as the SCC voltage returns to zero in order to minimize the conduction loss. The SCC MOSFET is turned on and off at ZVS conditions, therefore the switching loss is the minimum as well.

Fig. 10 shows waveforms of a comparable 600W single-phase LLC converter at 50A load, with identical output capacitance that is used in the prototype *h*SCC-LLC. The output voltage ripple is measured 500mV peak to peak.

Fig. 11 shows waveforms of the *h*SCC-LLC at 50A load. The SCC capacitance is 30nF. The output voltage ripple is reduced to 210mV peak to peak. The output currents of the two phases are balanced even though the resonant tanks are intentionally made different. It is noticeable that the output current of the two half-cycles in Phase 2 are slightly asymmetrical due to the half-wave SCC modulation.

Fig. 12 shows waveforms of the *h*SCC-LLC at 50A load, with the SCC capacitance changed to 155nF. It is observed that when C_a is larger, it has to carry current for a longer period to achieve the same equivalent resonant capacitance, and this way mitigates the asymmetrical effect of the output current. Thus the resultant output voltage ripple is further reduced to 130mV peak to peak. The larger C_a also results in lower peak SCC voltage, thus lowers the voltage-rating of SCC MOSFETs, which reduces the conduction loss. Therefore, for optimal performance, the SCC capacitance should be just small enough to provide sufficient modulation, but be as large as possible.

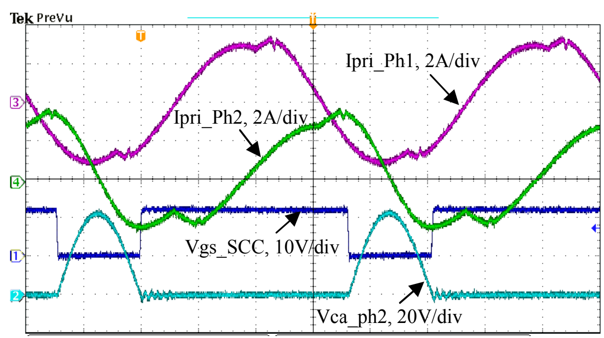


Figure 9 Operation of half-wave SCC.

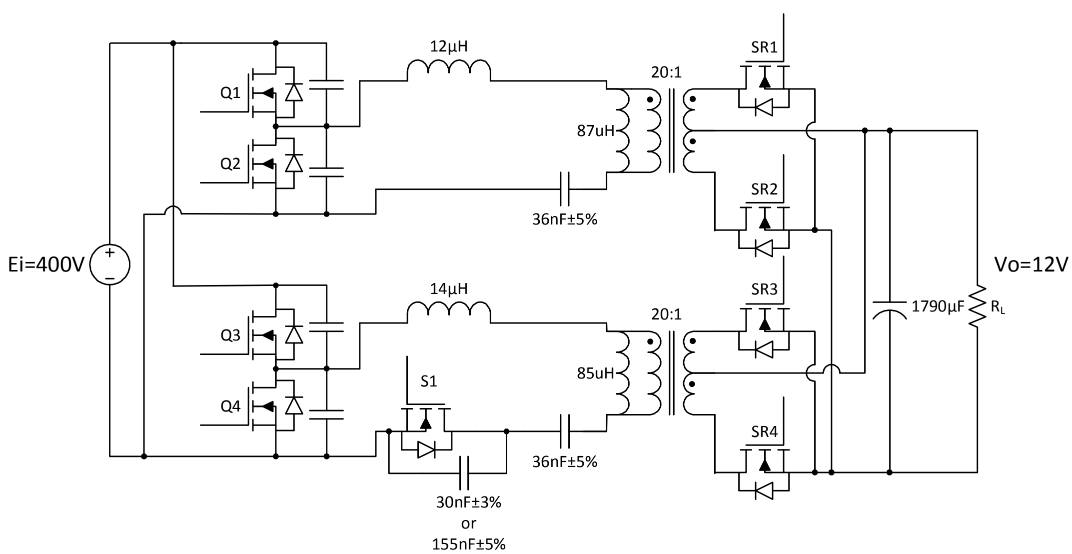


Figure 8 The implemented two-phase interleaved *h*SCC-LLC.

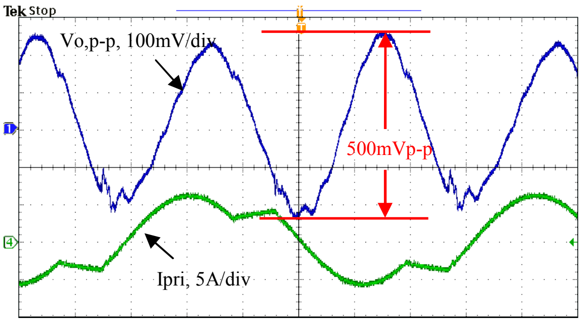


Figure 10 Output voltage ripple of single phase LLC. I_o=50A, C_o=1790µF.

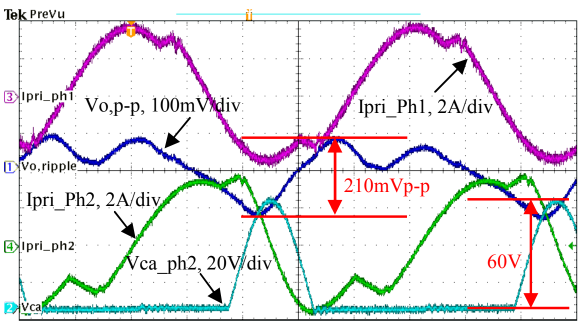


Figure 11 Output voltage ripple of two-phase interleaved *h*SCC-LLC. Io=50A, C_o=1790µF, C_a=30nF.

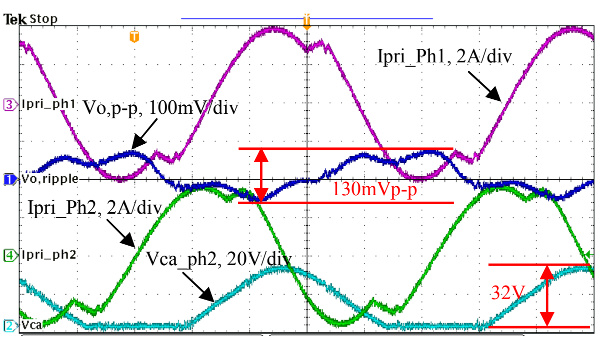


Figure 12 Output voltage ripple of two-phase interleaved *h*SCC-LLC. Io=50A, C_o=1790µF, C_a=155nF.

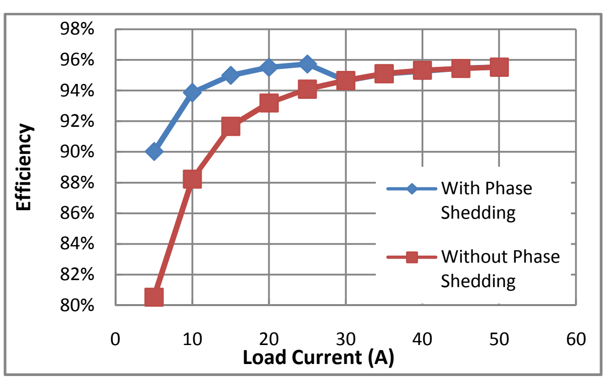


Figure 13 Efficiency comparison, with and without phase shedding.

Fig. 13 shows the efficiency improvement using the phase-shedding technique in the proposed *h*SCC-LLC. The heavy load efficiency is above 95.5%, and the 5A (10%) load efficiency is improved from 81% to 90%.

VI. Conclusion

A switch-controlled capacitor (SCC) modulated multiphase LLC converter (SCC-LLC) is proposed in this paper to achieve interleaving, load sharing and phase shedding. The benefits include expandable load capacity, reduced output current ripple, and higher light-load efficiency. Analysis reveals that the half-wave SCC-LLC with variable switching frequency (*h*SCC-LLC) is more advantageous than the full-wave SCC-LLC with constant switching frequency (*f*SCC-LLC). The load sharing characteristic of *h*SCC-LLC is further studied, and a visual assisted method is proposed to determine the optimal SCC capacitance value. A two-phase interleaved *h*SCC-LLC prototype is built and shows good performances in load sharing, current ripple cancellation and improving light-load efficiency.

References

[1] B. Yang, F. C. Lee, A. J. Zhang, and G. Huang, "LLC resonant converter for front end DC/DC conversion," in *Proc. Appl. Power Electron. Conf. and Expo.(APEC '02)*, 2002, pp. 1108-1112 vol.2.

[2] Y. Zhang, D. Xu, M. Chen, Y. Han, and Z. Du, "LLC resonant converter for 48 V to 0.9 V VRM," in *Proc. Power Electron. Specialists Conf. (PESC '04)*, 2004, pp. 1848-1854 Vol.3.

[3] S. De Simone, C. Adragna, C. Spini, and G. Gattavari, "Design-oriented steady-state analysis of LLC resonant converters based on FHA," in *Int. Symp. Power Electron., Elect. Drives, Autom., Motion (SPEEDAM '06)*, 2006, pp. 200-207.

[4] B. Lu, W. Liu, Y. Liang, F. C. Lee, and J. D. van Wyk, "Optimal design methodology for LLC resonant converter," in *Proc. Appl. Power Electron. Conf. and Expo.(APEC '06)*, 2006, p. 6 pp.

[5] E.-S. Kim, K.-H. Yoon, S. Phum, S. Meas, J.-S. Won, S.-J. Oh, and Y.-S. Bae, "Operation characteristics of two-stage DC/DC converter for photovoltaic system," in *Proc. Appl. Power Electron. Conf. and Expo. (APEC '12)*, 2012, pp. 681-685.

[6] E.-S. Kim, Y.-J. No, S.-M. Lee, B.-G. Chung, J.-S. Lee, M.-S. Park, and D.-Y. Huh, "A low profile LLC resonant converter using novel planar transformer," in *Proc. Appl. Power Electron. Conf. and Expo. (APEC '12)*, 2012, pp. 1307-1312.

[7] T. Jin and K. Smedley, "Multiphase LLC Series Resonant Converter for Microprocessor Voltage Regulation," in *Proc. Ind. Applicat. Conf. (IAS '06)*, 2006, pp. 2136-2143.

[8] K.-H. Yi, B.-C. Kim, and G.-W. Moon, "A simple and novel two phase interleaved LLC series resonant converter employing a phase of the resonant capacitor," in *Proc. Energy Convers. Congr. and Expo. (ECCE'09)*, 2009, pp. 754-757.

[9] B.-R. Lin, W.-R. Yang, J.-J. Chen, C.-L. Huang, and M.-H. Yu, "Interleaved LLC series converter with output voltage doubler," in *Proc. Int. Power Electron. Conf. (IPEC '10)*, 2010, pp. 92-98.

[10] M. Kim, "Two-phase interleaved LLC resonant converter with phase shedding control," in *Proc. Int. Power Electron. Conf. (IPEC '10)*, 2010, pp. 1642-1645.

[11] H. Figge, T. Grote, N. Froehleke, J. Boecker, and P. Ide, "Paralleling of LLC resonant converters using frequency controlled current balancing," in *Proc. Power Electron. Specialists Conf. (PESC '08)*, 2008, pp. 1080-1085.

[12] B.-C. Kim, K.-B. Park, C.-E. Kim, and G.-W. Moon, "Load sharing characteristic of two-phase interleaved LLC resonant converter with parallel and series input structure," in *Proc. Energy Convers. Congr. and Expo. (ECCE'09)*, 2009, pp. 750-753.

[13] E. Orietti, P. Mattavelli, G. Spiazzi, C. Adragna, and G. Gattavari, "Current sharing in three-phase LLC interleaved resonant

converter," in *Proc. Energy Convers. Congr. and Expo. (ECCE'09)*, 2009, pp. 1145-1152.

[14] W.-J. Gu and K. Harada, "A new method to regulate resonant converters," *IEEE Trans. Power Electron.,* vol. 3, pp. 430-439, 1988.

[15] Y.-T. Chen, W.-M. Lin, and Y.-H. Liu, "Analysis and design of a dimmable electronic ballast controlled by a switch-controlled capacitor," *IEEE Trans. Ind. Electron.,* vol. 52, pp. 1564-1572, 2005.

[16] W. J. Gu and K. Harada, "A circuit model for the class E resonant DC-DC converter regulated at a fixed switching frequency," *IEEE Trans. Power Electron.,* vol. 7, pp. 99-110, 1992.

[17] J.-H. Cheng, A. F. Witulski, and J. L. Vollin, "Dynamic analysis of the Class-D converter at fixed frequency using amplitude and phase modulation," in *Proc. Power Electron. Specialists Conf. (PESC '98)*, 1998, pp. 387-393 vol.1.

[18] J.-H. Cheng, A. F. Witulski, and J. L. Vollin, "A generalized DC model and low-frequency dynamic analysis for the Class-D converter at fixed frequency," *IEEE Trans. Power Electron.,* vol. 15, pp. 1212-1220, 2000.

[19] L. Huber and M. M. Jovanoviae, "Evaluation of AC VRM topologies for high-frequency power distribution systems," in *Proc. Appl. Power Electron. Conf. and Expo.(APEC '01)*, 2001, pp. 160-166 vol.1.

[20] H.-J. Chiu and S.-J. Cheng, "Single-Stage Voltage Source Charge-Pump Electronic Ballast With Switched-Capacitor Dimmer for Multiple Fluorescent Lamps," *IEEE Trans. Ind. Electron.,* vol. 54, pp. 2915-2918, 2007.

[21] D. Fu, B. Lu, and F. C. Lee, "1MHz High Efficiency LLC Resonant Converters with Synchronous Rectifier," in *Proc. Power Electron. Specialists Conf. (PESC '07)*, 2007, pp. 2404-2410.

[22] C. Adragna, S. De Simone, and C. Spini, "A design methodology for LLC resonant converters based on inspection of resonant tank currents," in *Proc. Appl. Power Electron. Conf. and Expo.(APEC '08)*, 2008, pp. 1361-1367.

[23] X. Fang, H. Hu, J. Shen, and I. Batarseh, "An optimal design of the LLC resonant converter based on peak gain estimation," in *Proc. Appl. Power Electron. Conf. and Expo. (APEC '12)*, 2012, pp. 1286-1291.