Double Integral Sliding Mode Control of Paralleled DC/DC Converters

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***Abstract*—The use of dc-dc converters connected in parallel is a suitable way to solve the technological problems that arise in large-capability power supply systems. This paper presents a new approach to parallel converters using double integral sliding mode control. This approach could alleviating the steady-state regulation error and enhancing dynamic current-sharing property by increasing the order of the proportional integral sliding mode (ISM) controllers using an additional integral term. Theoretical analysis and simulation results are provided for verification.**

***Index Terms*—Paralleled DC/DC Converters, Integral Sliding Mode(ISM) Control, Double-integral sliding mode (DISM), Current-sharing**

I. Introduction

Paralleling of power converters has become a popular approach to construction power supplies for high-current high-power applications, with high degree of flexibility, maintainability, reliability and ease of expansion. Currently, the parallel DC / DC converters are widely used in motor drive, the computer system, communications equipment and other industrial applications[1-3]. For the effectiveness of the parallel system the control must ensure both the equal sharing of the load current among the converters and the regulation of the output voltage. In order to achieve current sharing between the converters, this paper uses a master-slave current sharing method, which ensures that all of the slave modules follow the reference current of the master[4-5].

Dc-dc converters are non-linear in nature. And sliding mode controller is a kind of non-linear controller which was introduced for controlling variable structure systems. Its major advantages are guaranteed stability and robustness against parameter, line, and load uncertainties. Various studies in the application of sliding-mode control for paralleled dc-dc converters have been reported in the past several decades[6-10].

The main feature of the sliding mode is the robustness that the system acquires against disturbances in the load and in the input voltage[11]. And the integral sliding mode(ISM) control strategy could get a good dynamic response[12], but does not effectively eliminate the steady state error which is due to the imperfect steady-state error correction method of the PWM-based sliding-mode controller[13].

This paper explores the possibility of alleviating the steady-state regulation error by increasing the order of the integral sliding mode controllers using an additional integral term.

II. Paralleled Buck Converter Current-Sharing Based on Double Integral Sliding Mode Control

A. Proposed Solution

Direct SM controllers are enforced to track a desired sliding surface to the equilibrium state. Since SM control can achieve order reduction, it is typically sufficient to have an SM controller of $n-1$ th order for achieving stable control of an n n th order converter.

And it explains why the steady-state errors are presents in the equivalent control. This paper will introduced an additional double-integral term of the state variables ($\int\left(\int x_i dt\right)dt$) to correct the error of the steady-error. And the instantaneous state variable's trajectory can be represented by

$$S=\sum_{i=1}^{n-1}\alpha_i x_i+\alpha_n\int\sum_{i=1}^{n-1}x_i dt+\alpha_{n+1}\iint\sum_{i=1}^{n-1}x_i dtdt\ . \quad (1)$$

And its time differentiation is represented by

$$\dot{S}=\sum_{i=1}^{n-1}\alpha_i\dot{x}_i+\alpha_n\sum_{i=1}^{n-1}x_i+\alpha_{n+1}\int\sum_{i=1}^{n-1}x_i dt\ . \quad (2)$$

And the equivalent control u_{eq} is a function of the state variables $\dot{x}_i$ 、 x_i ,and $\int x_i dt$. And the term $\int x_i dt$ could correcting the steady-state errors.

So introduced an additional double-integral term of the state variables easily resolves the problem of steady-state errors in integral sliding-mode controlled converters.

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B. Control Design Process Based on the Double Integral Sliding Mode Control

To verify the feasibility of the control strategy ,a two cell paralleled buck converter under the Master/Slave current-sharing configuration was constructed and analyzed.

And the paralleled buck converter's state equation in a complete cycle can be written as:

$$\begin{cases} \dfrac{di_{L_j}}{dt} = -\dfrac{1}{L_j} v_o + \dfrac{1}{L_j} v_i \times u & j = 1,2 \\ \dfrac{dv_o}{dt} = \dfrac{1}{C_o} \sum_{k=1}^{n} i_k - \dfrac{1}{R_L C_o} v_o & C_o = \sum_{k=1}^{n} C_j \end{cases} . \quad (3)$$

Where u is the system's control vector which represents the logic state of power switch. Also L_j , C_j ,and R_L denote the inductance, capacitance, and instantaneous load resistance respectively; i_{L_j} , i_C , v_o ,and v_i denote the inductor currents, capacitor currents, output voltages, and input voltage.

The paralleled buck converter use the switching function $u = \frac{1}{2}(1 + \mathrm{Sign}(S))$ and the sliding surface

$$S_j = \alpha_1 x_1 + \alpha_2 x_2 + \alpha_3 x_3 + \alpha_4 x_4 \quad j = 1,2 . \quad (4)$$

Where α_1 、 α_2 、 α_3 and α_4 represent the desired sliding coefficients.

For the DISM voltage controlled paralleled buck converter, the controlled state variables are the current error x_1 ,the voltage error x_2 ,the integral of the current and the voltage errors x_3 ,and the double integral of the current and the voltage errors x_4 ,which are expressed as

$$\begin{cases} x_1 = i_{ref} - i_{Lj} \\ x_2 = V_{ref} - \beta v_o \\ x_3 = \int (x_1 + x_2) dt \\ x_4 = \iint (x_1 + x_2) dt dt \end{cases} \quad j = 1,2 \quad . \quad (5)$$

Where

$$i_{ref} = K(V_{ref} - \beta v_o) \quad (6)$$

and K is the amplified gain of the voltage error. substituting the paralleled buck converter's behavioral models under CCM into the time differentiation of (5) gives the dynamical model of the proposed system as

$$\begin{cases} \dot{x}_1 = \dfrac{d(i_{ref} - i_{Lj})}{dt} = -\dfrac{\beta K}{C} i_c + \dfrac{v_o - v_i u}{L_j} \\ \dot{x}_2 = \dfrac{d(V_{ref} - \beta v_o)}{dt} = -\dfrac{\beta}{C} i_c & j = 1,2 \\ \dot{x}_3 = x_1 + x_2 \\ \dot{x}_4 = \int (x_1 + x_2) dt \end{cases} . \quad (7)$$

By solving $\dot{S} = 0$,the equivalent control u_{eq} could be expressed as

$$\begin{aligned} u_{eq} = & -\frac{\beta L_j}{C} \left(\frac{\alpha_2}{\alpha_1} + K \right) \frac{i_c}{v_i} \\ & + \frac{v_o}{v_i} + \frac{\alpha_3 L_j}{\alpha_1 v_i} \left[V_{ref} - \beta v_o \right] \\ & + \frac{\alpha_3 L_j}{\alpha_1 v_i} \left[K \left(V_{ref} - \beta v_o \right) - i_{Lj} \right] \\ & + \frac{\alpha_4 L_j}{\alpha_1 v_i} \int \left(V_{ref} - \beta v_o \right) dt \\ & + \frac{\alpha_4 L_j}{\alpha_1 v_i} \int \left[K \left(V_{ref} - \beta v_o \right) - i_{Lj} \right] dt \end{aligned} \quad (8)$$

where u_{eq} is continuous and bounded between 0 and 1.

In PWM form, the proposed DISM voltage controller for the paralleled buck converter inherits the expression

$$\begin{cases} v_c = -K_3 i_c + G_s v_o \\ \quad + K_1 \left[(K+1) \left(V_{ref} - \beta v_o \right) - i_{Lj} \right] \\ \quad + K_2 \int \left[(K+1) \left(V_{ref} - \beta v_o \right) - i_{Lj} \right] dt & j = 1,2 \\ v_{ramp} = G_s v_i \end{cases} \quad (9)$$

where $K_1 = G_s \frac{\alpha_3}{\alpha_1} L_j$; $K_2 = G_s \frac{\alpha_4}{\alpha_1} L_j$; and

$$K_3 = G_s \frac{\beta L_j}{C} \left(\frac{\alpha_2}{\alpha_1} + K \right) \quad (10)$$

are the fixed gain parameters in the propose controller. Figure 1 shows a schematic diagram of the derived PWM-based DISM voltage controller for the paralleled buck converter.

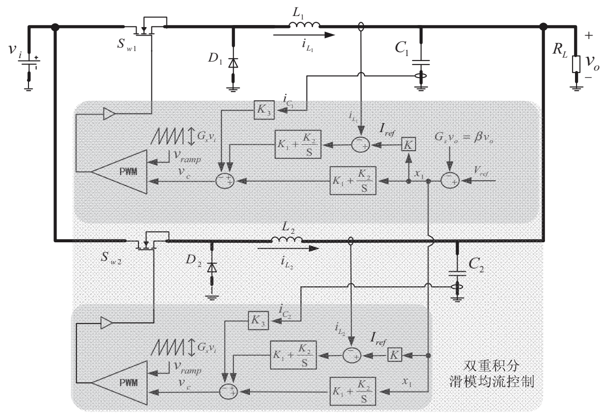


Figure 1. schematic diagram of the derived PWM-based DISM voltage controller for the paralleled buck converter.

Description	Parameter	Nominal value
Input voltage	v_i	12V
Output voltage	v_o	2.4V
capacitance	C	100μF
inductance	$L_1 = L_2$	10μH
Switching frequency	f_s	400K
Minimum load resistance	$R_{L(min)}$	0.3Ω
Maximum load resistance	$R_{L(max)}$	0.6Ω

TABLE I. SPECIFICATION OF THE PARALLELED BUCK CONVERTER

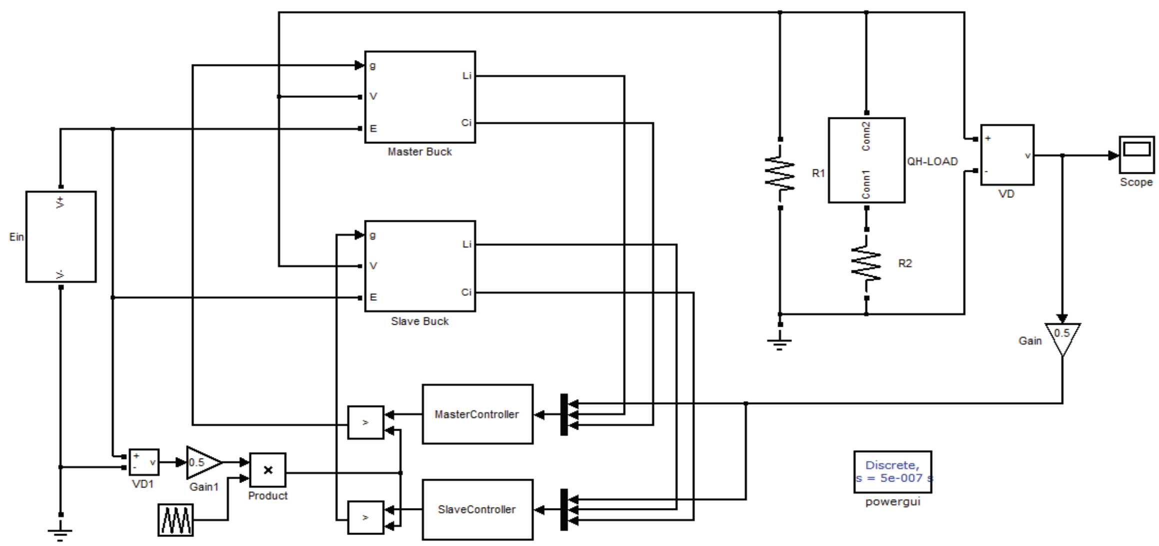
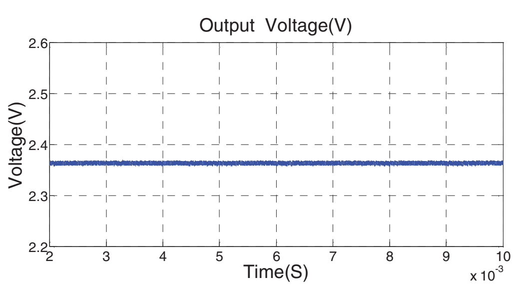
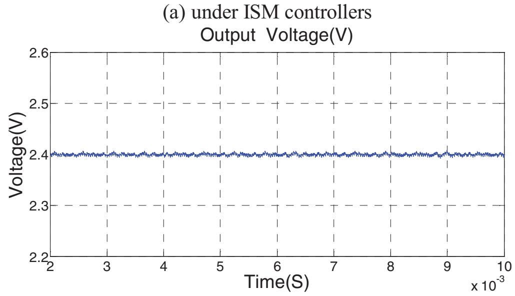


Figure 2. The Matlab simulation model of the paralleled buck converter under PWM-based DISM voltage controller

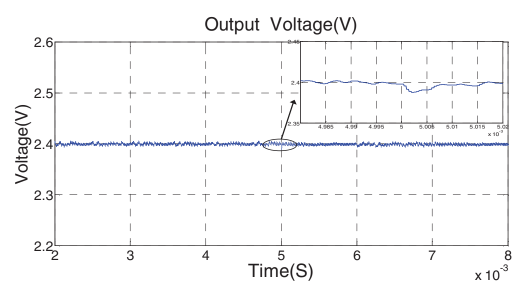


(a) under ISM controllers

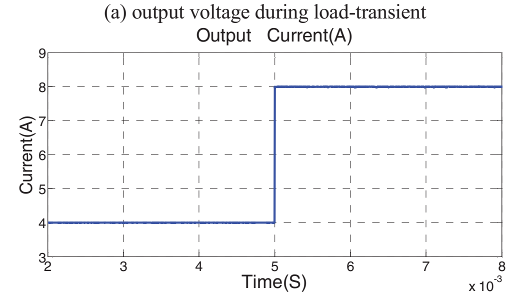


(b) under DISM controllers

Figure 3. The steady-state output voltage waveforms of the paralleled buck converter under ISM and DISM controllers.



(a) output voltage during load-transient



(b) output current during load-transient

Figure 4. The output voltage and current waveforms of the paralleled buck converter under DISM controllers during load-transient

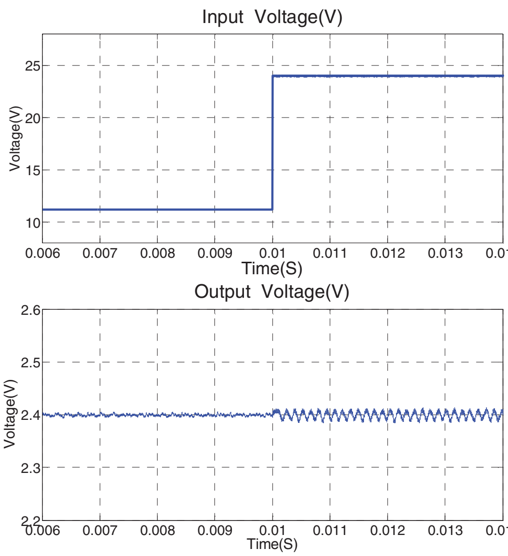
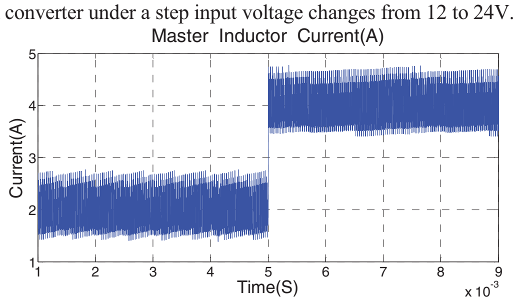
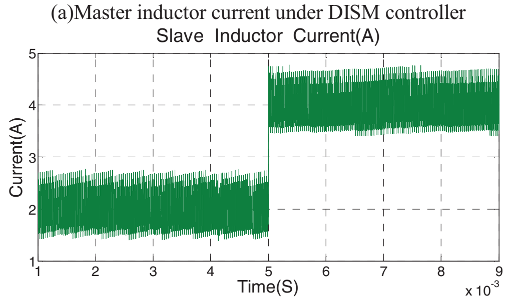


Figure 5. The steady-state output voltage waveforms of the paralleled buck converter under a step input voltage changes from 12 to 24V.



(a)Master inductor current under DISM controller



(b)Slave inductor current under DISM controller

Figure 6. The master and slave inductor currents waveforms against disturbances in the load.

III. SIMULATION RESULTS AND ANALYSIS

This paper is verified alleviating the steady-state regulation error and enhancing dynamic current-sharing property of the DISM controller through Matlab/Simulink simulation. The specification of the paralleled buck converter is given in Table I.

The Matlab simulation model of the paralleled buck converter under PWM-based DISM voltage controller has been shown in Figure 2.

And Figure 3 represents the steady-state output voltage waveforms of the paralleled buck converter under ISM and DISM controllers. Figure 3(a) shows that the paralleled buck converter output voltage contains a significant level of steady-state error of around 30 mV under ISM controller. However, the steady-state error is not present in the converter under DISM controller[see Figure 3(b)].

Figure 4 represents the output voltage and current waveforms of the paralleled buck converter under DISM controllers during load-transient. The simulation result demonstrate that the controller has a robust response during load-transient. And Figure 5 shows the output voltage waveforms of the paralleled buck converter operate under a step input voltage changes from 12 to 24V. It is not usually finding the steady-state output voltage is very stable with little oscillation. And the simulation results demonstrate that the robustness against disturbances in the input voltage. And the Figure 6 shows that the master and slave inductor currents under a step load change from 0.6 to 0.3Ω. And it is worth mentioning that the inductor currents of the slave module track the corresponding signal of the master well.

IV. SUMMARY AND CONCLUSION

This paper presents using double integral sliding mode(DISM) control parallel dc/dc converters to eliminate the steady-state output voltage error. And the simulation results have been shown that introduced an additional double-integral term of the state variables easily alleviating the steady-state regulation error and enhancing dynamic current-sharing property. And this paper has also shown the controller is robust against disturbances in the load and in the input voltage. Although this paper was evaluated with a parallel buck converter comprising two modules, it should be noted that the approach could be applied to system with arbitrary modules.

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