Improved Hybrid Rectifier for 1-MHz LLC-Based Universal AC-DC Adapter

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***Abstract*— This paper proposes a 1-MHz single stage LLC converter with improved hybrid full bridge / voltage doubler rectifier for laptop power adapter. Using single stage LLC instead of the two stage configuration is expected to reduce both the size and loss of the existing commercial products. For universal AC input, the hybrid full bridge / voltage doubler rectifier is desired. At 220 V AC input condition, the rectifier operates in full bridge mode, while at 110 V AC input, it operates as voltage doubler rectifier. With this mode switcher, the LLC converter resonant tank design only takes consideration of 220 V AC input case, such that the required operational input voltage range is reduced, and the efficiency of the LLC converter could be optimized. In this paper, two configurations of the improved hybrid full bridge / voltage doubler rectifiers are proposed with reduced cost and improved efficiency. Besides, for the LLC stage, a large magnetizing inductor could be used to significantly reduce the circulating current. To verify the effectiveness of the proposed hybrid full bridge / voltage doubler rectifier and the design of LLC converter, analysis will be carefully explained towards the rectifier and the LLC parameter design in this digest. A 65W prototype is built to demonstrate the feasibility.**

Keywords*— *LLC; voltage doubler; hybrid rectifier; power adapter;

I. INTRODUCTION

The demand remains ever increasing for AC-DC power adapters with high efficiency and high power density, especially under the background that the laptops are more affordable and portable today [1]-[5]. Compared with Flyback converter, LLC topology is gaining favor due to the proved higher efficiency [1]. Earlier studies of the LLC-based power adapter focuses on 90 W – 130 W power design [2], [3], in which two-stage configuration [4], [5] is prevailing to satisfy both Power Factor Correction (PFC) and the DC-DC conversion requirements. Thanks to the improved semiconductor fabrication process, CPUs nowadays consume less power, and the design of the new power adapters could be derated to 45 W – 65 W. Within such power range, power factor is not a mandatory requirement anymore, thus the PFC stage could be removed. Both the size and the loss of the adapter are expected to reduce with the single stage LLC converter.

A special fact about the laptop AC-DC adapter is that the converter needs to be designed as universal AC input adapted. Conventionally, full bridge (FB) diode rectifier with a reasonable DC link capacitor value is used as the rectification stage between the grid and the LLC converter. However, in order to operate from 90 V AC to 264 V AC, it requires very high DC voltage gain for the LLC converter, and such design will degrade the efficiency. To reduce the required operational input voltage range, the hybrid full bridge and voltage doubler (FB-VD) rectifier comes into sight (shown in Fig. 1). The basic idea is to use the full bridge rectifier for 220 V AC, while the voltage doubler rectifier for 110 V AC. Thus, ideally the resonant tank design of the LLC converter only considers 220 V AC input case, and the required DC gain will reduce to a great extent. The detailed comparison of full bridge rectifier and FB-VD rectifier, as well as their impact on the LLC stage design will be explained in a later section.

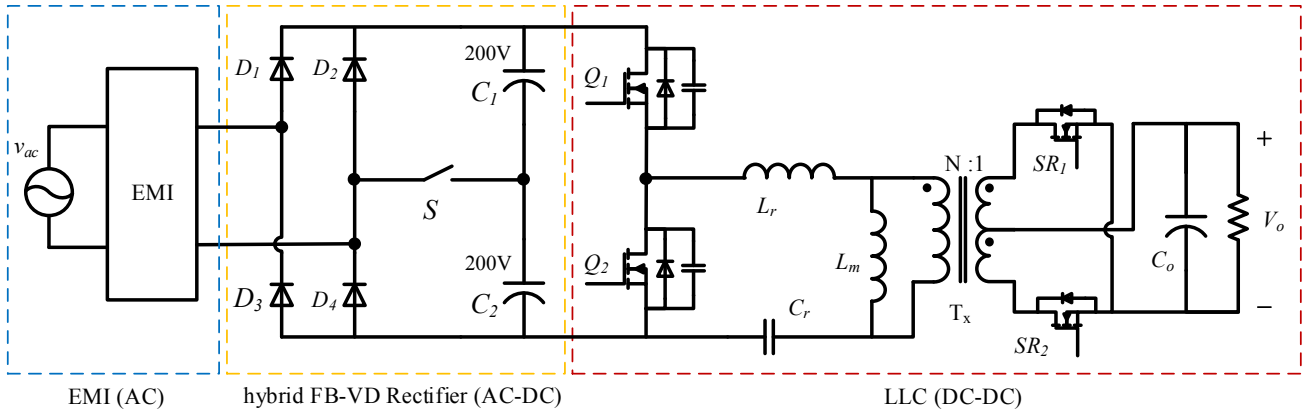


Fig. 1. Single stage LLC converter with hybrid FB-VD rectifier for AC-DC power adapter

The research focuses of this paper are 1) the FB-VD rectifier, 2) the LLC stage design. In this paper, two new single stage LLC converter with improved hybrid rectifiers are proposed. Like the conventional FB-VD rectifiers, the proposed rectifier will automatically switch between full bridge and voltage doubler configuration to accommodate different AC input conditions. Compared with conventional FB-VD rectifier, the proposed configuration's features include: fewer switch number, reduced switch stress, and simplified the driving scheme. Most importantly, the conduction loss in the switches is reduced.

II. Principle and Analysis of the Proposed FB-VD Rectifiers

A. Conventional FB-VD rectifier

The circuit diagram of the single stage LLC converter with conventional FB-VD rectifier for AC-DC power conversion has been shown in Fig. 1. This hybrid rectifier has been widely used in the industrial applications since 1990s [6], [7]. In Fig. 1, the switch S should be of bidirectional current-conducting and voltage-withstanding capability. As shown in Fig. 2, such switch is usually implemented by two MOSFETs with back-to-back configuration. Alternatively, it could be a TRIAC, mechanical or solid state relay. C_1 and C_2 should be 200 V rating electrolytic capacitors of same capacitor value.

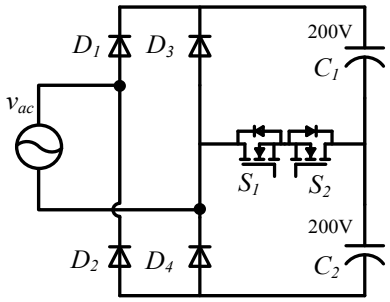


Fig. 2. conventional FB-VD rectifier

For 220 V AC input, the switches S_1 and S_2 remain off. So the D_1, D_2, D_3, D_4, and C_1, C_2 form a full bridge rectifier. The total capacitor value is half C_1 (or C_2).

For 110 V AC, the switches S_1 and S_2 should always be turned on. D_3 and D_4 do not operate at 110 V case, as they will be short circuit by S_1 and S_2 in the positive and negative half line cycle, respectively. So D_1, D_2, C_1, C_2, and S_1, S_2 form a voltage doubler rectifier. C_1 is charged during positive half line cycle, and C_2 is charged during the negative half cycle.

If C_1 and C_2 are of enough large value, 110 V AC should have same rectified DC output voltage as 220 V AC. In practice, C_1 and C_2 value is limited by the physical size. Thus, the output voltage of 110 V AC is only close to "doubled".

B. Proposed FB-VD rectifier #1

As shown in Fig. 3, for the proposed FB-VD #1, only one MOSFET is used instead two in the conventional structure. A 400 V rating capacitor as C_1 should be used for the 220 V AC case. Although this high voltage rating capacitor is not desirable, the overall cost are expected to reduce. Besides, when the rectifier is working in voltage doubler mode at 110 V AC, the conduction loss in the auxiliary switches will be reduced to half as compared to the conventional structure. Generally, 110 V AC is the worst case in terms of efficiency, since the current stress is high. Thus saving this part of loss is very desirable. The driver design is also simplified in that the driver could be powered by C_1. In this design, C_1 and C_2 capacitor value is chosen as 68 μF.

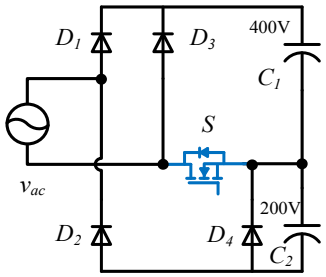


Fig. 3. Proposed FB-VD #1

The waveform of the FB-VD #1 at 110 V AC case is shown in Fig. 4. Vac is the input voltage; *Vo_FBVD_1* is the output voltage of the rectifier; V_{C1} and V_{C2} are the voltage stress on C_1 and C_2. I_{D1} and I_{D2} are the current stress in the diode D_1 and D_2.

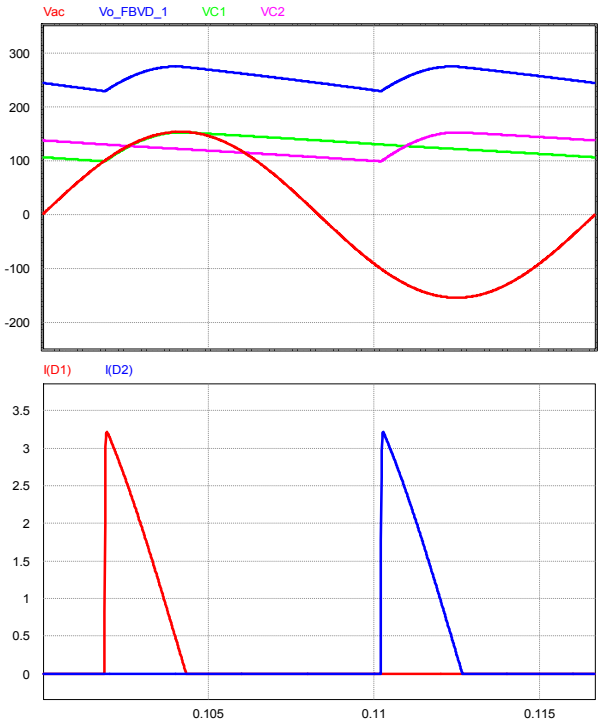


Fig. 4. FB-VD #1 waveform at 110 V AC

When the input AC voltage is below the output voltage, there is no current in the circuit. The two capacitors C_1 and C_2 in series discharge to provide power the load. When the input

AC is higher than the capacitor voltage, then the two capacitors could be charged. The charging current is approximately equal to the diode input current. The analysis here focuses on the charging process, during which the input current causes loss in the rectifier.

The charging process of FB-VD #1 at 110 V AC case is shown in Fig. 5. During the positive half cycle, as shown in Fig. 5 (a), D_1, C_1, S will conduct, so C_1 is charged by the AC source. It should be noted that, during this process, C_2 is not charged, and it is discharging to power the load.

During the negative half cycle, as shown in Fig. 5 (b), S, C_2, D_2 will conduct, so C_2 is charged by the AC source. During this process, C_1 is discharging.

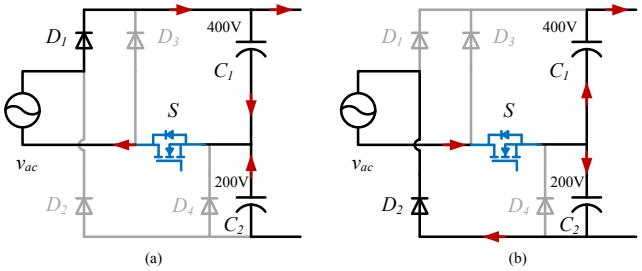


Fig. 5. Capacitor Charging process of FB-VD #1 at 110 V AC
(a) during positive half cycle; (b) during negative half cycle

Fig. 6 shows the waveform of the proposed FB-VD #1 at 220 V AC input case. The output of the rectifier resembles the full bridge rectifier despite that C_1 will be around 400 V, while C_2 only slightly participates the power transfer.

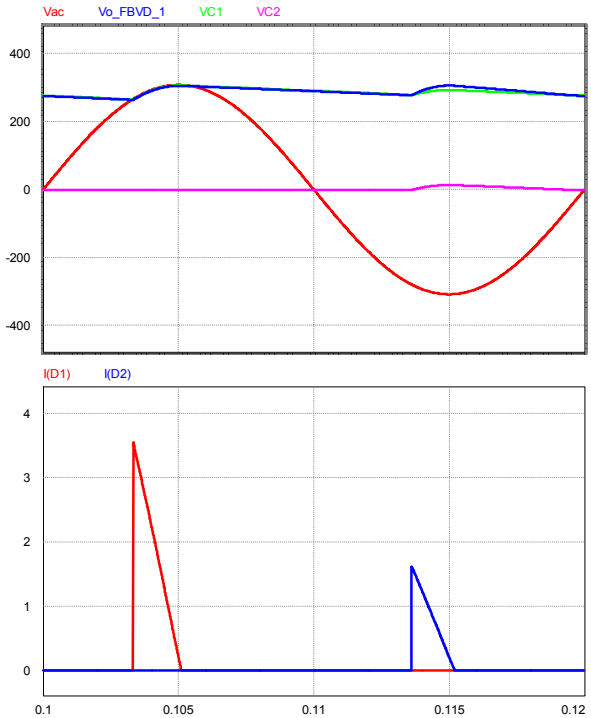


Fig. 6. FB-VD #1 waveform at 220 V AC

The operation of FB-VD #1 at 220 V AC case is shown in Fig. 7.

The charging process in the positive half cycle is shown as Fig. 7 (a). D_1, C_1 and the body diode of S will conduct to charge C_1. However, C_2 will not be charged due to the lack of charging path. D_4 will conduct to power the load, which also clamps C_2 to 0 V.

During the discharging process in the positive half cycle, as shown in Fig. 7 (b), C_1 will discharge through D_4. C_2 will still be clamped to 0 V.

Fig. 7 (c) shows the charging process in the negative half cycle. C_1 and C_2 will be charged together through D_2 and D_3. As the equivalent capacitance is reduced to only half C_1 (or C_2), the input current is also reduced to approximately half as compared to the positive half cycle.

Fig. 7 (d) shows the discharging process in the negative half cycle. As C_2 has been charged in stage (c), it also participates the discharging. When C_2 voltage reduces to 0 V, then D_4 will conduct, and C_1 alone provides power to the load. This process is same as that shown in Fig. 7 (b).

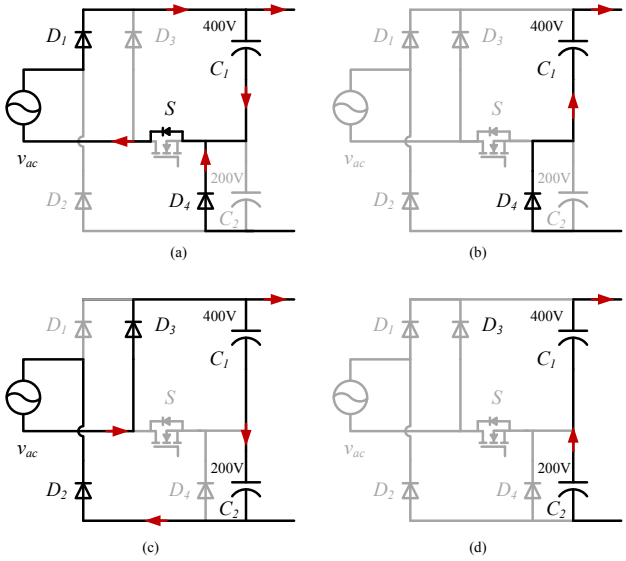


Fig. 7. Operation modes of FB-VD #1 at 220 V AC
(a) capacitor charging process during positive half cycle;
(b) capacitor discharging process during positive half cycle;
(c) capacitor charging process during negative half cycle;
(d) capacitor discharging process during negative half cycle

C. *Proposed FB-VD rectifier #2*

As shown in Fig. 8, in the proposed FB-VD #2, two MOSFETs are placed on the capacitor shunt branches instead of the common branch in the conventional structure. Thus, the conduction loss is reduced to half. It is even more beneficial from the thermal point of view, because the hot spot is split. At 220 V AC operation, C_1 and C_2 will not be connected. A 400 V rating capacitor C_3 is needed for full bridge mode operation. The value of C_3 is small, as the voltage ripple of 220 V AC input is much smaller than 110 V AC case. When operating at

110 V case, C_1, C_2 and C_3 will operate, thus, C_1 and C_2 value could be smaller as compared to conventional structure. In this design, C_1 and C_2 capacitor value is chosen as 47 µF at 200 V rating; C_3 value is chosen as 22 µF at 400 V rating. Thus, the overall size of C_1, C_2 and C_3 should be similar to two 68 µF capacitor at 200 V rating in conventional FB-VD structure, since the total CV product is very close.

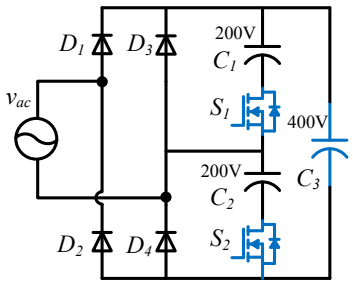


Fig. 8. Proposed FB-VD #2

The waveform of the FB-VD #2 at 110 V AC case is shown in Fig. 9. Vac is the input AC voltage at 60 Hz; *Vo_FBVD_2* is the output voltage of the rectifier; V_{C1} and V_{C2} are the voltage on C_1 and C_2. I_{D1} and I_{D2} are the current stress in the diode D_1 and D_2.

Fig. 10 shows the operation of FB-VD #2 at 110 V AC input. During the positive half cycle, as shown in Fig. 10 (a), C_1 is charged through D_1 and S_1. C_3 is charged through D_1 and S_2. C_2 discharges to provide current for both C_3 and the load. As can be observed in Fig. 9, V_{C2} have a dip during C_1 is charged.

During the negative half cycle, as shown in Fig. 10 (b), C_2 is charged through S_2 and D_2. C_3 is charged through S_1 and D_2. C_1 discharges to provide current for both C_3 and the load.

As shown in Fig. 10 (c), when the capacitors are not charging, C_1 and C_2 are connected in series and providing power to the load with C_3 in parallel.

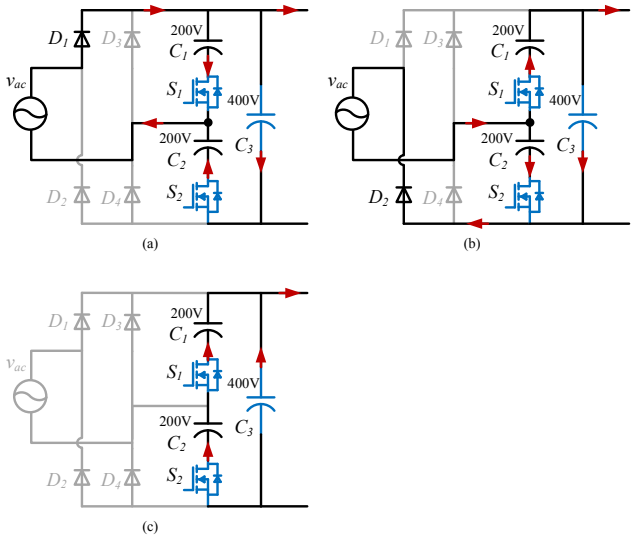


Fig. 10. Operation modes of FB-VD #2 at 110 V AC (a) capacitor charging process during positive half cycle; (b) capacitor charging process during negative half cycle; (c) capacitor discharging process

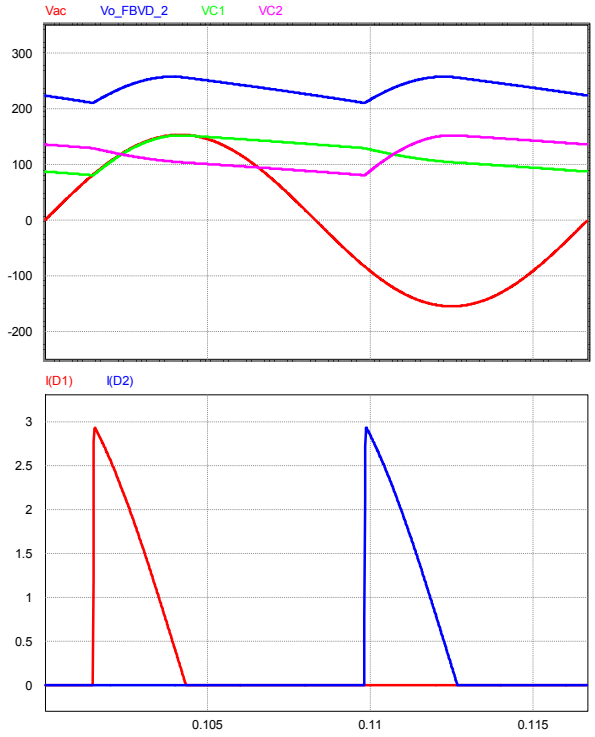


Fig. 9. FB-VD #2 waveform at 110 V AC

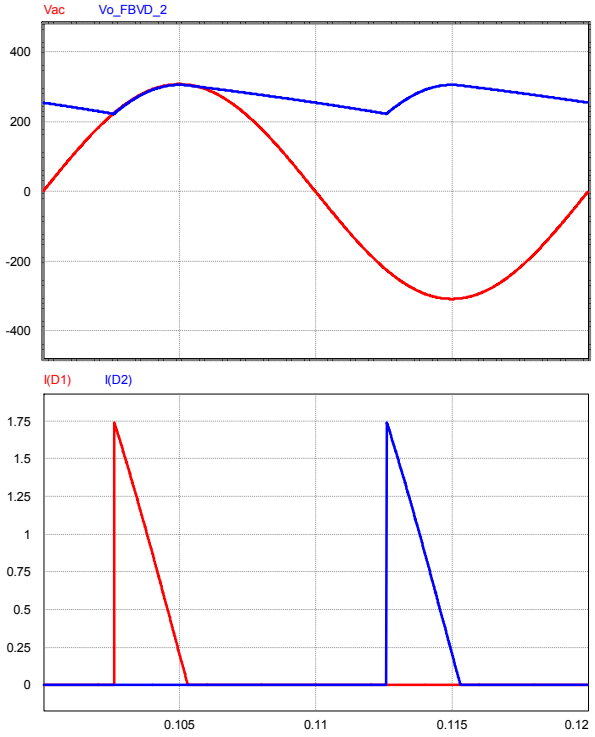


Fig. 11. FB-VD #2 waveform at 220 V AC

Fig. 11 shows the waveform of the proposed FB-VD #2 at 220 V AC input case. C_1, C_2, S_1 and S_2 remain idle at 220 V. $D_1 – D_4$ and C_3 operate as full bridge rectifier.

The operation of FB-VD #1 at 220 V AC case is shown in Fig. 12. The C_3 charging process during the positive and negative half line cycle are shown in Fig. 12 (a) and (b), respectively. D_1 and D_4 will conduct during the positive half cycle, and D_2 and D_3 for the negative.

When the rectifier is not conducting, C_3 will provide power for the load.

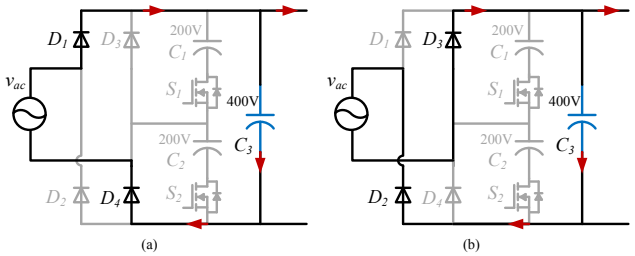


Fig. 12. Capacitor Charging process of FB-VD #2 at 220 V AC
(a) during positive half cycle; (b) during negative half cycle

D. *Performance comparison of the conventional and proposed FB-VD rectifiers*

The proposed FB-VD rectifiers are analyzed and compared with the conventional structure in this section from loss and power density point of view.

The specification of the analysis is shown in Table I. The analysis is conducted at 65 W. 650 V MOSFETs are used for safety consideration. In the table, the power density is calculated based on a 65 W, 1 MHz LLC prototype of 7.5 cm (L) * 3.2 cm (W) * 2.2 cm (H).

Table I. SPECIFICATION OF THE FB-VD RECTIFIERS

	Conventional FB-VD rectifier	Proposed FB-VD rectifier #1	Proposed FB-VD rectifier #2
Po	65W		
$D_1 – D_4$	600V 1V@1A (ES1J)		
MOSFETs	650V 190mOhm (IPD65R190C7)		
Switch No.	2	1	2
C_1	68 µF (200 V)	68 µF (400 V)	47 µF (200 V)
C_2	68 µF (200 V)	68 µF (200 V)	47 µF (200 V)
C_3	N/A	N/A	22 µF (400 V)
CV product	27,200 µF*V	40,800 µF*V	27,600 µF*V
Power density	1.23 W/cm^3	1.15 W/cm^3	1.23 W/cm^3

The loss breakdown for the three FB-VD rectifiers at 110 V and 220 V operation are summarized in Table II and Table III, respectively. The forward voltage drops of the input diode bridge used for calculation is 1V. The loss angle of the electrolytic capacitor used for calculation is 0.15, which is commonly seen value in the vendor's datasheet. The MOSFET Rdson is as in Table I. The current stress in the components are from PSIM simulation.

It could be observed that at 220 V operation, the three types of the FB-VD rectifier have similar losses. For 110 V case, at which the losses are nearly doubled due to the high current, the proposed two FB-VD rectifiers reduce the overall loss from ~1W to 0.75W, which is 1/4 of reduction. With this, the total efficiency improves approximately 0.4%. It should be noted that if D_2 and D_4 are replaced with MOSFETs operating as SR, then the efficiency improvement will be even more significant.

Table II. LOSS BREAKDOWN FOR FB-VD RECTIFIERS AT 110 V AC

	Conventional FB-VD rectifier	Proposed FB-VD rectifier #1	Proposed FB-VD rectifier #2
$D_1 – D_4$	0.512 W	0.512 W	0.548 W
S_1, S_2	0.435 W	0.218 W	0.15 W
C_1, C_2	0.03 W	0.03 W	0.03 W
C_3	N/A	N/A	0.002 W
Total	0.98 W	0.76 W	0.73 W

Table III. LOSS BREAKDOWN FOR FB-VD RECTIFIERS AT 220 V AC

	Conventional FB-VD rectifier	Proposed FB-VD rectifier #1	Proposed FB-VD rectifier #2
$D_1 – D_4$	0.474 W	0.452 W	0.48 W
S_1, S_2	0 W	0.07 W	0 W
C_1, C_2	0.017 W	0.03 W	0 W
C_3	N/A	N/A	0.02 W
Total	0.49 W	0.55 W	0.5 W

III. DESIGN OF LLC WITH REDUCED INPUT VOLTAGE RANGE

The motivation of using hybrid rectifier is to reduce the operational DC input voltage range, i.e. the required voltage gain, of the LLC stage. By doing so, a large magnetizing inductor could be used to reduce the both the magnetizing and the resonant current (and thus the conducting loss) in the resonant tank.

The design specifications are summarized in Table IV. The maximum DC input voltage is calculated from 264 V * 1.414 = 373 V, at which the LLC converter should operate at the resonant frequency. Based on this criteria, the turns ratio is designed at 10:1 for 19 V output voltage.

Table IV. DESIGN SPECIFICATION

Input AC Voltage	90 V AC – 277 V AC
Max Input DC Voltage	373 V DC
Output Voltage	19 V DC
Turns Ratio	10 : 1
Output Power	65 W

The rectified DC voltage of the proposed FB-VD #2 is compared with that of the full bridge rectifier (note not the conventional FB-VD) for both 220 V, 50 Hz and 110 V, 60 Hz AC input. For the FB-VD #2, two 47 µF capacitors at 200 V rating plus one 22 µF capacitors at 400 V rating are used. While for the FB rectifier, one 68 µF 400 V rating capacitor is used to match the CV product (size) of the capacitors used in FB-VD #2. The rectified DC voltages of both configurations

are shown in Fig. 13 and Fig. 14. In Fig. 13, the DC voltage range is from 107 V to 152 V for conventional full bridge rectifier. While with the FB-VD rectifier, the DC voltage increases to above 225 V.

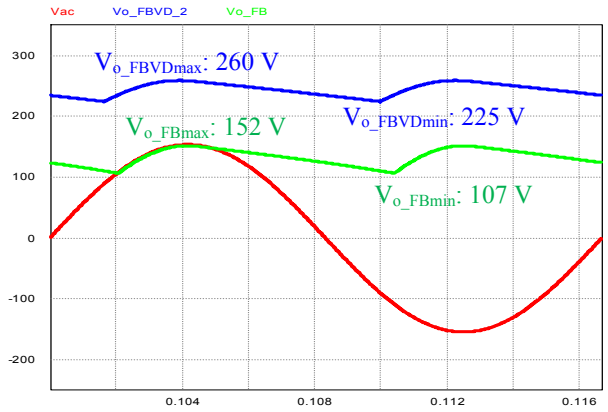


Fig. 13. Rectified voltage of FB-VD #2 (47 µF 200 V * 2 + 22 µF 400 V) and conventional FB (68 µF 400V) for 110 V 60 Hz AC input

In Fig. 14, the DC voltage range for conventional full bridge rectifier at 220 V input is very narrow. While with the FB-VD rectifier, the minimum DC voltage remains very close to that at 110 V case.

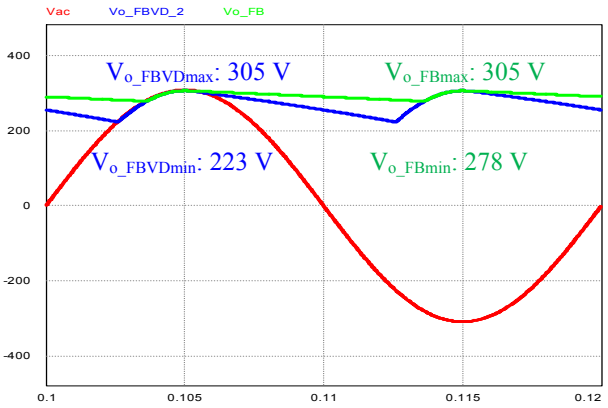


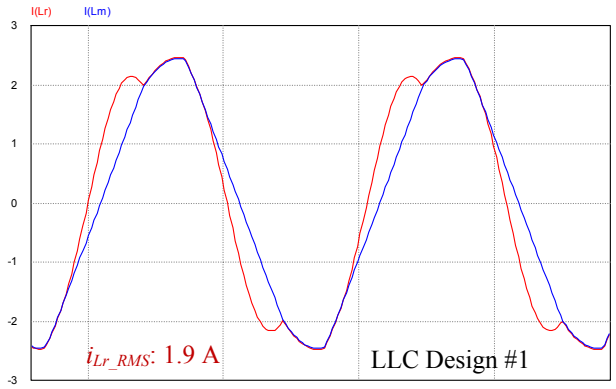
Fig. 14. Rectified voltage of FB-VD #2 (47 µF 200 V * 2 + 22 µF 400 V) and conventional FB (68 µF 400V) for 220 V 50 Hz AC input

The conclusion here is that with the FB-VD rectifier, conventional or the proposed, the rectified DC voltage range reduces significantly. It is observed that the minimum DC voltage increases from 107 V to 223 V, which means the required voltage gain for the LLC stage reduces from 3.5 (373 V / 107 V) to 1.7 (373 V / 223 V).

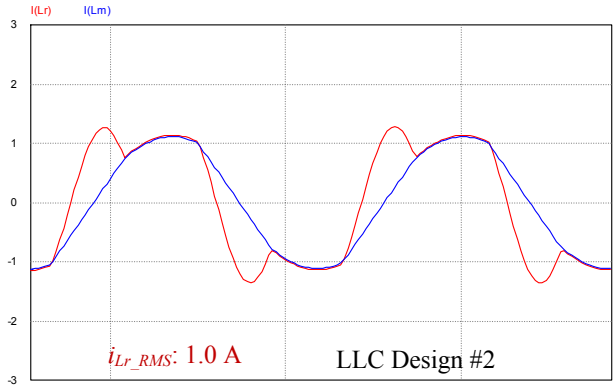
Table V. LLC PARAMETER DESIGN

	LLC Design #1	LLC Design #2
Lr	7 µH	7 µH
Cr	2 nF	2 nF
Lm	15 µH	35 µH
Gain (Vin_min)	3.5 (107 V)	1.7 (223 V)

Fig. 15 shows the resonant current comparison of two designs based on 107V and 223V minimum input. The designed parameters are shown in Table V. It is observed that the resonant current reduces significantly (~ halved) in terms of both RMS value and peak value, with the required voltage gain reducing from 3.5 for LLC Design #1 to 1.7 for LLC Design #2. It is expected the conducting loss in the HB switches and the transformers (inductor integrated) will be quartered.



(a)



(b)

Fig. 15. Resonant current stress of (a) LLC Design #1 and (b) LLC Design #2

IV. EXPERIMENT RESULTS

A 65W prototype was built to verify the feasibility of proposed two FB-VD rectifiers. The design specification is shown is Table I. The LLC parameter design is shown in Table V as LLC Design #2.

Fig. 16 shows the waveforms of the FB-VD #1 at 110 V 60 Hz AC input operation. The rectified DC voltage is from 225 V to 275 V, which agrees with the simulation result. The peak value of the input current stress is 4 A. It is somewhat higher than the simulation due to the impact of the parasitic components in the circuit.

Fig. 17 shows the waveforms of the FB-VD #1 at 220 V 50 Hz AC input operation. The results have very good agreement with the simulation. During the positive half cycle, only C_1 is charged. While during the negative half, both C_1 and C_2 are charged. This explains the asymmetric current waveform.

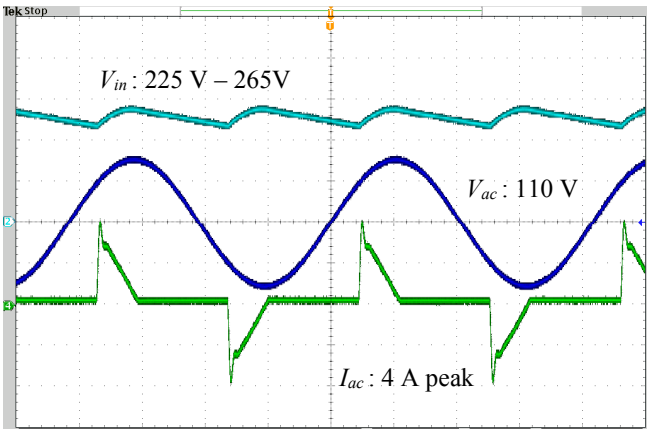


Fig. 16. Experiment waveforms of the FB-VD #1 at 110 V 60 Hz AC input. CH1: AC voltage (100 V/div); CH2: Rectified DC voltage (100 V/div); CH4: Input current (2 A/div).

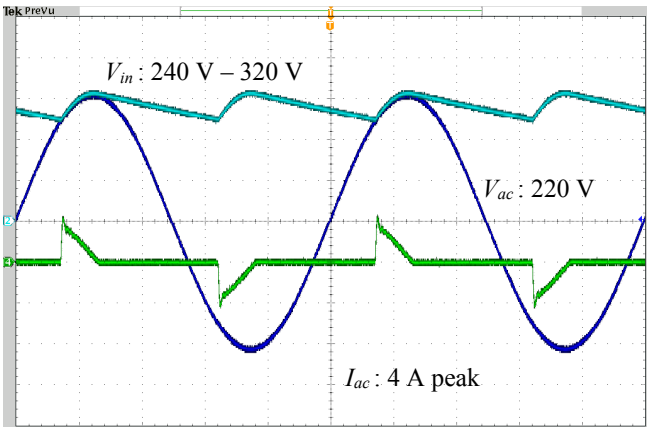


Fig. 19. Experiment waveforms of the FB-VD #2 at 220 V 50 Hz AC input. CH1: AC voltage (100 V/div); CH2: Rectified DC voltage (100 V/div); CH4: Input current (2 A/div).

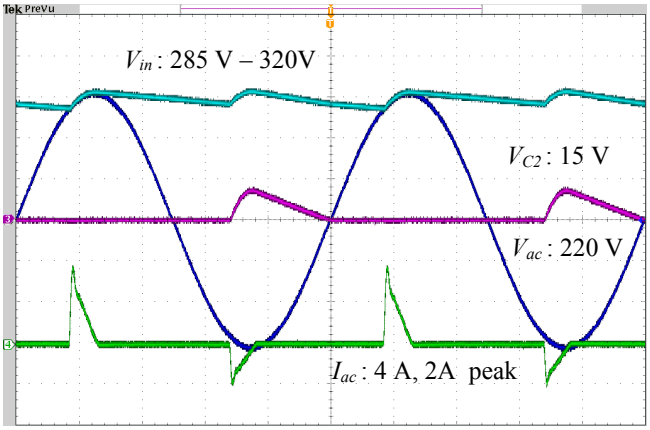


Fig. 17. Experiment waveforms of the FB-VD #1 at 220 V 50 Hz AC input. CH1: AC voltage (100 V/div); CH2: Rectified DC voltage (100 V/div); CH3: VC2 (20 V/div); CH4: Input current (2 A/div).

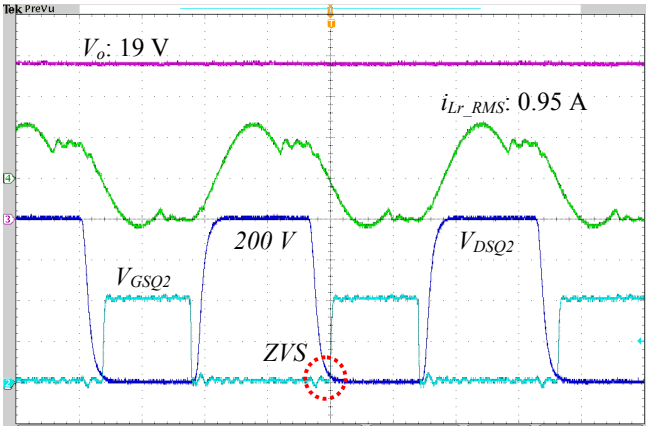


Fig. 20. Experiment waveforms of LLC converter at 200 V input at 700 kHz. CH1: DC voltage (50 V/div); CH2: Q2 Gate signal (5 V/div); CH3: Vo (5 V/div); CH4: Resonant current (1 A/div).

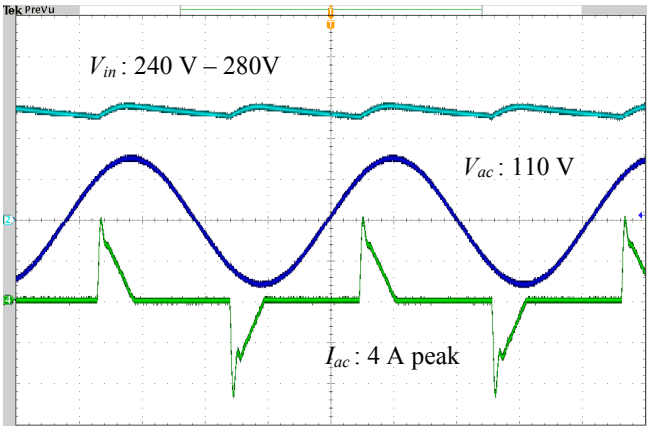


Fig. 18. Experiment waveforms of the FB-VD #2 at 110 V 60 Hz AC input. CH1: AC voltage (100 V/div); CH2: Rectified DC voltage (100 V/div); CH4: Input current (2 A/div).

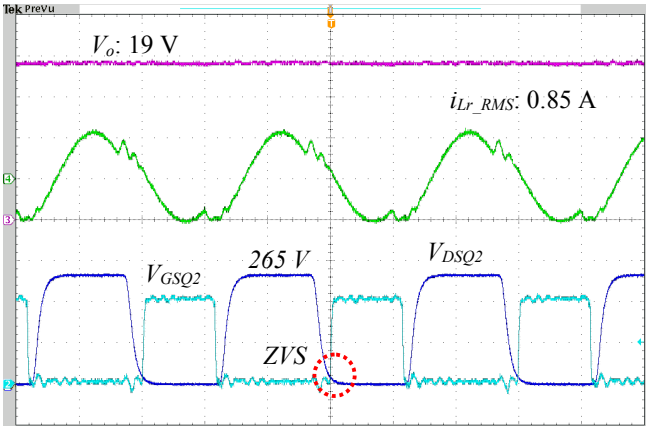


Fig. 21. Experiment waveforms of LLC converter at 265 V input at 850 kHz. CH1: DC voltage (100 V/div); CH2: Q2 Gate signal (5 V/div); CH3: Vo (5 V/div); CH4: Resonant current (1 A/div).

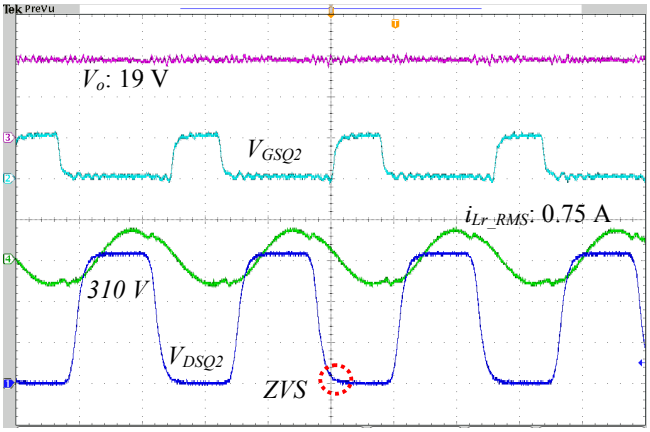


Fig. 22. Experiment waveforms of LLC converter at 310 V input at 1 MHz. CH1: DC voltage (100 V/div); CH2: Q2 Gate signal (10 V/div); CH3: Vo (10 V/div); CH4: Resonant current (1 A/div).

Fig. 18 shows the waveforms of the FB-VD #2 at 110 V 60 Hz AC input operation. And Fig. 19 shows the waveforms of the FB-VD #2 at 220 V 50 Hz AC input operation. The results have good agreement with the analysis and simulation.

In real world, considering the losses in the power train, as well as 100 V AC input operation, the input voltage of the LLC stage should be designed even wider. In this paper, the LLC stage could operation from 200 V to 370 V.

Fig. 20 shows the waveform of the LLC stage at 200 V DC operation. The switching frequency is 700 kHz. The resonant current is controlled below 1 A with a relatively large magnetizing inductor of 35 µH. As can be observed, the HB switches could achieve ZVS even at 200 V case, which is the lowest input voltage.

Fig. 21 shows the waveform of the LLC stage at 265 V DC input condition. This is the generally the maximum input voltage at 110 V AC. The switching frequency is 850 kHz. The resonant tank current is 0.85 A as RMS value.

Fig. 22 shows the waveform of the LLC stage at 310 V DC input condition, which is the maximum voltage at 220 V AC input. The switching frequency reaches 1 MHz. The resonant tank current is 0.75 A as RMS value. Still, ZVS operation can be achieved.

V. Conclusion

A 1-MHz single stage LLC converter with improved hybrid full bridge / voltage doubler rectifier is proposed for the laptop power adapter. Two configurations of hybrid FB-VD rectifiers have been proposed with reduced cost and improved efficiency. By using the FB-VD rectifiers, the required input voltage range is reduced for the LLC stage to a great extent. Such that a large magnetizing inductor could be used in the LLC converter, and the circulating current is reduced significantly. Analysis of the proposed FB-VD rectifier has been explained in the paper. Two designs of LLC converter with different voltage gain has been compared. Besides, a 65 W prototype was built to verify the proposed FB-VD rectifiers' operation as well as the LLC converter. The experiment results have very good agreement with the analysis and the simulation.

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