Parallel Energy Buffering LED Driver Achieves Electrolytic Capacitor-less and Flicker-free Operation

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***Abstract*—AC powered LED drivers experience imbalanced energy, between input and output, in a half line cycle. To achieve flicker-free operation, the imbalanced energy needs to be buffered, and often by energy-dense electrolytic capacitors. However, electrolytic capacitors are also well-known for short lifespan and the limiting factor of LED drivers' life. High voltage film capacitors and Buck converter had been used in the proposed LED driver to buffer imbalanced energy. When $P_{in} > P_{LED}$, the extra energy is transferred from AC input directly to the high voltage film capacitors. When $P_{in} < P_{LED}$, the shortage energy is transferred from the high voltage film capacitors to the output by the Buck converter. The imbalanced energy goes through two times power conversion in the proposed LED driver, which is one time less than other comparable electrolytic capacitor-less designs. Therefore, an improved efficiency can be achieved. A 28W Flyback topology based experimental prototype had been built and tested to verify the proposed design.**

Keywords—Energy buffering, Energy imbalance, Flicker-free LED driving, Electrolytic capacitor-less

I. INTRODUCTION

Light Emitting Diodes (LED) are great technological advancement in the lighting industry and have the potential to fundamentally change the future of lighting. They swept conventional incandescent, neon and fluorescent lighting devices for a variety of reasons, most notably their extended lifespan, reduced energy consumption, and low maintenance requirements. The benefit of energy saving from using LED lighting is phenomenal. Although using LED lighting is very promising, there are a lot of challenges that need to be overcome with the design of LED drivers, especially with AC powered LED driver, where a great deal of rigorous industry standards and regulations kick in. For example, EnergyStar requires power factor correction (PFC) implementation with AC powered LED drivers. They should have a PF higher than 0.7 for residential usage and 0.9 for commercial usage. In addition, there is also IEC61000-3-2 that imposes limitations on input harmonic currents. To meet these requirements, active power factor correction technology is usually implemented with AC powered LED drivers. As a result, the input power becomes a time-varying waveform, and there is an imbalanced energy between input and output in a half line cycle.

In conventional practice, the imbalanced energy is buffered by electrolytic capacitors being connected at the output of a PFC stage. It also leads to the generation of a double-line-frequency ripple voltage on the PFC output. For a single stage LED driver, the PFC is the only power stage and, therefore, the ripple voltage is directly applied on its LED load. The ripple voltage will produce an even more excessive double-line-frequency ripple current as an LED load has very low intrinsic resistance. The ripple current proportionally presents itself as light fluctuation – flicker. Although double-line-frequency flicker is usually not visible, it may lead to many well-known health issues, such as headache, fatigue and even seizure [3]. Two-stage LED drivers can naturally achieve flicker-free operation. The ripple voltage from a PFC output is filtered by a second stage converter. A double-line-frequency ripple free DC LED voltage is available at the output of the second stage converter to achieve flicker-free operation. The drawback of two-stage LED drivers is extra power loss from the second power stage, resulting in lower efficiency.

In addition to avoiding flicker, extending the lifespan of LED drivers is also paramount. Electrolytic capacitors are used both in conventional single-stage and two-stage LED drivers to buffer the double-line-frequency imbalanced energy. The drawback of using electrolytic capacitor is their limited lifespan. Although the life of electrolytic capacitors can vary with the conditions of operating temperature and ripple current, it is usually in the range of 1,000 ~ 10,000 hours. The electrolyte gradually dissipates in electrolytic capacitors and capacitance is reduced. On the contrary, LEDs are just semiconductor chips that can have several decades of lifespan. Therefore, it is critical to eliminate electrolytic capacitors in LED driver designs to achieve significant lifespan extension of LED lighting fixtures.

A variety of LED driving methods had been proposed attempting to reduce flicker, improve efficiency, reduce cost and eliminate electrolytic capacitors. These previous LED driving methods can be broadly categorized as follows: (1) Input harmonic currents injection methods [5]&[6]. Higher order harmonic currents are added to the fundamental AC input current to reduce imbalanced energy in a half line cycle. In this way, the double-line-frequency ripple voltage at the output of a single-stage LED driver is reduced as well as flicker. (2) Two-stage integrating methods [7]-[9]. The first stage PFC and the second stage DC-DC converter are

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combined to share power components. It can reduce cost but introduces additional constraints on design and operation. (3) Ripple voltage cancellation methods [10]-[14]. An opposite ripple voltage is generated and used to cancel the double-line-frequency ripple voltage produced by the main PFC stage of a LED driver. A DC LED voltage can be produced and applied to a LED load to achieve flicker-free LED driving. (4) Active filtering and three-port methods [15]-[17]. The imbalanced energy between the AC input and the LED output are buffered by the film capacitors.

A bi-directional DC-DC converter is used to transfer the imbalanced energy between the main circuit and the film capacitors. And there are other LED driving methods that do not fall into the above categories, such as output current shaping LED driver [18], two parallel inverted Buck converter average current modulation LED driver [19], averaged LED current modulation method [20], stacked switch capacitor LED driver [21], and valley-fill LED driver [22]-[24] and one and half stage LED driver [24]. The topology presented in [25] looks very similar to the topology proposed in this paper. However, it is operated in a very different way. When $P_{in} > P_{LED}$, the extra imbalanced energy cannot be effectively buffered, which leads to compromised LED lighting performance.

In this paper, an energy buffering LED driver is proposed to eliminate electrolytic capacitors as well as to achieve high power factor, flicker-free LED driving. It can reduce power conversion loss as compared to previous electrolytic capacitor-less design. A 28W experimental prototype had been built and tested to verify the operating principle. The remaining of this paper is arranged as follows. The concept of the proposed LED driver is derived in Section II. The circuit implementation and detailed operating principle are discussed in Section III. The control strategy is discussed in Section IV and the design analysis is discussed in Section V. Experimental result is discussed in Section VI and the paper is concluded in Section VII.

II. Basic Idea and Operating Principle of Energy Buffering

Fig. 1 shows the basic concept of the proposed parallel energy buffering LED driver and Fig. 2 shows the circuit implementation of the LED driver. The LED driver includes a main Flyback PFC, a Buck converter and one energy channeling MOSFETs, Q2. In Fig. 1, two switches are needed in the conceptual design to achieve power splitting. In a real circuit implementation, with carefully design, one switch can be removed and only using Q2 is enough. The Flyback PFC shapes the input current to achieve a high power factor and draws energy from the AC input. The Buck converter provides the power difference when $P_{in} < P_{LED}$. Fig. 3 shows the key line cycle waveforms of the proposed parallel energy buffering LED driver.

A. Switching Operation

The Flyback PFC in the proposed LED driver is operated under constant on time, fix switching frequency, discontinues conduction mode (DCM) to naturally achieve a high power factor correction [26]. The design of the Buck converter is very generic. To facilitate the discussion, the Buck converter is only considered as a function unit and its switching operation is not of interest. The switching operations to achieve energy buffering will be discussed in detail and separately for $P_{in} > P_{LED}$ and $P_{in} < P_{LED}$.

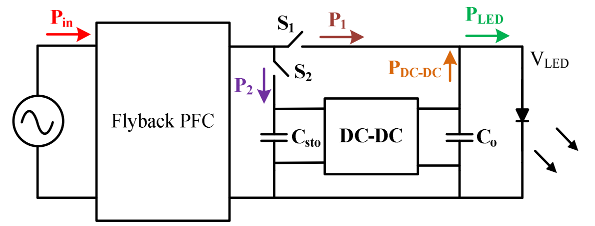

Fig. 1 Concept of the cycle by cycle energy buffering LED driver

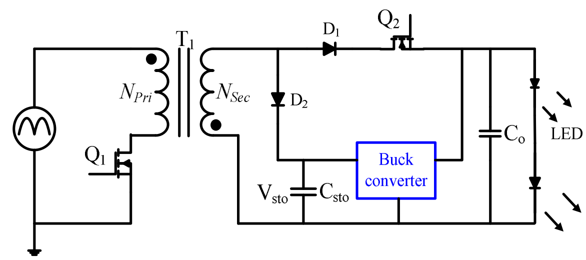

Fig. 2 Circuit implementation of the hybrid energy buffering LED driver

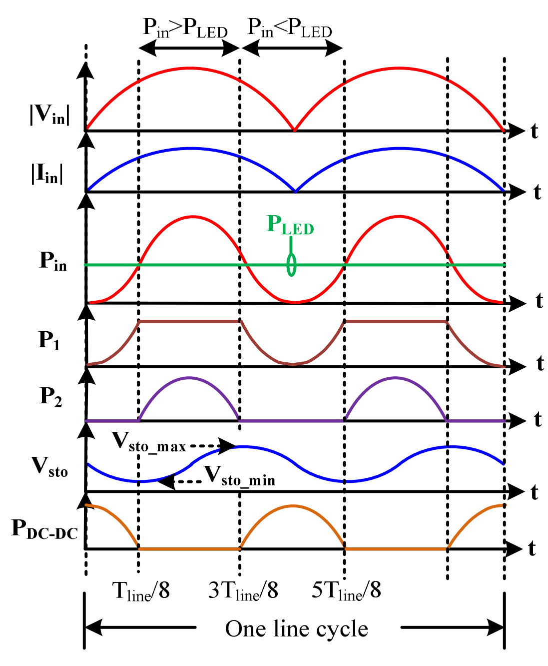

Fig. 3 Key line cycle waveforms of the proposed energy buffering LED driver

When $P_{in} > P_{LED}$

When $P_{in} > P_{LED}$, the Buck converter is not active. One switching cycle is divided into four time intervals, $[t_0\text{-}t_1]$, $[t_1\text{-}t_2]$, $[t_2\text{-}t_3]$ and $[t_3\text{-}t_4]$. Fig. 4 shows the key switching waveforms of the proposed LED driver and Fig. 5 shows the switching operation in each time interval when $P_{in} > P_{LED}$.

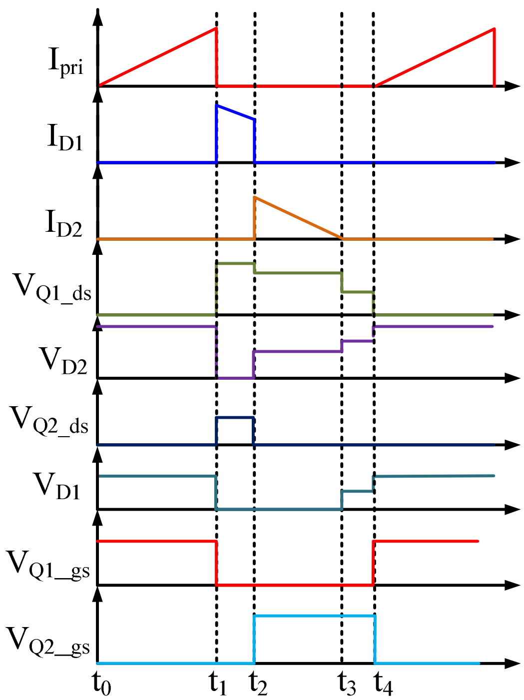

Fig. 4 Key switching waveforms of the proposed LED driver when Pin > PLED

Time interval $[t_0\text{-}t_1]$

One switching cycle starts at time t_0 when Q_1 is turned on. The switching current in winding N_{pri}, I_{pri}, starts increasing from zero. Due to the opposite orientation between the winding N_{pri} and N_{sec}, the diode D_1 and D_2 are reversely biased while the body diode of Q_2 is forward biased. The current I_{pri} peaks at t_1 when Q_1 is turned off and ends this interval.

Time interval $[t_1\text{-}t_2]$

As Q_1 is turned off at time t_1, the magnetic current commutes from the primary side winding to the secondary side winding. The MOSFET Q_2 is still off so that the magnetic current flows in diode D_2. The energy stored in the transformer is transferred to the capacitor C_{sto}. The voltage across the winding N_{sec} is clamped at V_{sto} and reflected to the primary side. This interval ends at t_2 when the MOSFET Q_2 is turned on.

Time interval $[t_2\text{-}t_3]$

The voltage on the secondary side winding is clamped at V_{LED} after Q_2 is on. Since V_{LED} is lower than V_{sto}, the diode D_2 becomes reversely biased and the switching current in D_2 is ended. The switching current in winding N_{sec} continues its flow in D_1 and Q_2 and the Flyback transformer releases its remaining energy to the LED load. The switching current in winding N_{sec} drops to zero at time t_3, which ends this time interval.

Time interval $[t_3\text{-}t_4]$

To achieve DCM operation, there is a small-time interval $[t_3\text{-}t_4]$ when there is no active switching operation. The switching cycle ends at t_4.

When $P_{in} < P_{LED}$

Fig. 6 shows the switching operation during each time interval when $P_{in} < P_{LED}$ and Fig. 7 shows the key

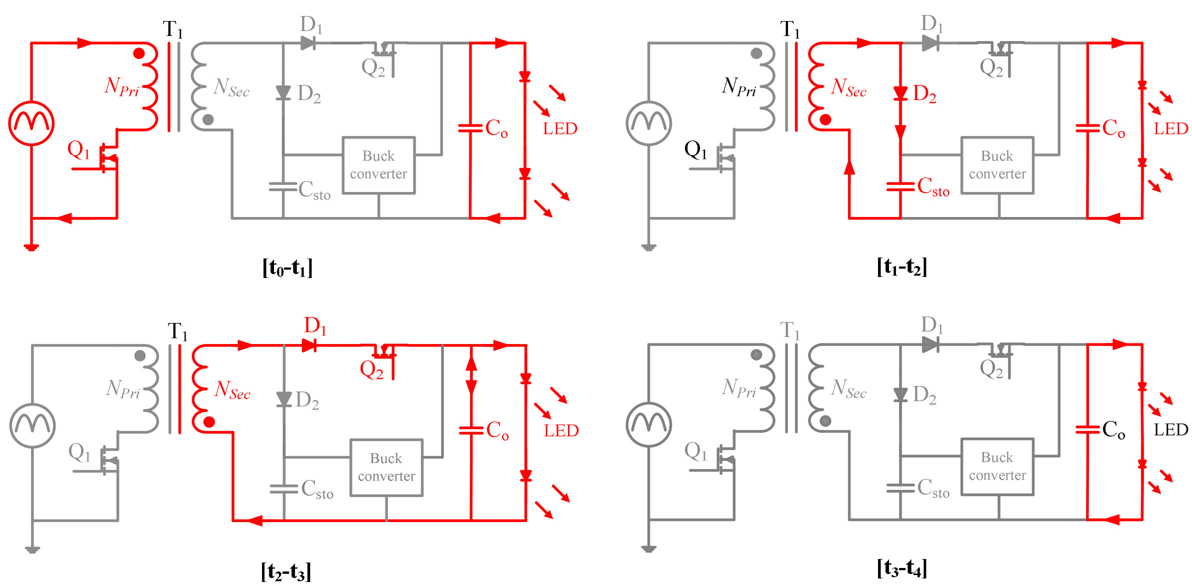

Fig. 5 Switching operation of the LED driver when Pin > PLED

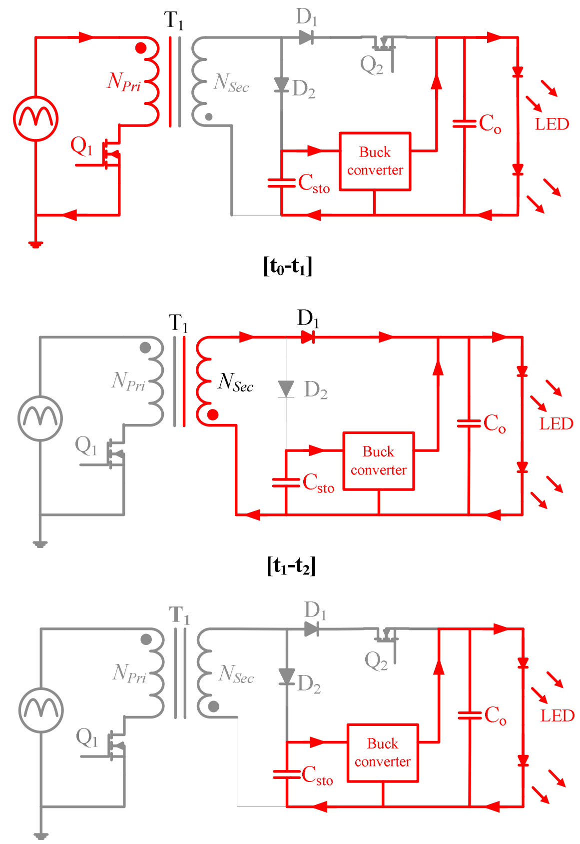

Fig. 6 Switching operation of the cycle by cycle energy buffering LED driver when Pin < PLED

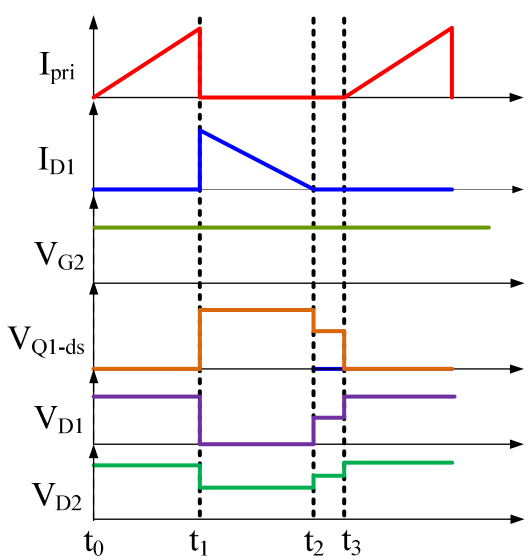

Fig. 7 Key switching waveforms of the LED driver when Pin < PLED

switching waveforms. One switching cycle is further divided into three time intervals [t_0-t_1], [t_1-t_2] and [t_2-t_3]. The MOSFET Q_2 is always on so that P_{in} = P_1. The Buck converter is activated, and energy is transferred from C_{sto} back to the LED load. The control loop will automatically force Q_2 to be fully on to maximize P_1. Therefore, the switching operation under $P_{in} < P_{LED}$ is just a special case of the switching operation under $P_{in} > P_{LED}$ and the detailed discussion on this will not be repeated.

Switching operation over half line cycle

As the switching operation during $P_{in} < P_{LED}$ and $P_{in} > P_{LED}$ had been discussed, the switching operation under the scale of a half line cycle is illustrated in Fig. 8.

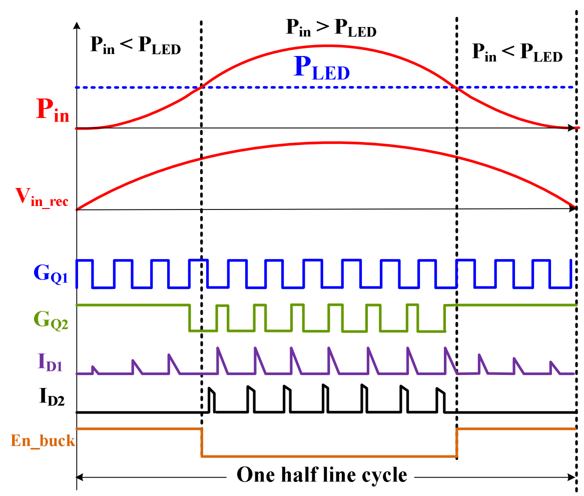

Fig. 8 Switching operation over a half line cycle

III. Control Scheme

Fig. 9 shows the control scheme of the proposed unidirectional current ripple compensation LED driver. There are two current regulation loops and one voltage regulation loop in the system to regulate the LED current and the voltage of the storage capacitor, V_{sto}. Although the goal is to buffer imbalanced energy in every switching cycle, the control is achieved by sensing and regulating currents and voltage.

The current in diode D_1 is sensed and averaged in every switching cycle. The averaged current in D_1, I_{D1_avg}, is then compared with the LED current reference, I_{LED_ref}. If I_{D1_avg} is larger than I_{LED_ref}, the compensated error voltage V_{c2} will be reduced. A reduced V_{c2} will generate a smaller duty cycle for Q_2, which will reduce I_{D1_avg}. When $P_{in} > P_{LED,}$ the duty cycle of Q_2 will be automatically controlled to achieve $I_{D1\_avg} = I_{LED\_ref.}$ When $P_{in} < P_{LED}$, because I_{D1_avg} is always less than I_{LED_ref}, the feedback loop will force Q_2 to be fully on. When it is detected that Q_2 is fully on, the Buck converter will be activated. The difference between I_{LED_ref} and I_{D1_avg}, I_{LED_ref} - I_{D1_avg}, becomes the output current reference of the Buck converter. The current feedback loop of the Buck converter ensures that the current generated by the Buck converter is equal to its reference. Therefore, exact amount of current can be delivered to the LED load under both $P_{in} > P_{LED}$ and $P_{in} < P_{LED}$.

The average voltage of V_{sto} is controlled as well to serve two purposes. First, net-zero energy storage with C_{sto} can be achieved by control the average voltage of V_{sto}. In a half line cycle, it is expected that net energy stored in C_{sto} is zero. In this way, the averaged input power is equal to the LED output power. To achieve this, V_{sto_avg} is compared with the reference voltage V_{sto_ref}. The compensated error, V_{c1}, determines the on time of Q_1, which also means to determine the input power. Whenever V_{sto_avg} is not equal to V_{sto_ref}, V_{c1} will be changed by the feedback loop to change the input power. As a chain reaction, V_{sto_avg} will be adjusted to follow V_{sto_ref} again. For example, if the net stored energy with C_{sto} is above zero, V_{sto_avg} will start growing and eventually become higher than V_{sto_ref}. Once this happens, the compensated error signal V_{c1} will be decreased. A decreased V_{c1} would generate a smaller on time for Q_1, which means less input power. As the output power remaining unchanged, a reduced input power means a reduced net energy stored in C_{sto}. The feedback loop will continues exert this effect and the net energy storage in C_{sto} will eventually become negative in a half line cycle. Then, V_{sto} will start decreasing and eventually be brought down to V_{sto_avg}. It is noted that with constant on time in a half line cycle, together with DCM operation, power factor correction is achieved automatically. In addition, V_{sto} should be controlled to maintain a proper operation. Since there is

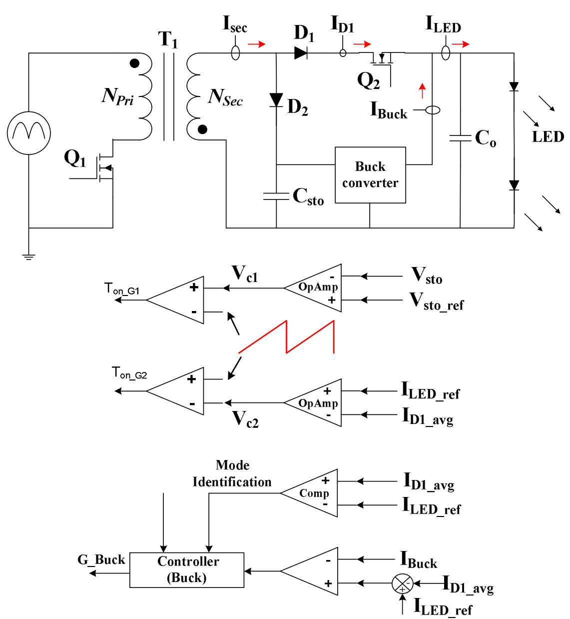

Fig. 9 Control scheme of the proposed unidirectional current ripple compensation LED driver

a significant double-line-frequency ripple voltage on V_{sto}, one needs to make sure that V_{sto_min} is always higher than V_{LED}. The reference voltage for V_{sto_avg} should be designed high enough to maintain this condition, which is achieved by the V_{sto_avg} voltage control loop, as shown in Fig. 9 as well.

IV. Experimental Verification

A 28W experimental prototype had been built and tested to verify the proposed energy buffering LED driving method. TABLE 1 shows the system specification and circuit parameter of the experimental prototype.

TABLE 1 The experimental prototype specification and key components

System Specification	
Input voltage	89Vrms – 132Vrms
Maximum output voltage	~65V
Maximum output current	0.43A
Maximum output power	28W
Circuit Parameter	
Transformer	N_{pri}: N_{sec}: = 1:1 L_{pri}=400μH, EE16 core
Switching frequency	50kHz
PFC Controller	PIC16F1578-I/SS
MOSFET Q1	STB13N80k5 (800V, 12A)
MOSFET Q2	FDP2532 (150V, 8A)
Diode D1	STPSC6H065D1 (650V, 6A)
Diode D2	LQA06T300 (400V, 6A)
Output capacitor	CGA9N3X7S2A106K230KB, 100V, 10μF
Storage capacitor	2 x ECW-FD2W335K 450V, 3.3μF
High and low sides MOSFET (Buck)	IRF730PBF (400V 5.5A)
Controller (Buck)	NCP159DR2G
Output inductor	DELEVAN-224 (220μH, 2.0A)
Output capacitor	CGA9N3X7S2A106K230KB, 100V, 10μF

Fig. 10 shows the key line cycle waveform of the proposed LED driver. 0.99PF had been measured with the AC input. The voltage on the buffer capacitor, Vsto, changes from 70V as minimum to 120V as maximum. The 120Hz ripple LED current is measured to be 21.7mA rms with FFT function in oscilloscope, which converts to 30.7mA peak ripple current. Therefore, the 120Hz ripple current is 7.1% of the average LED current.

Fig. 11 shows the key switching currents, as well as the status of the Buck converter of the proposed LED driver. When $P_{in} > P_{LED}$, the Buck converter is not active, and the extra energy is stored in the storage

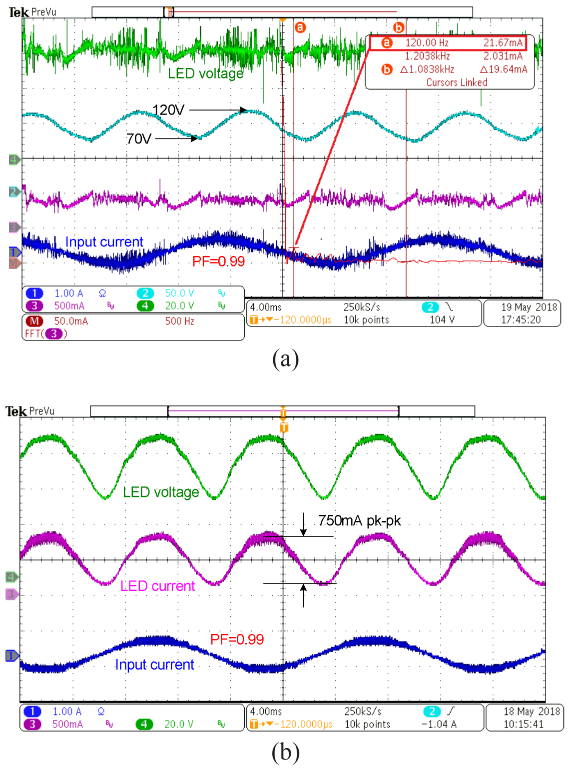

Fig. 10 Key line cycle waveforms of the proposed LED driver under 110Vrms input

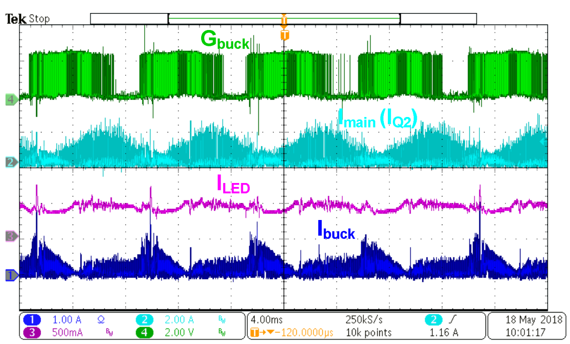

Fig. 11 Key switching waveforms of the proposed LED driver at line frequency time scale

capacitor. When $P_{in} < P_{LED}$, the Buck converter is active and transfers energy to the LED load.

The efficiency of the experimental prototype had been measured and compared with the efficiency of a conventional Flyback LED driver. These two designs share the same PFC stage to make a fair comparison. Both prototypes achieve their highest efficiency at 350mA LED load. The maximum efficiency of the conventional single stage LED driver is 86.6% while the maximum efficiency of the proposed LED driver is 85.6%, which is 1% lower and a very small price to pay when flicker-free LED driving and electrolytic-capacitorless design is achieved.

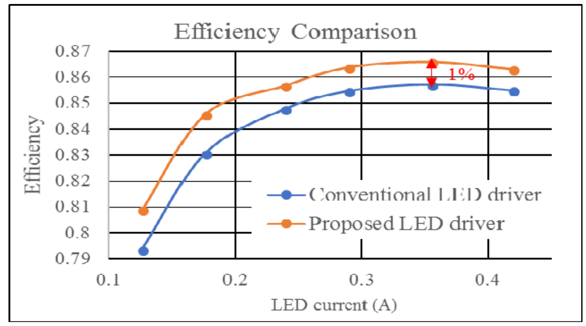

Fig. 12 Efficiency comparison between the proposed unidirectional current ripple compensator LED driver and a conventional LED driver

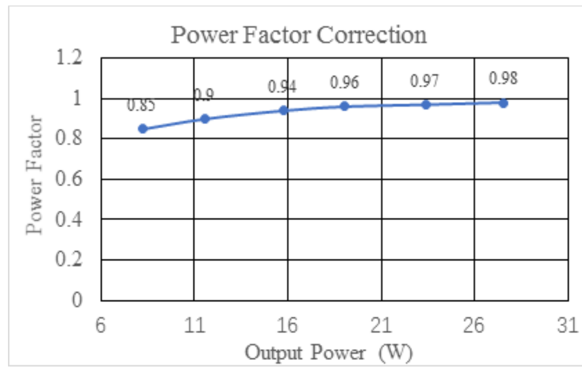

Fig. 13 Power factor performance under 110Vrms input

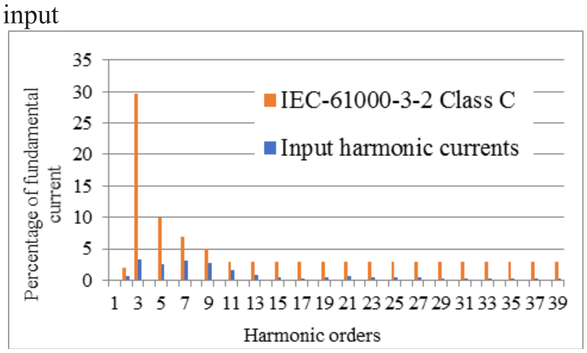

Fig. 14 Input harmonic currents versus IEC-61000-3-2 limit under 110Vrms input, full load

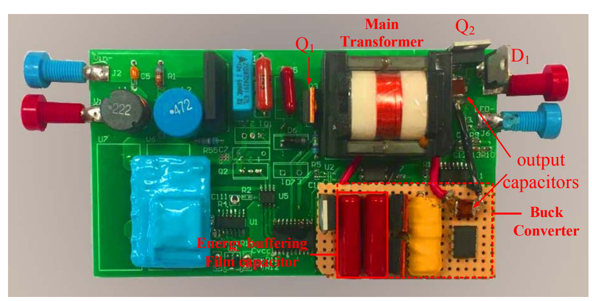

Fig. 15 Photo of the experimental prototype

Fig. 13 shows the power factor of the proposed LED driver. Since the proposed LED driver applies the same PFC technology as a conventional design, a high

PF is achieved. At full load, the experimental prototype achieved 0.99PF, which meets the requirement from EnergyStar. Fig. 14 shows each order of input harmonic currents and it is below the limit from the IEC-61000-3-2 required in LED driving designs. Fig. 15 shows the photo of the experimental prototype.

V. Conclusion

In this paper, an energy buffering LED driver has been proposed to achieve electrolytic capacitor-less and flicker-free design. A 28W experimental prototype had been designed and tested. The 120Hz ripple current is measured to be 7.1% of the DC LED current. It can be further improved with a better circuit design. By altering the way to buffer imbalanced energy, the power conversion loss is reduced as compared with previous electrolytic capacitor-less design, such as active filter and three-port LED drivers. The efficiency of the proposed LED driver is only 1 % lower than a conventional design, which is a significant improvement from previous electrolytic capacitor-less design. The PF and harmonic currents of the proposed LED driver had also been verified in the experimental prototype, and measured results can meet the requirement. Overall, the measured results highly agree with the analysis and demonstrated a very promising LED driving technology.

References

[1] U.S department of energy. LED Lighiting. [online]. Available: https://energy.gov/energysaver/led-lighting [2017, July]

[2] Global LED Lighting Market Size & Share Worth $54.28 Billion by 2022 Zion Market Research [online]. Available:https://globenewswire.com/news-release/2017/01/30/911985/0/en/Global-LED-Lighting-Market-will-reach-USD-54-28-Billion-by-2022-Zion-Market-Research.html [2017, Aug]

[3] B. Lehman, A.J. Wilkins, "Designing to Mitigate Effects of Flicker in LED Lighting: Reducing risks to health and safety," in IEEE Power Electronics Magazine, Vol 1, No 3, September 2014. pp. 18-26.

[4] Illions Capacitor Limited. Aluminum Electrolytic Capacitors Life expectancy [online]. https://www.illinoiscapacitor.com/pdf/Papers/Life%20expectancy%20of%20Aluminum%20electrolytic%20capacitors.pdf [2017, Aug]

[5] X.B. Ruan, B.B. Wang, K. Yao, S. Wang, "Optimum Injected Current Harmonics to Minimize Peak-to-Average Ratio of LED Current for Electrolytic Capacitor-Less AC–DC Drivers" IEEE Transactions on Power Electronics, Vol.26, No.7, 2011, pp.1820,1825

[6] B.B. Wang, X.B. Ruan, K. Yao, M. Xu, "A Method of Reducing the Peak-to-Average Ratio of LED Current for Electrolytic Capacitor-Less AC–DC Drivers," IEEE Transactions on Power Electronics, Vol.25, No.3, March 2010, pp.592,601

[7] C.A. Cheng, C.H. Chang, T.Y. Chung and F.L. Yang, "Design and Implementation of a Single-Stage Driver for Supplying an LED Street-Lighting Module With Power Factor Corrections," IEEE Transactions on Power Electronics, Vol.30, No.2, Feb. 2015, pp.956,966

[8] J. C. W. Lam and P. K. Jain, "Isolated AC/DC Offline High Power Factor Single-Switch LED Drivers Without Electrolytic Capacitors," in IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 3, No. 3, pp. 679-690, September 2015.

[9] J. C. W. Lam and P. K. Jain, "A High Power Factor, Electrolytic Capacitor-Less AC-Input LED Driver Topology With High Frequency Pulsating Output Current," in IEEE Transactions on Power Electronics, Vol. 30, Vo. 2, pp. 943-955, Feburary 2015.

[10] D.Camponogara, D.R.Vargas, M.A.Dalla Costa, J.M.Alonso, J.Garcia and T.Marchesan, "Capacitance reduction with an optimized converter connection applied to LED drivers," in IEEE Transactions on Industrial Electronics, Vol. 62, No.1, pp.184-192, January 2015.

[11] D.Camponogara, G.F.Ferreira, A. Campos, M.A. Dalla Costa and J. Garcia, "Offline LED Driver for Street Lighting With an Optimized Cascade Structure," in IEEE Transactions on Industry Applications, Vol.49, No 6, pp.2437-2443, December 2013.

[12] P. Fang, Y. j. Qiu, H. Wang and Y. F. Liu, "A Single-Stage Primary-Side-Controlled Off-line Flyback LED Driver With Ripple Cancellation," in IEEE Transactions on Power Electronics, vol. 32, no. 6, pp. 4700-4715, June 2017.

[13] Y. Qiu, L. Wang, H. Wang, Y. F. Liu and P. C. Sen, "Bipolar Ripple Cancellation Method to Achieve Single-Stage Electrolytic-Capacitor-Less High-Power LED Driver," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 3, no. 3, pp. 698-713, Sept. 2015.

[14] P. Fang and Y. F. Liu, "Energy Channeling LED Driver Technology to Achieve Flicker-Free Operation With True Single Stage Power Factor Correction," in IEEE Transactions on Power Electronics, vol. 32, no. 5, pp. 3892-3907, May 2017.

[15] S. Wang, X.B. Ruan, K. Yao, S.C. Tan, Y. Yang and Z.H Ye, "A Flicker-Free Electrolytic Capacitor-Less AC–DC LED Driver" IEEE Transactions on Power Electronics, Vol.27, No.11, 2012, pp.4540,4548

[16] Q.C. Hu and R. Zane, "Minimizing Required Energy Storage in Off-Line LED Drivers Based on Series-Input Converter Modules" ,IEEE Transactions on Power Electronics, Vol.26, No.10, 2011, pp.2887,2895

[17] P. T. Krein, R. S. Balog and M. Mirjafari, "Minimum Energy and Capacitance Requirements for Single-Phase Inverters and Rectifiers Using a Ripple Port," in IEEE Transactions on Power Electronics, Vol. 27, No. 11, pp. 4690-4698, November. 2012.

[18] W. Chen and S.Y.R. Hui, "Elimination of an Electrolytic Capacitor in AC/DC Light-Emitting Diode (LED) Driver With High Input Power Factor and Constant Output Current," in IEEE Transactions on Power Electronics, Vol. 27, No. 3, pp. 1598-1607, March 2012.

[19] H. C. Kim, M. C. Choi, S. Kim and D. K. Jeong, "An AC–DC LED Driver With a Two-Parallel Inverted Buck Topology for Reducing the Light Flicker in Lighting Applications to Low-Risk Levels," in IEEE Transactions on Power Electronics, vol. 32, no. 5, pp. 3879-3891, May 2017.

[20] B. White, H. Wang, Y. F. Liu and X. Liu, "An Average Current Modulation Method for Single-Stage LED Drivers With High Power Factor and Zero Low-Frequency Current Ripple," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 3, no. 3, pp. 714-731, Sept. 2015.

[21] M. Chen, Y. Ni, C. Serrano, B. Montgomery, D. Perreault and K. Afridi, "An electrolytic-free offline LED driver with a ceramic-capacitor-based compact SSC energy buffer," 2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, 2014

[22] L. Wang, B. Zhang and D. Qiu, "A Novel Valley-Fill Single-Stage Boost-Forward Converter With Optimized

Performance in Universal-Line Range for Dimmable LED Lighting," in IEEE Transactions on Industrial Electronics, vol. 64, no. 4, pp. 2770-2778, April 2017

[23] H. Ma, J. S. Lai, Q. Feng, W. Yu, C. Zheng and Z. Zhao, "A Novel Valley-Fill SEPIC-Derived Power Supply Without Electrolytic Capacitor for LED Lighting Application," in IEEE Transactions on Power Electronics, vol. 27, no. 6, pp. 3057-3071, June 2012.

[24] H. Ma, J. S. Lai, C. Zheng and P. Sun, "A High-Efficiency Quasi-Single-Stage Bridgeless Electrolytic Capacitor-Free High-Power AC–DC Driver for Supplying Multiple LED Strings in Parallel," in IEEE Transactions on Power Electronics, vol. 31, no. 8, pp. 5825-5836, Aug. 2016

[25] H. Valipour, G. Rezazadeh and M. R. Zolghadri, "Flicker-Free Electrolytic Capacitor-Less Universal Input Offline LED Driver With PFC," in IEEE Transactions on Power Electronics, vol. 31, no. 9, pp. 6553-6561, Sept. 2016.

[26] Richtek. "Single-Stage High Power Factor Flyback for LED Lighting" [online]. May 2014.

[27] Fairchild. "LED Application Design Guide Using Half-Bridge LLC Resonant Converter for 100W Street Lighting" [online]. Nov 2011.

[28] Texas Instrument. "A New Off-Line LED Lighting Driver Solution with Multi-Transformer LLC Control". [online]. Sep 2011.