Power Adapter with Line Voltage Control for USB Power Delivery

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***Abstract*—The demand for high-power-density high-efficiency power adapters is increasing due to the wide adopt of the USB Power Delivery as the charging protocol in consumer electronics. Flyback converters have conventionally prevailed for such applications. To further improve the power density of power adapters, an increase in switching frequency is required. However, this will increase the burden of the EMI filter, and the heat will be difficult to manage as the loss increases when size is reduced. Resonant converters have long been used for high frequency applications due to the easily-implemented soft switching and low current stresses. With the development of faster switching devices and new ferrites, the switching frequency of resonant converters is pushed as high as megahertz with acceptable thermal performance. In this paper, a series resonant converter is combined with the proposed line voltage control circuit to accommodate both the 120 VAC and the 220 VAC lines, as well as the wide output voltage range from 5 V to 20 V required by the USB Power Delivery. In the 60 W prototype, peak 94% efficiency is achieved at 1 MHz operation enabled by a budget MCU.**

Keywords — power adapter; USB PD; power delivery; SRC; series resonant converter; wide voltage; universal AC

I. INTRODUCTION

Technologies associated with power adapters for laptops and cellphones are quickly advancing as new protocols and devices are unveiled. For power at 60 W and below, Flyback converters at below 150 kHz are dominant due to their simple implementation, satisfactory performance and low cost. As the demand increases for compact power adapters [1]–[3], the conventional Flyback is becoming limited due to device size and thermal performance. Further improving the power density will require increasing the switching frequency which consequently requires a larger EMI filter. Additionally, the heat would be difficult to manage because the loss increases significantly while the size is reduced. Although frequency and efficiency improvements can be realized with the active clamp technique [4][5], the cost increases, and approaches that of the half-bridge LLC resonant converter. Resonant converters generally have lower current stress, much easier implementation of soft switching on all switches, and better transformer performance in high frequency and very high frequency (VHF) applications [6]. Thus, a technology shift has been seen in this sector from conventional hard-switching converters operating at 65-130 kHz to (quasi-) resonant converters operating towards megahertz [7].

Within the scope of resonant topologies, LLC converter and series resonant converter (SRC) are the most conventional. Compared to SRC, LLC has a narrower frequency range, smaller inductor and better load regulation. For high current applications, LLC converters have lower turn-off current on the primary switches. At 60 W power, however, SRC also has respectable performance in various aspects. For example, SRC has lower primary current stresses due to the absence of circulating current, as well as lower secondary critical continuous current. The ZVS margin is less of an issue because the turn-off current is near its peak. Also, with the removal of magnetic air gaps and fewer windings, the fringing effect is automatically removed. This allows the SRC converter to use a smaller transformer with less conduction loss. Moreover, SRC is receptive to slow turn-off transient (dv/dt), enabling silicon to operate at megahertz [8][9].

For the most part, resonant converters are not renowned for having wide voltage regulation range. Designing the converter for wide voltage range will sacrifice the high efficiency. A great challenge has been placed for resonant converters due to the wide output voltage range from 5 V to 20 V required by the USB PD [10]. Table I shows the power profile for up to 60 W, below which there is no power factor correction requirement [11]. Taking into

Table I. POWER PROFILE OF USB PD UP TO 60 W

	5 V	9 V	15 V	20 V
15 W	3 A	N/A	N/A	N/A
27 W	3 A	3 A	N/A	N/A
45 W	3 A	3 A	3 A	N/A
60 W	3 A	3 A	3 A	3 A

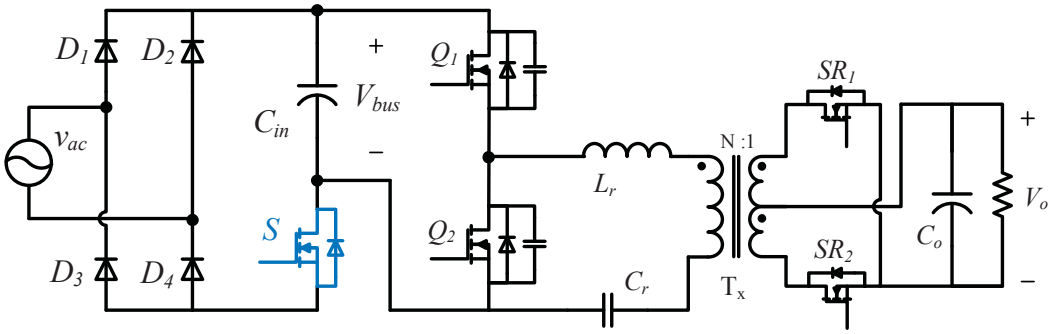


Fig. 1. SRC converter with line voltage control circuit

consideration of universal AC input of 100 - 240 VAC, it only increases the design challenge for the DC-DC stage. Even with Flyback converter, optimization is difficult.

This paper focuses on improving the power adapter performance by controlling the AC voltage, so to further control the input voltage range of the DC-DC stage. An additional switch is used to limit the input voltage within a specified maximum value. In this way, the DC input voltage variation is significantly reduced, despite of the universal AC input as wide as 100Vac - 240Vac commonly seen in such applications. Additionally, the input voltage range can be adjusted based on the output voltage ladders, so to reduce the design burden of the DC-DC stage. Besides, the size of the input capacitor can also be significantly reduced due to the much reduced voltage rating requirement. With the proposed line voltage control method, the design of the converter only needs to be optimized for a narrow voltage range. Thus, high performance is expected for the power stage, and more high-efficient DC-DC solutions are enabled for such applications. In this paper, SRC is used as an example for DC-DC stage because it maximizes the above mentioned benefits. In practice, LLC converters and Flyback *etc*. can also be applied.

II. Operation Principle of Line Voltage Control

Fig. 1 shows a half-bridge SRC with the line voltage control circuit, in which the switch S is added to the conventional full bridge rectifier. S should be connected in such a way that the rectified line current should not charge the capacitor C_{in} through the body diode. In other words, the line power is transferred to C_{in} and the load side only when S is turned on. When S is turned off, the line power is disconnected. By the turn off instant, the voltage on capacitor C_{in} reaches its maximum.

Fig. 2 shows the critical control logic and key waveforms of the line control circuit. V_{bus} is the voltage on the input capacitor C_{in}, which is also the bus voltage for the following DC-DC converter. $|v_{ac}|$ is the absolute value of the AC input. i_S is the current through the switch S. G_s is the gate signal of the switch S. In this paper, the turn-on timing is synchronized with the AC voltage zero crossing point, although in practice the turn-on timing can be around the zero crossing point as long as $|v_{ac}|$ is lower than V_{bus}. In the case of a late turn-on happens, an inrush current will be seen on the capacitor, which is not very desired. The operation and control are explained in details as follows.

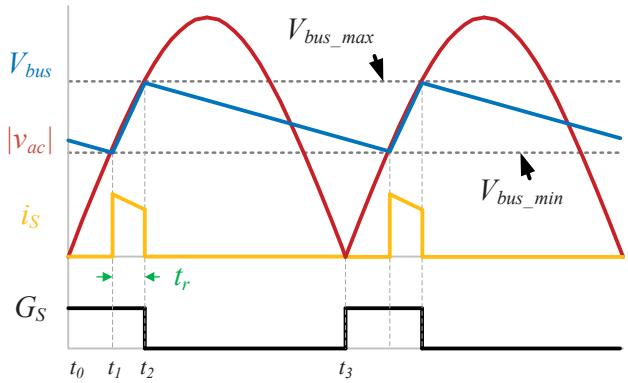


Fig. 2. Key waveforms of line voltage control circuit

State [t_0, t_1]: As shown in Fig. 3, although S is turned on at t_0, D_1 and D_4 are still reversely biased and will not start to conduct until t_1, at which time v_{ac} becomes higher than V_{bus}. From t_0 to t_1, C_{in} will continuously discharge to power the load.

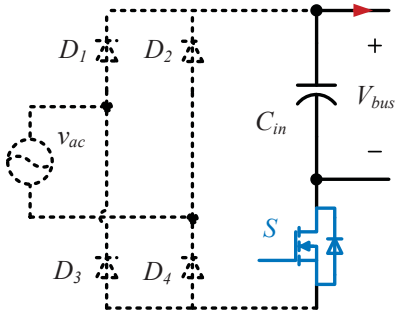


Fig. 3. Line voltage circuit operation at [t_0, t_1]

State [t_1, t_2]: As shown in Fig. 4, D_1 and D_4 start to conduct at t_1. The capacitor voltage will keep increasing with the $|v_{ac}|$. At t_2, the bus voltage reaches the pre-determined maximum value V_{bus_max} and S is then turned off. It should be noted that the voltage rising time t_r (period between t_1 and t_2) will be different for 120 VAC and 220 VAC lines. Thus, the i_S will also be different depending on the rising time. If the V_{bus_max} is higher than the peak value of v_{ac} (saying V_{bus_max} is 170 V, and v_{ac} is 100 VAC with peak at 141 V), then S will always remain turned on and the operation will be the same as a conventional full bridge rectifier.

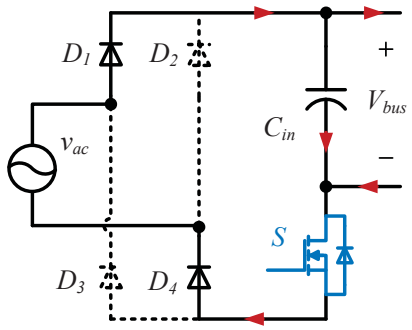


Fig. 4. Line voltage circuit operation at *[t_1, t_2]*

State [t_2, t_3]: As shown in Fig. 5, after S is turned off at t_2, the AC power is disconnected, and the load is powered by the capacitor C_{in} alone. During t_2 to t_3, the diode bridge remains as forward-biased while the body diode of S is reverse-biased. The peak voltage stress on S, which equals to the difference between $|v_{ac}|$ and V_{bus_max}, is reached sometime after the v_{ac} reaches its peak. In practice, the voltage stress varies based on the V_{bus_max} and the C_{in} value. In a typical design, the peak voltage stress is between 150 V to 200 V. However, a 500 V rated MOSFET should be used, because S should withstand the peak line voltage (340V in worst scenario) during power up.

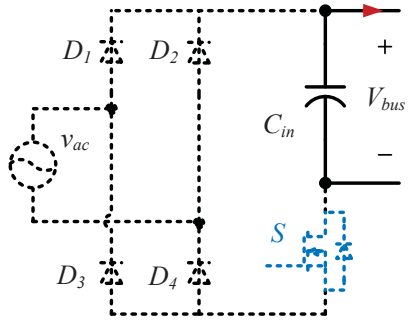


Fig. 5. Line voltage circuit operation at *[t_2, t_3]*

III. Performance Analysis

Fig. 6 shows the voltage rising time t_r and the current stress in S for different AC voltages. The results are from 20 V/60 W output, which is the worst case in terms of current stress in S. The V_{bus_max} is set at 170 V. Generally, the 120 VAC line has a longer rising time than the 220 VAC line so that the current in S is lower at 120 VAC. For 100 VAC and 110 VAC, the actual V_{bus_max} is less than 170 V and the average bus voltage is lower than the other cases. Therefore, the current is higher even if the conducting time is longest.

From the loss perspective, the diode bridge will have the same loss for different AC input. Although the current increases with the AC voltage, the conducting time is reduced. This results in the same total amount of charge going through the diodes. For the MOSFET S and capacitor C_{in}, the losses will increase at higher AC voltage. Because these are resistive losses and the RMS current is higher at high input.

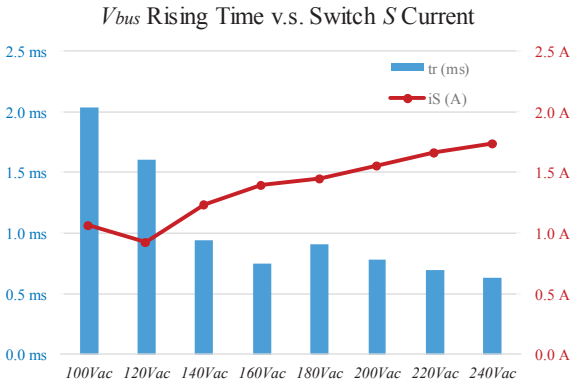


Fig. 6. Rising time and current stress for different AC voltages

As the C_{in} voltage is clamped below 170 V, its size can be greatly reduced by using 200 V rated capacitors. This is significant because for power adapters at such power level, the electrolytic capacitor can occupy as much as 1/4 of the entire converter. Fig. 7 compares the size of 200 V and 400 V rated C_{in} used in conventional diode bridge rectifiers. Generally, more than half of the size is saved.

It is also observed that as the capacitor value increases, the minimum bus voltage is also increased. This will have impact on the SRC design, as the resonant point and transformer turns ratio are designed based on the V_{bus_min}. On one hand, a higher V_{bus_min} is preferred so that a higher turns ratio can be used. This will help reduce the current stress in the resonant tank. On the other hand, a small V_{bus_min} is beneficial in terms of the overall size. In this case, 82 µF is selected since it achieves good trade-off between the V_{bus_min} and size.

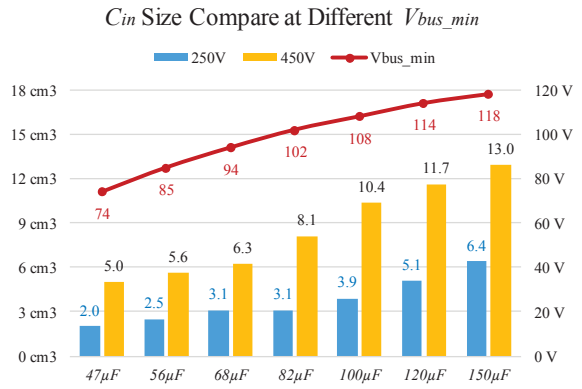


Fig. 7. Reduced C_{in} size for different V_{bus_min} design

If the V_{bus} remains the same for all output conditions, the SRC gain should be designed to cover at least 4 times, so to accommodate output voltages from 5 V to 20 V. This is not desirable as the wide gain will lower the efficiency. The AC control method can be used to reduce the SRC gain range and improve its design. As shown in Fig. 8, once the 20 V/60 W design is final, the SRC converter can also achieve operations at 5 V, 9 V *etc.* simply by lowering bus voltage.

For example, with 82 µF C_{in} and V_{bus_max} at 170 V, the V_{bus_min} is 110 V for 20 V/3 A conduction. The transformer turns ration is selected at 7:3, so that V_{bus} for the SRC at resonance is designed at around 90 V (20 V*(7/3)*2 = 93 V) in this case to allow for some ZVS margin for 110 V operation. Then, for 5 V output, at the resonant frequency, the corresponding input voltage should be 23 V (5 V/20 V*90 V). The V_{bus} voltage can be selected as, for instance, 55 V to 95 V. Then the ratio-to-resonance is close to that of the 20 V output. The objective is to have the same gain design of SRC for all output voltages, so that the switching frequency and operation is same throughout all output conditions.

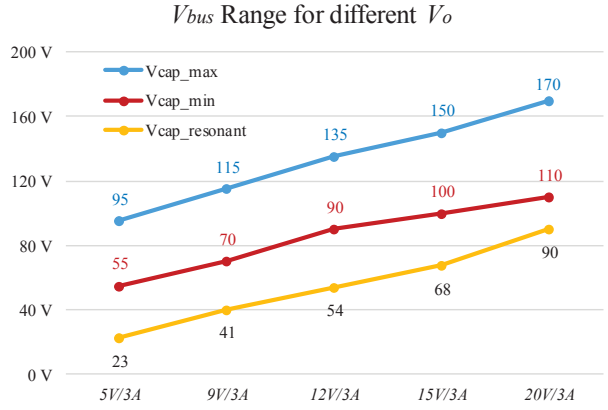


Fig. 8. V_{bus} range setting for 5 V – 20 V for PD requirement

IV. Experiment Results

To verify the feasibility and demonstrate the advantages of the proposed line voltage control method, a 60 W prototype has been built. The specifications and the parameter designs are shown in Table II.

Table II. Specifications and Designs of Line Power Control Method

Input AC voltage	100VAC – 240VAC
Output voltage	5V, 9V, 12V, 15V, 20V
Max output current / power	3A / 60 W
Input capacitor C_{in}	82 µF / 200V
Bus Voltage V_{bus_max}	170V @ 20V Vo 150V @ 15V Vo 135V @ 12V Vo 115V @ 9V Vo 95V @ 5V Vo
Auxiliary MOSFET	STF43N60DM2 (85mOhms)
HB MOSFET	IPB320N20N3 G (32mOhms)
Switching frequency	660 kHz-1000 kHz
Resonant inductor L_r	8 µH (13T RM6)
Resonant capacitor C_r	8 nF
Transformer T_x	7:3:3 (RM6)

For 20 V output voltage, the maximum voltage on C_{in} is designed as 170 V, at which the switch is turned off. When outputting 60 W of power, the capacitor voltage will reach its minimum, which is selected at 100 V in this design. With these two boundary selected, a 200 V rated capacitor of 82 µF can be used. As 20 V/60 W is the worst case in terms of power, the selected capacitor value will only be sufficient for other output voltage (5V, 9V, 12V and 15V) and power conditions. The sizes of 82 µF capacitor at 200 V rating and 400 V rating of Nichicon UCY series are compared in Fig. 9. It is observed that the 200 V capacitor occupies less than 40% of the space required by a 400 V capacitor. This greatly helps achieve the goal of reducing the total converter size.

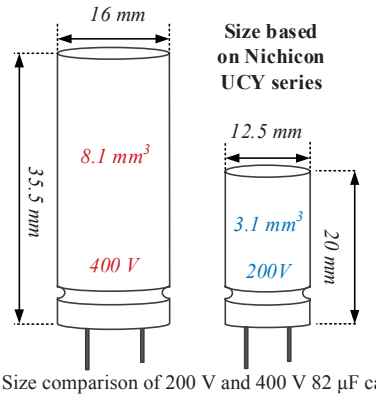
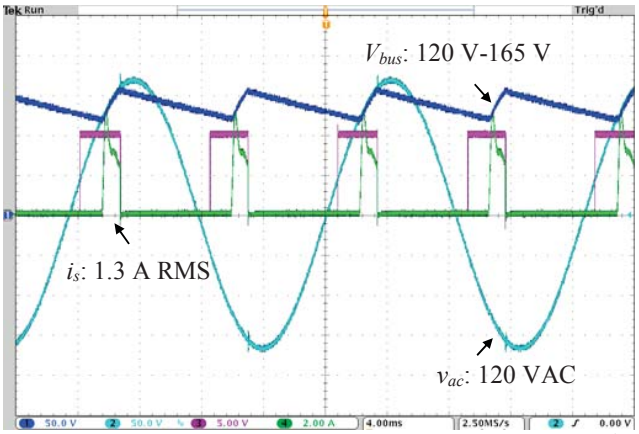


Fig. 9. Size comparison of 200 V and 400 V 82 µF capacitor

For the SRC converter design, as the input voltage is limited below 170 V, 200 V rated MOSFETs are used, which have much reduced R_{dson} and conduction loss as compared to those 600 V rated counterparts. The transformer turns ratio is selected as 7:3:3 as a trade-off between the current stress and the input capacitor size. If a small ratio is used the resonant tank will have high current, while a large ratio will call for a high minimum capacitor voltage and a larger capacitor value. Besides, to minimize the size of the magnetics, the switching frequency is selected at around megahertz.

Fig. 10 shows the waveform of the line voltage control circuit under 120 VAC / 60 Hz input and 60 W power. Channel 2 shows the bus voltage controlled below 165 V with a minimum value at 120 V. The rise time is around 1.2 ms. And the RMS current in the auxiliary switch is measured as 1.3 A.

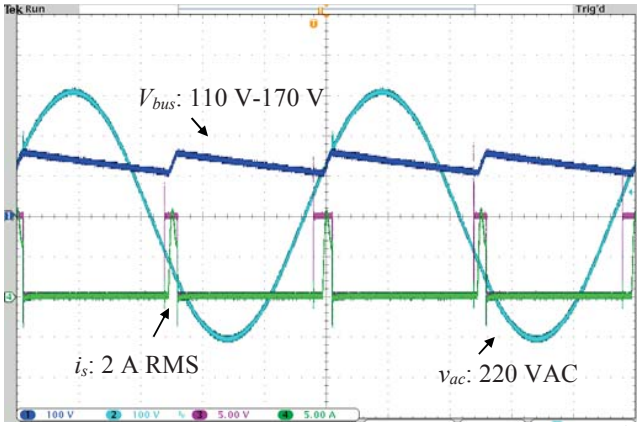


Ch1: V_{bus} (50 V/div); Ch2: v_{ac} (50 V/div); Ch3: G_s (5 V/div); Ch4: i_s (2 A/div)

Fig. 10. Line voltage control waveform for 120 VAC and 60 W load

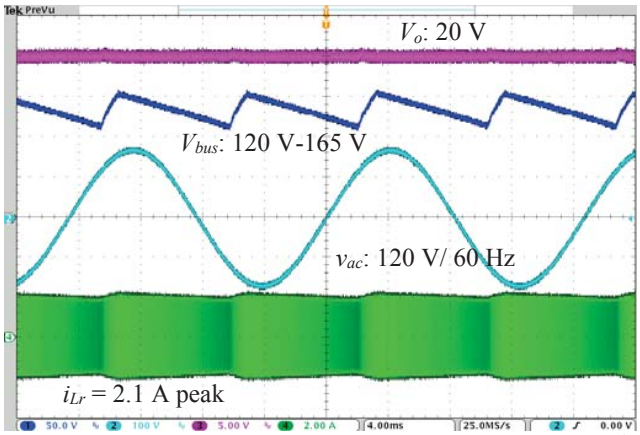
Fig. 11 shows the waveform of the line voltage control circuit under 220 VAC / 50 Hz input and 60 W power. The bus voltage is controlled below 170 V with a minimum value at 110 V. The rise time is around 0.7 ms. The RMS current in the auxiliary switch is 2 A.

Fig. 12 - Fig. 21 shows the SRC waveform at 20 V/3 A, 15 V/3 A, 12 V/3 A, 9 V/3 A, and 5 V/3 A output under 120 VAC and 220 VAC, respectively. For all cases the resonant current peaks at around 2.1 A, because the SRC converter behaves like current source and the switching frequency is design to be same for all output conditions. For most cases the output voltage is well regulated at the desired level. The output of 5 V is the worst case in terms of regulation, because the rising time of the input voltage is very short, and the dv/dt is high.



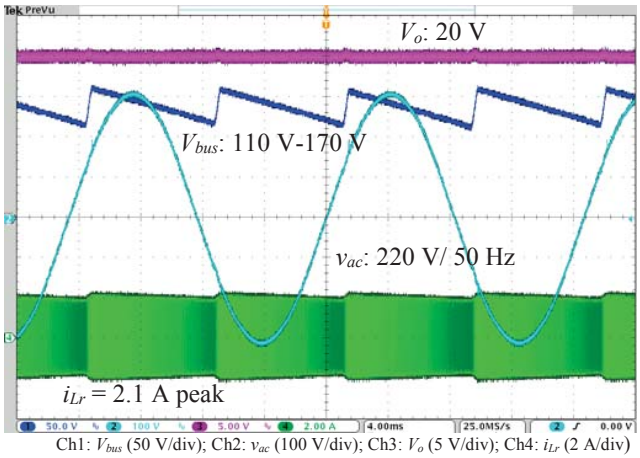
Ch1: V_{bus} (100 V/div); Ch2: v_{ac} (100 V/div); Ch3: G_s (5 V/div); Ch4: i_s (5 A/div)

Fig. 11. Line voltage control waveform for 220 VAC and 60 W load



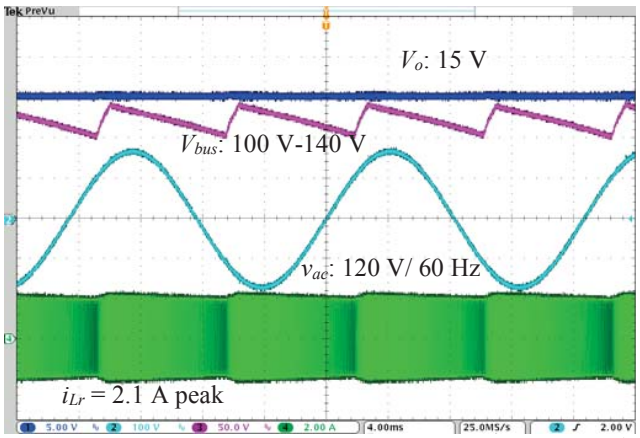
Ch1: V_{bus} (50 V/div); Ch2: v_{ac} (100 V/div); Ch3: V_o (5 V/div); Ch4: i_{Lr} (2 A/div)

Fig. 12. SRC waveform regulated at 20 V / 3 A output for 120 VAC



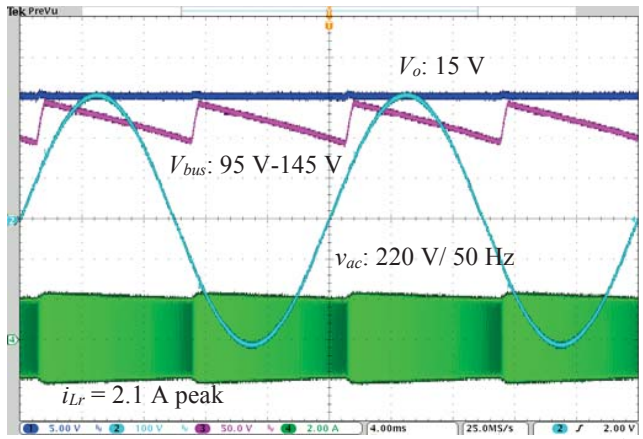
Ch1: V_{bus} (50 V/div); Ch2: v_{ac} (100 V/div); Ch3: V_o (5 V/div); Ch4: i_{Lr} (2 A/div)

Fig. 13. SRC waveform regulated at 20 V / 3 A output for 220 VAC



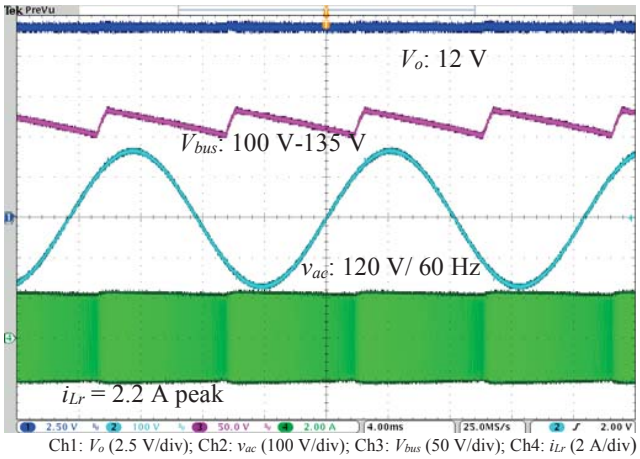
Ch1: V_o (5 V/div); Ch2: v_{ac} (100 V/div); Ch3: V_{bus} (50 V/div); Ch4: i_{Lr} (2 A/div)

Fig. 14. SRC waveform regulated at 15 V / 3 A output for 120 VAC



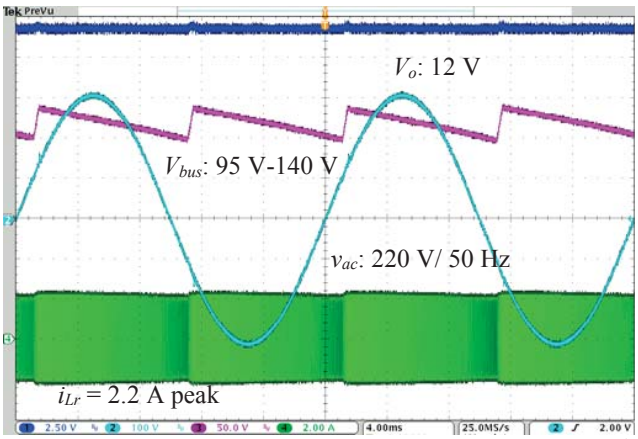
Ch1: V_o (5 V/div); Ch2: v_{ac} (100 V/div); Ch3: V_{bus} (50 V/div); Ch4: i_{Lr} (2 A/div)

Fig. 15. SRC waveform regulated at 15 V / 3 A output for 220 VAC



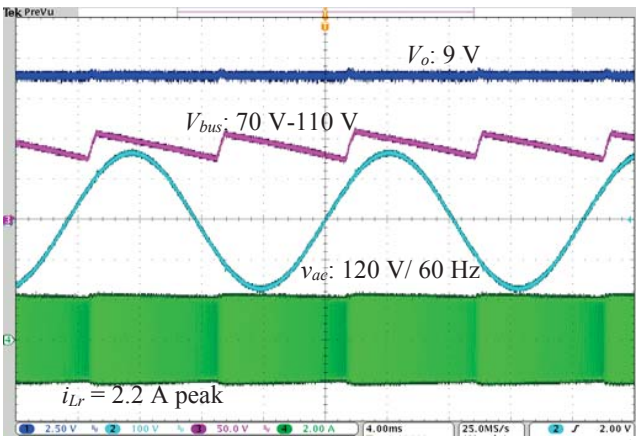
Ch1: V_o (2.5 V/div); Ch2: v_{ac} (100 V/div); Ch3: V_{bus} (50 V/div); Ch4: i_{Lr} (2 A/div)

Fig. 16. SRC waveform regulated at 12 V / 3 A output for 120 VAC



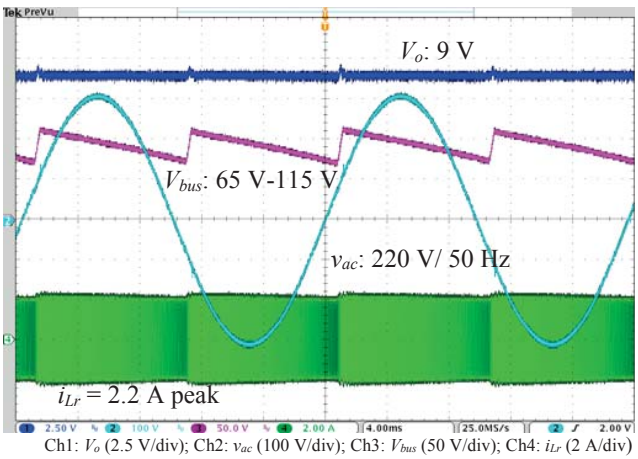
Ch1: V_o (2.5 V/div); Ch2: v_{ac} (100 V/div); Ch3: V_{bus} (50 V/div); Ch4: i_{Lr} (2 A/div)

Fig. 17. SRC waveform regulated at 12 V / 3 A output for 220 VAC



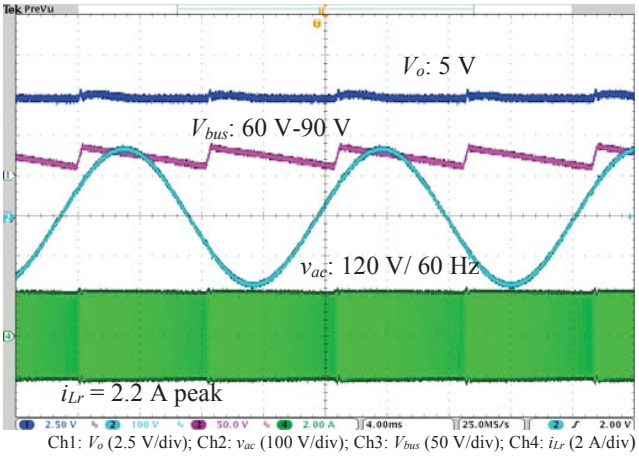
Ch1: V_o (2.5 V/div); Ch2: v_{ac} (100 V/div); Ch3: V_{bus} (50 V/div); Ch4: i_{Lr} (2 A/div)

Fig. 18. SRC waveform regulated at 9 V / 3 A output for 120 VAC



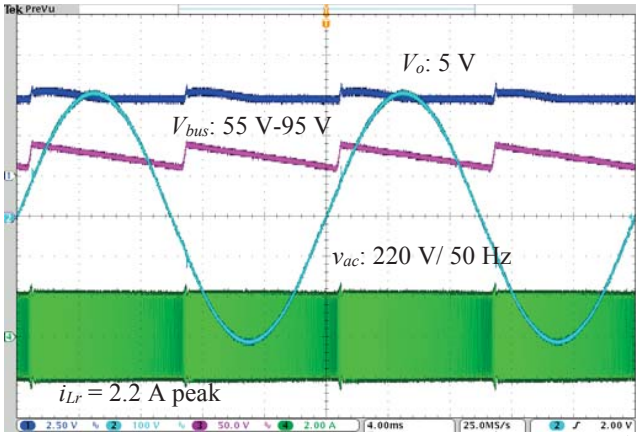
Ch1: V_o (2.5 V/div); Ch2: v_{ac} (100 V/div); Ch3: V_{bus} (50 V/div); Ch4: i_{Lr} (2 A/div)

Fig. 19. SRC waveform regulated at 9 V / 3 A output for 220 VAC



Ch1: V_o (2.5 V/div); Ch2: v_{ac} (100 V/div); Ch3: V_{bus} (50 V/div); Ch4: i_{Lr} (2 A/div)

Fig. 20. SRC waveform regulated at 5 V / 3 A output for 120 VAC



Ch1: V_o (2.5 V/div); Ch2: v_{ac} (100 V/div); Ch3: V_{bus} (50 V/div); Ch4: i_{Lr} (2 A/div)

Fig. 21. SRC waveform regulated at 5 V / 3 A output for 220 VAC

The efficiency at different output are measured and shown in Fig. 22. Generally, the 220 VAC efficiency is lower because of the higher losses in the line voltage control circuit.

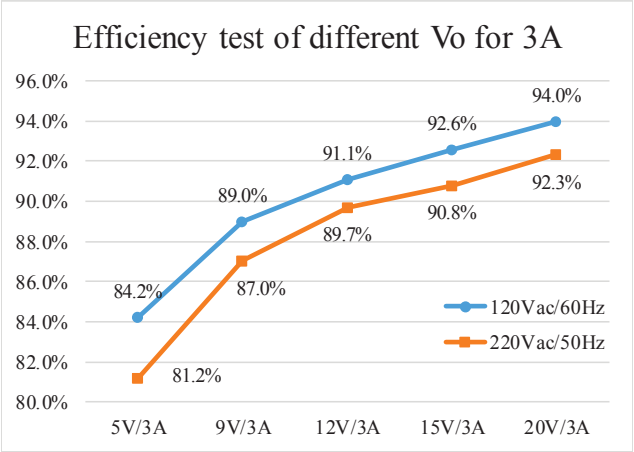


Fig. 22. Efficiency test at different output voltages

V. Conclusion

In this paper, a line voltage control method was proposed to control the input voltage range for the DC-DC stage within a desired range. As compared to a conventional diode bridge rectifier, only one switch is added. The new circuit and the control method result in a narrower gain requirement when designing the DC-DC converter over the universal AC input. Besides, the capacitor voltage rating can be significantly reduced, so the size of the converter can be reduced significantly. For USB-PD applications, where the output voltage varies from 5V to 20V, the design of the DC-DC stage does not need to compromise since the input voltage can be adjusted based on the actual output voltage. A 60 W prototype was built with the SRC converter operating at 1 MHz, and the test results justified the feasibility and good performance of both the line control circuit and the SRC converter. Peak 94% efficiency was achieved with a budget MCU.

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