4 kW Auxiliary Power Module for Electric Vehicles Utilizing a Dual-Phase LLC DC-DC Converter

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***Abstract*— This paper introduces a novel resonant tank design approach for dual-phase LLC DC-DC resonant converters in Auxiliary Power Module (APM) applications. The proposed design ensures that the impedance of one phase is consistently either larger or smaller than that of the other phase across a wide range of input and output voltages. As a result, only a single Switch-Controlled Capacitor (SCC) circuit is needed to achieve current sharing across the load range. This reduces system complexity and implementation costs without compromising efficiency or current-sharing performance. The design procedure is detailed for both phases, and experimental results from a full-scale, GaN-based 4 kW APM validate the effectiveness of the proposed approach in maintaining current sharing across varying input/output voltages and load conditions. Furthermore, flat efficiency curves with calculated average of more than 95.5% were achieved for different battery voltages, with a peak efficiency surpassing 96.3%.**

Keywords—Dual-phase LLC, DC-DC Resonant Converter, SCC-LLC, Auxiliary Power Module (APM), Electric Vehicle (EV).

I. INTRODUCTION

The High-Voltage (HV) to Low-Voltage (LV) DC-DC converter in Electric Vehicles (EVs) supports the 12 V battery from the HV battery to supply on-board auxiliary loads. One of the key requirements for such a system is to accommodate the larger demands of future EVs, which may require a maximum load of approximately 4 kW to 5 kW. The most significant challenge in achieving improved performance for Auxiliary Power Modules (APMs) lies in the wide input and output voltage range, due to the varying operating voltage ranges of HV and LV batteries based on their State-of-Charge (SoC) [1].

The main topologies that can meet the requirements for an APM are typically based on full-bridge configurations. The Phase-Shifted Full-Bridge (PSFB) is a topology that employs a fixed switching frequency and variable phase shift control, enabling the achievement of soft switching [2]. Proper implementation of PSFB can realize ZVS at the turn-on instant by utilizing leakage/stray inductances and the parasitic capacitances of the switching devices [3]. However, some drawbacks of the PSFB topology include the loss of ZVS under light load conditions, the load dependency of the ZVS delay time, and higher circulating and RMS currents.

When full-bridge active switch rectification is used in a FSFB converter, the topology is referred to as a Dual Active Bridge (DAB) converter [4]. The DAB is very popular in APM applications due to its ability to achieve ZVS, flexibility of control, and high efficiency [5] and [6]. However, a drawback of the DAB is the loss of ZVS across wide operating voltage and load ranges, which can deteriorate the converter's efficiency and power density. The three-phase DAB converter is another topology suitable for high-power applications with high power density requirements [7], This configuration inherently reduces current ripple, requiring smaller filtering on both sides, and offers fault tolerance capabilities, which are advantageous for automotive applications. Despite the advantages of DAB converters, the switch turn-off current in both single-phase and three-phase DAB topologies undergoes hard switching, leading to significant losses, particularly in the LV side switches, and poses severe EMI challenges.

In an approach to reduce turn-off current of LV side switches, a two-stage topology is proposed in [8], utilizing an interleaved buck in the front followed by a DC transformer (DCX) converter, where wide voltage adjustments occur in the first stage, and DCX operates as an LLC converter at the resonant frequency. This approach eliminates turn-on/-off losses of the LV side switches via Zero Current Switching (ZCS). However, while this two-stage approach reduces switching losses in the DCX stage, it introduces additional conduction losses, which can negatively impact overall efficiency and power density. To mitigate conduction losses and improve the efficiency of the LLC converter across a wide range of operating voltages, various hybrid control modes, including Discontinuous Conduction Mode (DCM), Continuous Conduction Mode (CCM) and Boundary Conduction Mode (BCM), are explored in [9].

Another aspect of achieving high-efficiency performance is the minimization of conduction losses. A common approach is to distribute conduction losses across multiple components by implementing a parallel converter design. However, resonant converters can face challenges with unbalanced loading and current sharing due to resonant tank component tolerances, even with slight impedance mismatches. In [10], a double-phase LLC converter is proposed for APM applications with dual control

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loops to balance the current. However, this approach results in two different switching frequencies, creating a variable beat frequency with fluctuations that can deteriorate the converter's performance. In [11], dual duty cycle control is used in a two-phase LLC converter for DCX applications to balance the load between phases while maintaining the same switching frequency for both phases. Additionally, passive current-sharing methods have been implemented in multi-phase LLC converters [12]. Despite these efforts, none of these methods can achieve accurate current sharing over a wide voltage and load range with large component tolerances. Moreover, interleaving to reduce current ripple and filtering requirements is not possible in most of these solutions.

In [13], a Switch-Controlled Capacitor (SCC) was incorporated in series with the resonant capacitors of both phases in an interleaved LCLC converter. This configuration matched the impedance of each phase at every switching frequency, ensuring effective load sharing. The method is both accurate and reliable across the entire load range, as it leverages active balancing based on sensed currents. In [14], a multi-phase LLC converter is proposed for APM applications, employing SCC circuits on all phases. The SCC circuits actively tune the impedance of the LLC tanks to ensure that the resonant tank impedances match across all phases. This approach mitigates many of the challenges associated with parallel LLC converters while effectively balancing load sharing between phases under all operating conditions. However, a notable drawback of the three-phase APM topology described in [14] is the increased cost associated with adding SCC components to each phase, which represents a significant barrier in the automotive industry.

In this paper, a novel resonant tank design is proposed for dual-phase LLC DC-DC converters. The design ensures that the voltage gains of the parallel phases are separate without any intersection over the frequency range, meaning that the voltage gain of one phase is always either larger or smaller than that of the other phase. This approach enables current sharing over a wide operating voltage range using only one SCC circuit, reducing cost and complexity while enhancing reliability. However, special care should be taken into the design of the resonant tanks to be able to achieve the latter, which will be described in the following sections.

II. The Proposed Dual-Phase LLC DC-DC Converter

As mentioned earlier, the impedances of the resonant tanks in multi-phase resonant converters are sensitive to component tolerances, which directly affect the current distribution between the phases. A phase with a resonant tank of higher impedance will carry a smaller share of the output current. On the other hand, an SCC circuit can only reduce the equivalent resonant capacitance compared to its original value. Therefore, the SCC circuit is limited to increasing the load current share in a given phase. Fig. 1 illustrates the proposed two-phase LLC converter with one SCC circuit on phase 2. It is crucial in the design procedure of the proposed converter to make sure that when the SCC circuit is removed, phase 2 always carries less output current, and when the SCC circuit is operating, the output current of phase 2 can be increased to achieve a balanced current sharing in every operating point. For the sake of manufacturing convenience, the magnetics are built with the same values (i.e., $L_{r1} \approx L_{r2}$ and $L_{m1} \approx L_{m2}$) and only the resonant capacitance of phase 2 is chosen to be larger than the resonant capacitance of phase 1 (i.e., $C_{r2} > C_{r1}$).

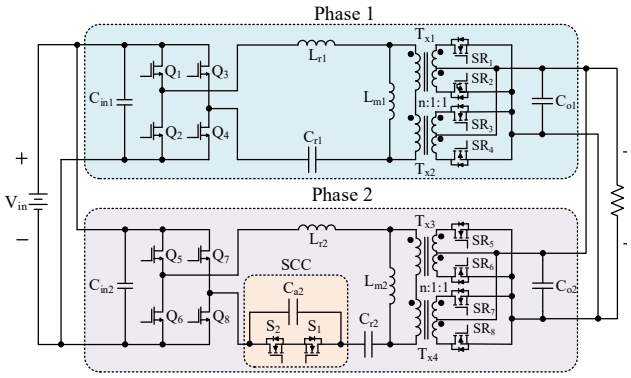


Fig. 1. The proposed dual-phase LLC DC-DC converter.

The first step in the design is the selection of the transformer turn ratio and then the resonant tank parameters of phase 1 for the half-load operation. As mentioned before, the resonant tank of phase 2 can be designed such that the impedance of phase 2 with SCC is always smaller than phase 1 over the whole operation conditions. Then, the SCC capacitor on phase 2 (i.e., C_{a2}) should be designed such that the impedance matching can be achieved based on the predefined component tolerances. The detailed requirement and design procedure of the proposed converter will be provided in the following of this section.

The design requirements of the DC-DC converter for EV APM are outlined in the following: the desired input voltage range is 250 V to 475 V, the output voltage range is 9 V to 16 V. The rated output continuous current is available through 320V to 450V input voltage range for 9 V to 14 V output voltage range, and from 14 V to 16 V output voltage range the output current derates to keep the output power constant at 4 kW. It should be mentioned that for the input voltage range below 320 V and above 450 V a linear derating can be implemented from 4 kW to around zero watts. The derating starts from 285 A for the output voltage of 9 V to 14 V, and it starts from 245 A for the output voltage of 16 V. It should be mentioned that when the output voltage varies between 14 V to 16 V, the output current is restricted by the rated output power. The nominal operation condition is with 320 V input voltage and 14 V output voltage at 285 A load current.

In this design, an operating frequency range between 200 kHz to 500 kHz is considered for the resonant converter to take advantage of passive component miniaturization. Moreover, 650 V GaN switches have been considered for the HV side switching bridge of each phase for maximum performance improvement over the operating range.

The turn ratio of the transformer is determined the same as that of the conventional design approaches. As it is desired to keep most of the operation range below the series resonant frequency (i.e., f_r) to achieve ZCS, the resonant frequency where the voltage gain of the LLC tank is unity should be set for the maximum input voltage and minimum output voltage. Hence, the transformer turn ratio can be found from

$$n = N_p/N_s = V_{in\_max}/V_{o\_min} \quad (1)$$

where N_p and N_s are the transformer's primary and secondary number of turns.

As the input and output voltage range of the EV APM are too wide and we want to minimize the circulating current at the primary side of the transformers, we design the transformer turn ratio for the gain of 0.9 instead of 1 meaning that the switching frequency goes above resonant to meet highest input and lowest output voltage condition. With 450 V maximum input and 9 V minimum output, the equivalent transformer turn ratio should be 0.9 × (450/9) = 45. It should be mentioned that in high current applications it is usually desired to use two or more center tap transformers with series connected primary and parallel connected secondary so the large output current will be distributed as well as the conduction losses. As we want to use two center-tapped transformers in each phase, we select the final turn ratio to be 44 and each transformer has a turn ratio of n:1:1 = 22:1:1. In the next section, the resonant tank design of the phase without SCC is provided first (i.e., phase 1), and then the resonant tank design of the phase with an SCC circuit is provided (i.e., phase 2).

III. Design Consideration for the Proposed Dual-Phase LLC DC-DC Converter

A. Design of the Resonant Components in the Phase Without an SCC Circuit

In phase 1, the designed parameters include L_{r1}, C_{r1}, and L_{m1}. The parameters are designed the same as conventional LLC converters. The design objective is to meet the desired frequency range and all the input/output voltage and load regulations and at the same time reduce the circuiting current at the primary side of the transformers.

The worst-case scenario for the voltage gain requirement of the LLC tank happens with the highest load condition at the highest gain. The highest gain within the normal operating condition is for 320 V input to 16 V output and the hardest voltage gain to achieve is for the nominal operating condition with the highest load. The minimum voltage gain condition is for 450 V input to 9 V output and 140 A load. Hence, the following corner conditions are listed below for half of the rated power of the EV APM:

(1) The maximum voltage Gain = 44 × 16 / 320 = 2.2 for 320 V input, 16 V output, and 122.5 A load.

(2) The worst-case scenario with Gain = 44 × 14 / 320 = 1.93 for 320V input, 14 V output, and 140 A load.

(3) The minimum voltage Gain = 44 × 9 / 450 = 0.88 for 450 V input, 9 V output, and 140 A load.

The design is based on the well-known First Harmonic Approximation (FHA) method, and then the parameters need to be fine-tuned based on computer simulation results to consider the effect of higher-order harmonics. It should be mentioned that the voltage gain found from FHA is lower than the actual gain for the switching frequencies far away from the resonant frequency. In this design, the desired resonant frequency is between 450 kHz to 500 kHz. A relatively small quality factor

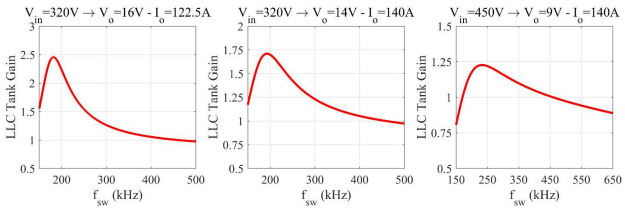


Fig. 2. The plot of voltage gain versus switching frequency at different operating conditions.

(i.e., Q = 0.3) is considered for the worst-case scenario, as a wide input/output voltage range and load range need to be accommodated. Moreover, the circulating currents can be reduced by using a large inductance ratio. Hence, a relatively large inductance ratio is considered in the design (i.e., L_m/L_r=6). The final resonant tank parameters of phase 1 are listed in TABLE I. Fig. 2 illustrates the voltage again curves for different operating conditions. As can be observed the voltage gain of 2.2 is achievable for the first case (left curve) and the voltage gain of 0.88 is also achievable for the third case (right curve). As mentioned before, the hardest gain is for the nominal condition at rated power that is shown in the middle curve of Fig. 2. Although the required 1.93 voltage gain is not achieved with this design using FHA, the simulation results show that the achievable voltage gain using the designed resonant parameters is more than 1.93.

TABLE I. Parameters of Phase 1 of the Proposed Converter

Parameters	Values
L_r inductance	15 µH
L_m inductance	90 µH
C_r capacitance	8 nF
Transformer turn ratio (n:1:1)	22:1:1

B. Design of the Resonant Components in the Phase With an SCC Circuit

In phase 2, the magnetics are identical to phase 1 (i.e., L_{r2} = L_{r1} and L_{m2} = L_{m1}), and hence only the resonant capacitance C_{r2} and the SCC capacitance C_{a2} need to be designed. The design criteria are such that the voltage gain of phase 2 is kept below the voltage gain of phase 1 over the switching frequency range in all operating conditions. Both capacitances are designed based on the operation principles of the SCC circuit.

By modulating the SCC switches, the equivalent resonant capacitance in phase 2 is modified, which alters the impedance of phase 2. When the SCC modulation angle (i.e., α) is a certain value between the minimum and the maximum, the impedance of phase 1 matches that of phase 2, and current sharing is achieved. If α increases, the impedances of phase 2 increase, and phase 2 carry smaller currents. On the contrary, if α decreases, the impedances of phase 2 decrease, and phase 2 carry larger currents. Thus, the design criteria can be summarized as follows:

(1) When α is maximum, in any components' tolerances and operation points, phase 2 carries less current than phase 1.

(2) When α is minimum, in any components' tolerances and operation points, phase 2 carries more current than phase 1.

The components' tolerances are the main reason causing impedances unmatched and current unbalancing, which is compensated by the SCC circuit. In this design, +/-5% tolerances for all the resonant elements and the SCC capacitor are considered. The two design criteria mentioned above can be expressed by

$$I_{o2}\left(M, f_{sw}, L_{m2}, L_{r2}, C_{r-eq(\alpha=max)}\right) < I_{o1}(M, f_{sw}, L_{m1}, L_{r1}, C_{r1}) \quad (2)$$

$$I_{o2}\left(M, f_{sw}, L_{m2}, L_{r2}, C_{r-eq(\alpha=min)}\right) > I_{o1}(M, f_{sw}, L_{m1}, L_{r1}, C_{r1}) \quad (3)$$

where I_{o1} and I_{o2} are the output currents of phase 1 and phase 2, respectively. M is the LLC tank voltage gain, f_{sw} is the switching frequency, $C_{r-eq(\alpha=max)}$ and $C_{r-eq(\alpha=min)}$ are the equivalent capacitances when the SCC modulation angles are maximum and minimum, respectively. Note that M and f_{sw} indicate different operating conditions. The equivalent resonant capacitance C_{r-eq} satisfies,

$$\frac{C_{a2}C_{r2}}{C_{a2}+C_{r2}} < C_{r-eq(\alpha=min)} < C_{r-eq} < C_{r-eq(\alpha=max)} < C_{r2} \quad (4)$$

When components' tolerances are considered, the following inequations can be found

$$I_{o1}(M, f_{sw}, L_{m1}, L_{r1}, C_{r1}) \leq I_{o1}\left(M, f_{sw}, L_{m1(min)}, L_{r1(min)}, C_{r1(min)}\right) \quad (5)$$

$$I_{o1}(M, f_{sw}, L_{m1}, L_{r1}, C_{r1}) \geq I_{o1}\left(M, f_{sw}, L_{m1(max)}, L_{r1(max)}, C_{r1(max)}\right) \quad (6)$$

$$I_{o2}\left(M, f_{sw}, L_{m2}, L_{r2}, C_{r-eq(\alpha=max)}\right) \leq I_{o2}\left(M, f_{sw}, L_{m2(min)}, L_{r2(min)}, C_{r-eq(\alpha=max, C_{a2}=min, C_{r2}=min)}\right) \quad (7)$$

$$I_{o2}\left(M, f_{sw}, L_{m2}, L_{r2}, C_{r-eq(\alpha=min)}\right) \geq I_{o2}\left(M, f_{sw}, L_{m2(max)}, L_{r2(max)}, C_{r-eq(\alpha=min, C_{a2}=max, C_{r2}=max)}\right) \quad (8)$$

where the subscripts *_min* and *_max* indicate the minimum and maximum values of the associated variables due to components' tolerances. $C_{r-eq(\alpha=max, C_{a2}=min, C_{r2}=min)}$ is the equivalent resonant capacitance when α is maximum, C_{a2} is minimum and C_{r2} is minimum, and $C_{r-eq(\alpha=min, C_{a2}=max, C_{r2}=max)}$ is the equivalent resonant capacitance when α is minimum, C_{a2} is maximum and C_{r2} is maximum.

Reminding that increasing any component's value in a passive impedance network will increase the total impedance and a larger impedance will contribute to a smaller output current. Hence, the two criteria in equations (2) and (3) can be expressed as follows:

$$I_{o2}\left(M, f_{sw}, L_{m2(min)}, L_{r2(min)}, C_{r-eq(\alpha=max, C_{a2}=min, C_{r2}=min)}\right) < I_{o1}\left(M, f_{sw}, L_{m1(max)}, L_{r1(max)}, C_{r1(max)}\right) \quad (9)$$

$$I_{o2}\left(M, f_{sw}, L_{m2(max)}, L_{r2(max)}, C_{r-eq(\alpha=min, C_{a2}=max, C_{r2}=max)}\right) > I_{o1}\left(M, f_{sw}, L_{m1(min)}, L_{r1(min)}, C_{r1(min)}\right) \quad (10)$$

where X_{max} = 1.05 × X and X_{min}= 0.95 × X considering +/-5% tolerances, X represents L_{m1}, L_{m2}, L_{r1}, L_{r2}, C_{r1}, C_{r2}, and C_{a2}. The two equivalent capacitances $C_{r-eq(\alpha=max, C_{a2}=min, C_{r2}=min)}$ and $C_{r-eq(\alpha=min, C_{a2}=max, C_{r2}=max)}$ which satisfy the design criteria are determined first.

The current sharing performance becomes worse at heavy loads, and it is less influenced by the voltage gain. The two equivalent capacitances are determined first in the heaviest load operation at the nominal condition voltage gain, then are verified and adjusted in other operation points. After some iterations, the two equivalent capacitances are determined as

$$C_{r-eq(\alpha=max, C_{a2}=min, C_{r2}=min)} = 10\ nF \quad (11)$$

$$C_{r-eq(\alpha=min, C_{a2}=max, C_{r2}=max)} = 6\ nF \quad (12)$$

With the help of the expression of the equivalent resonant capacitance and computer simulations, and considering the minimum and maximum α angles, C_{r2} and C_{a2} are designed as C_{r2} = 11 nF, C_{a2} = 9.5 nF. Hence, the final LLC tank parameters of the proposed converter are listed in TABLE II.

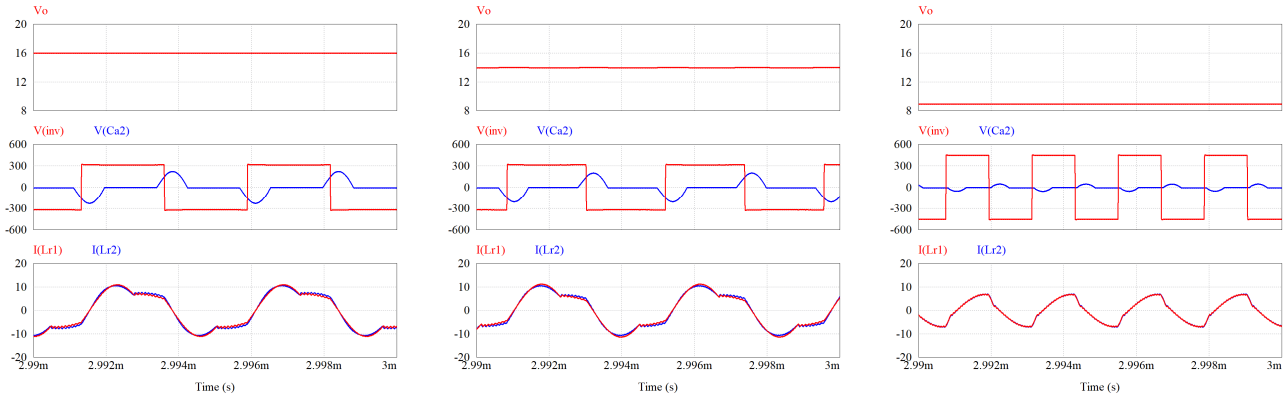
TABLE II. DESIGNED PARAMETERS OF THE PROPOSED DUAL-PHASE LLC DC-DC CONVERTER

Parameters	Phase 1	Phase 2
L_r inductance	15 µH	15 µH
L_m inductance	90 µH	90 µH
C_r capacitance	8 nF	11 nF
C_a capacitance	-	9.5 nF
Transformer turn ratio (n:1:1)	22:1:1	22:1:1

IV. SIMULATION AND EXPERIMENTAL VERIFICATIONS

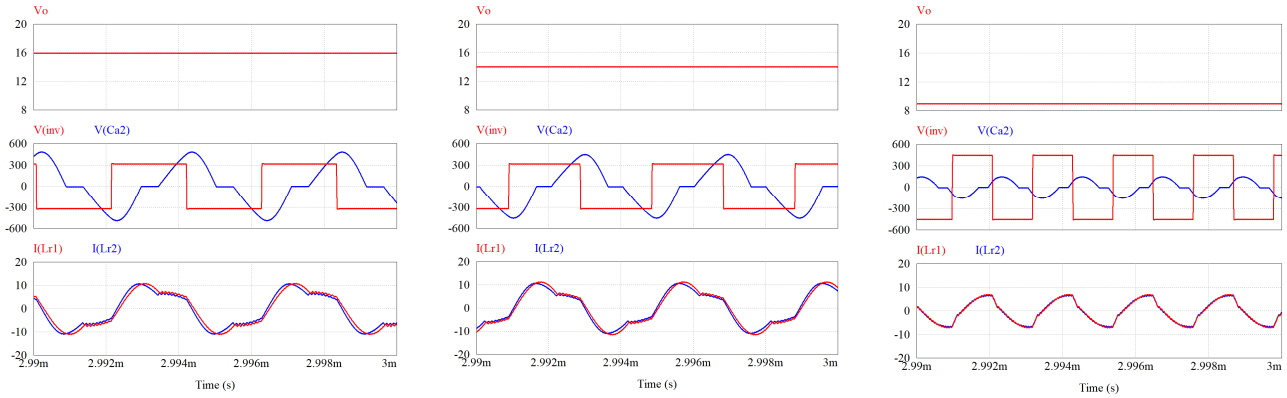
A. Simulation Results

In order to verify the theoretical design of the two-phase SCC-LLC converter some computer simulations have been done in the PSIM environment. The parameters used in the simulation are the same as the resonant tank parameters designed in the previous section and a maximum of 5% tolerance is considered for the resonant tank components of both phases. The test conditions are (1) V_{in}=320 V to V_o=16 V at rated output power that is equal to I_o=245 A, (2) V_{in}=320 V to V_o=14 V at rated output power with I_o=280 A, and (3) V_{in}=450 V to V_o=9 V at the rated output current of I_o=280 A. Fig. 3 illustrates the simulation results with +5% on the resonant components of phase 1 and with -5 % on the resonant components of phase 2. Fig. 4 illustrates the simulation results with -5% on the resonant components of phase 1 and with +5 % on the resonant components of phase 2. It can be observed that in both extreme cases the SCC circuit was able to achieve current balancing for all corner cases.



(a) (b) (c)

Fig. 3. Simulation results of the proposed dual-phase design for different conditions considering extreme component tolerances as L_{r1}+5%, L_{m1}+5%, C_{r1}+5%, L_{r2}-5%, L_{m2}-5%, C_{r2}-5%, C_{a2}-5%, (a) V_{in}=320V, V_o=16V, I_o=250A, f_{sw}=218.8k, α=145°, (b) V_{in}=320V, V_o=14V, I_o=280A, f_{sw}=229.2k α=144°, and (c) V_{in}=450V, V_o=9V, I_o= 280A, f_{sw}=421.8k α=141°.



(a) (b) (c)

Fig. 4. Simulation results of the proposed dual-phase design for different conditions considering extreme component tolerances as L_{r1}-5%, L_{m1}-5%, C_{r1}-5%, L_{r2}+5%, L_{m2}+5%, C_{r2}+5%, C_{a2}+5%, (a) V_{in}=320V, V_o=16V, I_o=225A, f_{sw}=241.8k α=99°, (b) V_{in}=320V, V_o=14V, I_o=280A, f_{sw}=252.6k α=95°, and (c) V_{in}=450V, V_o=9V, I_o= 280A, f_{sw}=454.2k α=116°

B. *Experimental results*

A 4 kW laboratory prototype is built to test the performance of the proposed two-phase SCC-LLC converter. The general system specifications used for the design of the prototype and the components used in the prototype are listed in TABLE III. Fig. 5 shows the 4 kW EV APM prototype that is mounted on a cold plate for proper thermal dissipation. The dimensions of the

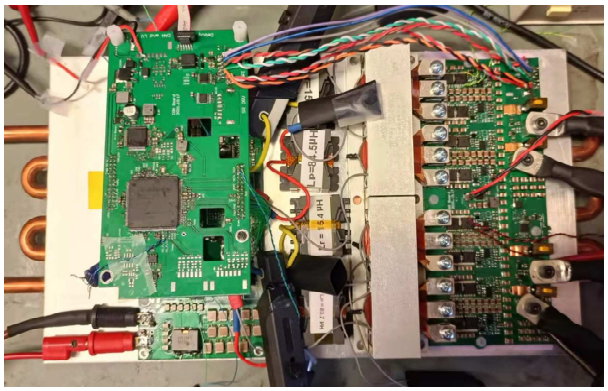


TABLE III. SYSTEM SPECIFICATIONS AND PARAMETERS OF EACH PHASE IMPLEMENTED IN THE EXPERIMENTAL SETUP

Parameters/Descriptions	Values/Part Number
Input voltage range	250 V – 450 V
Output voltage range	10 V – 16 V
Rated output voltage	14 V
Maximum output current	285A
Maximum output power	4 kW (2 kW × 2)
Transformer	n = 22:1:1, (× 2)
Parallel inductor	L_{m1} = 85µH, L_{m2} = 85µH, (PQ32/20 - 3C97)
Series inductor	L_{r1} = 15µH, L_{r2} = 15µH, (PQ32/20 - 3C97)
Series capacitor of phase 1	C_{r1} = 8.1nF (4.7nF × 4 + 6.8nF × 2), (CGA6M1C0G3A472J200AE × 4 + CGA6M1C0G3A682J200AE × 2)
Series capacitor of phase 2	C_{r2} = 10.9nF (6.8nF × 2 + 15nF × 2), (CGA6M1C0G3A682J200AE × 2 + C3225C0G3A153J250AC × 2)
SCC capacitor of phase 2	C_{a2} = 9.4nF (4.7nF + 4.7nF), (CGA6M1C0G3A472J200AE × 2)
Primary side switches	650V, 30A, (GS66508B × 4)
Secondary side switches	40V, 250A, (IAUA250N04S6N007AUMA1 × 8)
SCC switches	650V, 69A, (IPT65R033 × 2)
Output capacitor	620µF (10µF × 31 × 2) + 180uF (10uF × 18, (12105C106K4Z2A × 80)
Micro-controller	TC375TP96F300WAAKXUMA1

prototype are 22cm × 17.2cm × 2.6cm resulting in a 4 kW/L power density. It should be noted that phase shedding is employed to enhance efficiency across the load range. For load currents up to approximately 120 A, only phase 1 operates, while for currents between 120 A and 280 A, both phases are active to share the load.

Fig. 6 presents the experimental waveforms for two-phase operation under different input voltages and a nominal output voltage at the rated current. It can be observed that, under all operating conditions, the resonant currents in both phases are highly similar, indicating a well-balanced load distribution between the two phases. It should be mentioned that the output current of each phase is measured and compared within a 5 A hysteresis band to modulate the SCC circuit for effective current sharing. Fig. 7 illustrates the current difference between the phases across the tested load range, from 100 A to 280 A, under different input voltage conditions. It can be observed that current sharing is successfully maintained within the hysteresis band.

For further testing with thermal performance consideration, the prototype was tested with the liquid cooling temperature set to 40°C and 65°C. The thermal images operations with V_{in}=380 V and a fixed V_o=14 V at rated current with 40°C coolant temperature are illustrated in Fig. 8. It should be mentioned that in all cases the circuit was operating for more than 10 minutes so the component temperatures were stabilized. It can be observed that the SR of phase 2 operates at a slightly higher temperature that could be due to the SCC operation. The maximum operating junction temperature of the MOSFETs used for the SR is 175°C. Therefore, the implemented EV APM prototype can reliably operate under rated power conditions with SR temperatures of up to 100°C. Additionally, the temperatures of the parallel inductors remain stable between the two phases,

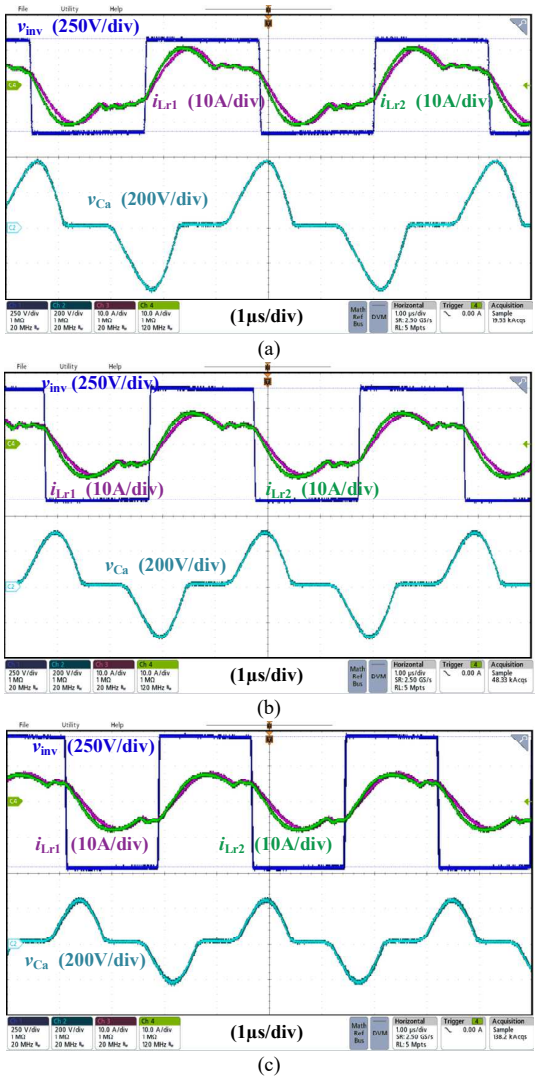


Fig. 6. Experimental results of the two-phase operation with SCC operation, (a) V_{in}=320 V to V_o=14 V and I_o=285 A, (b) V_{in}=380 V to V_o=14 V and I_o=280 A, and (c) V_{in}=450 V to V_o=14 V and I_o=285 A.

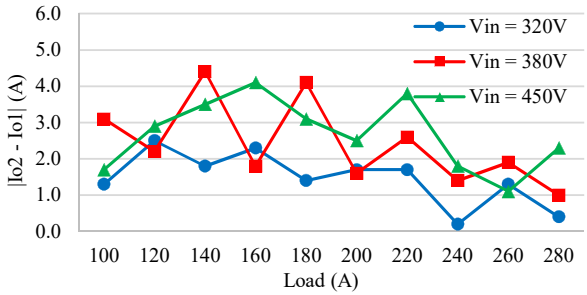


Fig. 7. Current sharing performance of the proposed dual-phase LLC converter from 100 A to 280 A load current.

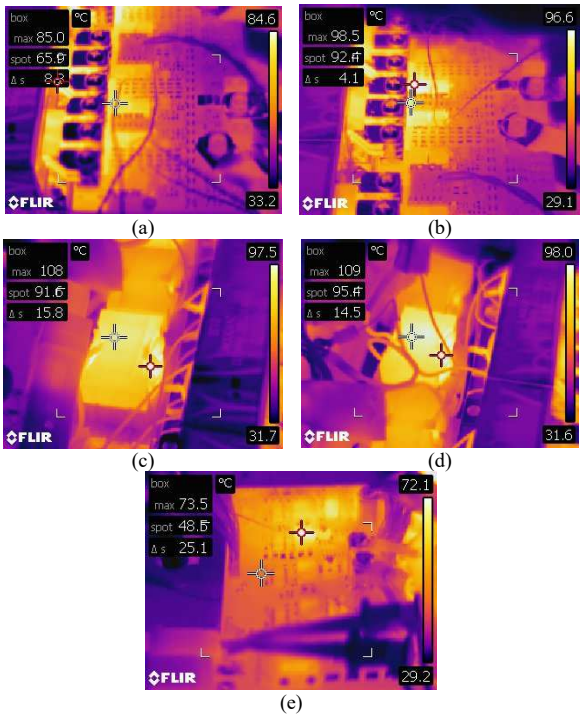


Fig. 8. Thermal images captured for dual-phase operation for V_{in}=380 V, V_o=14 V, and I_o=280 A with 40°C coolant temperature, (a) SR of phase 1, (b) SR of phase 2, (c) L_{m1}, (d) L_{m2}, and (e) GaN and SCC switches.

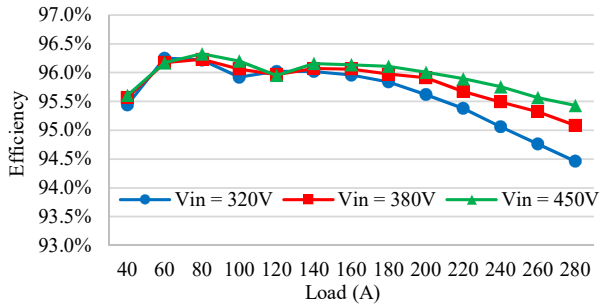


Fig. 9. Efficiency measurement results of the proposed two-phase SCC-LLC converter over the load range with 40℃ coolant temperature.

and the maximum temperature of the GaN devices and SCC MOSFETs are well below 100℃.

Fig. 9 illustrates the efficiency curves for two-phase operation at different input voltage levels and V_o=14 V over the load range, with a coolant temperature of 40℃. A flat efficiency curve exceeding 95% is observed across the load range. Up to a load current of 120 A, only phase 1 operates, while beyond 120 A, both phases operate to share the load. The average efficiencies for V_{in}=320 V, V_{in}=380 V, and V_{in}=450 V are calculated as 95.6%, 95.8, and 95.9%, respectively.

V. Conclusion

This paper introduces a novel resonant tank design for a dual-phase LLC converter in APM applications, reducing the cost and complexity of conventional multi-phase designs. Unlike traditional approaches requiring SCC circuits on each phase, the proposed method utilized a single SCC circuit on one phase while achieving current sharing across a wide voltage range. In the design procedure the impedance of the SCC-equipped phase is deliberately kept lower to ensure effective current balancing, even under ±5% component tolerances. Computer simulations and experimental results from a 4 kW EV APM prototype validated the proposed design method in achieving accurate current sharing. Experimental measurements demonstrated successful current balancing within a 5 A limit, achieving a power density of 4 kW/L and a peak efficiency of 96.3%.

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