

A Gate Drive Strategy for Full Output Voltage Regulation of a Zero-Inductor-Voltage Converter

Sina Salehi Dobakhshari, Aamna Nasir Hameed, Binghui He, Mojtaba Forouzes, Yan Fei Liu

Abstract- The Zero-Inductor-Voltage (ZIV) converter is a step-down capacitive solution which conventionally has a fixed input to output voltage conversion ratio. It has zero output current ripple that has led to high power density and high efficiency at high output current applications. However, the fixed conversion ratio has limited the converter's utilization. Nonetheless, in this paper a new pulse pattern for the 7-Switch is proposed by which the output voltage can be regulated from $0V$ to V_{in} . Unlike the other control methods introduced in the literature, this method does not need any auxiliary components, and the regulation range is from zero to unity. At the same time, the output current ripple is kept at lower value as compared with conventional Buck converter or three-level Buck converter. The benefit of a lower current ripple is that a smaller inductor can be used which improves the power density and reduces the cost significantly. In the paper, the performance of the proposed control method is investigated through theoretical analysis, and it has been validated by a prototype with 20-60V input voltage, 12V output voltage, 21A output current, with 97.12% average efficiency at full load, and 1025W/in³ power density.

Index Terms- Full voltage conversion range, high efficiency, high power density, switched capacitor converter, zero-inductor-voltage.

I. INTRODUCTION

Generally, step-down converters can be divided into two main categories, as inductive and capacitive solutions. The inductive converters are those that usually utilize coupled inductors and/or high frequency transformers to step up or down the voltage, and sometimes provide galvanic isolation. Although they provide excellent voltage regulation with high efficiency [1], the bulky and costly magnetic components are the major drawbacks [2]. By comparison, capacitive solutions are extremely compact with a high-power density, sometimes even more than 4000W/in³ [3]. Moreover, they can be extremely efficient at high power (>97%) [2-13], with a very fast dynamic response [14-17]. Accordingly, capacitive solutions have gained significant attention lately, especially because of the recent advances in semiconductors that have made them more cost effective. In [2], an LLC converter is compared with a Switched Capacitor Converter (RSCC) which is a capacitive solution, and it is shown that at the same output power, the power density of the RSCC is 5.8 times higher.

The switched-capacitor converters (SCCs) are the first generation of capacitive solutions. The conventional SSCs were only composed of switches and capacitors that made them suffer from high current spikes due to paralleling capacitors with uneven voltage level. This has caused power loss known as charge redistribution loss [1]. Also, a major limitation of these converters is that the voltage conversion ratio is fixed,

which hinders these converters from being utilized in most applications.

To eliminate the current spikes and charge redistribution loss issues, inductors are inserted in series with the capacitors. In some studies, such as [9-13, 18], inductors are distributed in the converter and form series resonant tank with capacitors, which are called switched-tank converters (STCs). These converters can achieve soft switching for all switches taking advantage of resonant nature. Furthermore, in some other SCCs the inductors are aggregated in one, which provides the only resonant tank in series with the converter's capacitors. When the resonant frequency is close to the switching frequency it forms resonant switched-capacitor converters (RSCCs) [3, 6, 15, 17-26]. However, by increasing the capacitors value the resonant frequency moves far lower than the switching frequency and the capacitors voltage ripple becomes very small. In this condition, the voltage across the inductor would be almost zero (except for small capacitors voltage ripple) at every switching interval in a switching cycle. This converter is also known as zero-inductor-voltage (ZIV) [4, 5, 7, 27, 28], in which the zero voltage across the inductor leads to zero current ripple, in that case, a very small inductor can be used.

These new generations of the SCCs (STC, RSCC, and ZIV), have successfully eradicated the redistribution loss problem by effectively using inductor(s). However, the voltage regulation is still a major challenge in these converters. Nevertheless, in some studies, they achieved a limited range of voltage regulations [5, 6, 11, 12, 19, 20, 24]. In [11], the multi-level STC achieved very high efficiency adopting soft switching, however using phase shift technique for voltage regulation has restricted the conversion range between 0.28 and 0.38. In [12], a multi-level STC converter is introduced that regulates the output voltage by adjusting the phase shift among the tanks. The voltage conversion ratio in this converter is limited to the range between 0.16 and 0.2 which is very narrow. A non-resonant STC is proposed in [13] that controls the output voltage by duty cycle. Although the control technique in that converter is unique, the conversion ratio is from 0 to maximum 0.5, and the peak efficiency is 88%. In [18], a resonant STC is introduced with high power density and high efficiency, however, the voltage conversion ratio is restricted to the discrete values as $2^n:1$, where "n" is the number of modules. Each module includes six switches. Therefore, the efficiency drops as the number of modules increases.

In recent years, RSCCs have become very popular. In [19], a Binary/Fibonacci RSCC is introduced, utilizing a current sensor on each capacitor to enable soft switching. As implied by the converter's name, the conversion ratio is limited to discrete values such as 1/8, 3/8, 5/8, and 7/8. The proposed

design in [20] has converted a three-level buck topology into an RSCC and regulates the output voltage by phase shift adjustment. The efficiency is reported to be more than 99% when the voltage conversion is 0.5, and for conversion ratio higher than 0.55 or lower than 0.45, the efficiency drops below 97%. Although this converter is highly efficient, the effective conversion ratio is very limited (between 0.45 and 0.55). The same topology has been utilized in [6] that uses an asymmetric control technique in which the frequency, duty cycle and phase shift values are being controlled to regulate the output voltage. It extends the voltage conversion ratio to 1/3 to 2/3. Just like [11], the efficiency significantly drops when the conversion ratio deviates from 0.5. In [24], a partial voltage conversion ratio is achieved by using on-time fixed variable frequency control. However, the voltage gain is limited to 0.33.

Some RSCCs have achieved full voltage conversion ratio by frequency control method [21, 23]. The converter in [23] has a wide conversion ratio ranging from 0.5 to 2, meaning that it can even boost the input voltage. However, the maximum efficiency is 90% and it occurs at unity voltage ratio. In [21], the RSCC has achieved full range of voltage conversion by applying frequency and phase shift control combined, but the converter needs to sense the resonant tank current, and its maximum efficiency is 91%.

In order to achieve full voltage conversion ratio, in some cases a buck converter is associated with the SCC [14, 16, 29-37]. In [29, 30], a buck converter is connected in series with a SCC converter. Since it has to deliver the nominal output current, the overall efficiency of these converters is low (<85%). Similarly, in [31-34], a LEGO-POL converter is proposed for 48V-to-1V voltage conversion which is comprised of a 30:1 SCC and a buck converter in series for post voltage regulation. The converter delivers up to 850 A, achieving an efficiency of 87%, which is considered to be very good for this current level. A dual inductor hybrid SCC is introduced in [35]. Similarly, this converter uses a buck converter in the last conversion stage, however using two phases has improved the maximum efficiency to almost 95%. In [36], a buck converter is connected in series at input and parallel at output with a SCC. Since the buck converter delivers a part of the nominal power, the efficiency is more than the mentioned SCC in series with buck solutions (95.3%), but it is still low in comparison with the SCCs without voltage regulation. The same structure for connecting a buck converter to a SCC is utilized in [16]. Although the number of switches is increased in comparison with [36], the efficiency is slightly improved.

For further efficiency enhancement, in some studies multi-phase buck converters are utilized [14, 38-40]. In [38], three phase buck converters regulate the output of a 6:1 SCC. Although the first stage preserves soft switching, the overall efficiency at full load is 88.7%. Likewise, two 3-to-1 Dickson SCCs are connected to nine interleaved buck converters in [40]. Considering the soft switching in association with multiple interleaved buck converters, it potentially results in a significant reduction in power loss, however, maximum 93.5% efficiency is reported.

In this paper, a new pulse arrangement is going to be presented to extend the voltage conversion ratio of the 7-switch ZIV converter to the fullest. The converter is shown in Fig. 1, which was initially introduced in [4], and a partial voltage regulation for which was proposed in [5] where the efficiency of the converter is preserved (>97% at full load), however, the voltage conversion ratio is limited to 0.2-0.3. In this paper, a new gate pulse strategy is going to be discussed that is applied to this converter. This new method does not need any extra component to be added to the converter, and it only uses the duty cycle to regulate the output voltage. Moreover, this new method keeps the inductor current as low as possible, which is the key point in SCCs to achieve very high efficiency. A diagram for this introduction is presented in Fig. 1.

The main advantage of the proposed gate pulse strategy is to extend the voltage gain of the ZIV converter to the full range (from 0 to 1) without any additional component or sensor, while maintaining high efficiency, high power density. Fig. 1 shows a summary diagram of the SCCs and the voltage regulation solutions introduced in the literature.

In Section II, the operation principle of the converter based on the new gate drive strategy is explained in detail. Section III

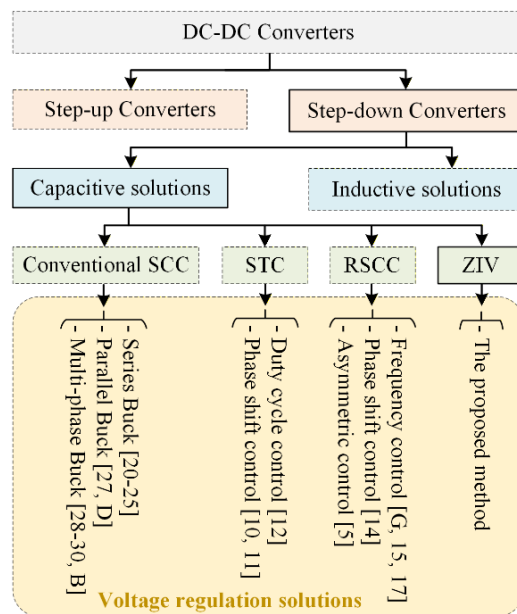


Fig. 1 A summary of the introduction for SCCs

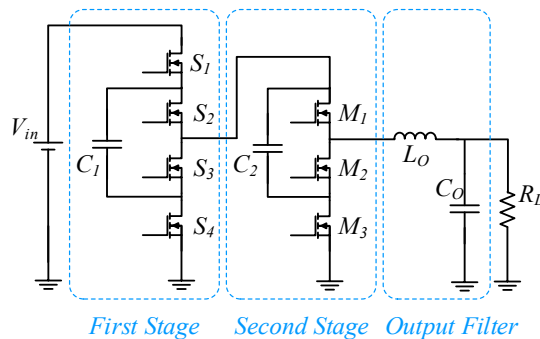


Fig. 2 The 7-Switch ZIV converter circuit

provides theoretical analysis and shows that the output voltage can be regulated from $0V$ to V_{in} while maintain a small inductance value. Experimental results are presented in Section IV, and finally, the results are compared with the other similar solutions in Section V. Section VI is conclusion.

II. CONVERTER OPERATION WITH PROPOSED GATE DRIVE STRATEGY

According to Fig.2, the converter is comprised of two stages and one output filter. The first stage includes four switches (S_1 , S_2 , S_3 , and S_4), and a flying capacitor C_1 . The second stage is formed by three switches (M_1 , M_2 , and M_3) and a flying capacitor C_2 . Moreover, inductor L_o and capacitor C_o are the output filter. In this figure, the input source and output load symbols are V_{in} and R_L , respectively. Based on the duty cycle value (D) of switch S_1 , the converter's operation is divided into four modes as follows:

- Mode I: $0 \leq D \leq 1/4$
- Mode II: $1/4 \leq D \leq 1/3$
- Mode III: $1/3 \leq D \leq 1/2$
- Mode IV: $1/2 \leq D \leq 1$

The converter's operation in these four modes is discussed in detail as follows. In this section it is assumed that the components are ideal meaning that there is no equivalent series resistance or voltage drop.

A. MODE I: $0 \leq D \leq 1/4$

The pulse pattern and inductor's current in a switching cycle for the $0 \leq D \leq 1/4$ are shown in Fig.3 (a). In this mode:

- 1) Switches S_1 and S_3 are turned on simultaneously at the beginning of the switching cycle and are turned off at DT_s .
- 2) Switches S_2 and S_4 also are turned on simultaneously at $t=Ts/4$ and turned off at DT_s .
- 3) Switch M_1 is turned on at $t=Ts/2$ and remains on for duration of $2DT_s$.
- 4) Switch M_2 operates complementary with M_1 meaning that whenever M_1 is off, M_2 is on and vice versa.
- 5) Finally, M_3 is turned on when S_2 is turned off, and it is turned off at the end of the switching cycle.

Therefore, one switching cycle could be divided into six intervals that are explained in detail below and the current flow paths in each interval are depicted in Fig. 4.

Interval 11 [$t_{10} t_{11}$]: At t_{10} , S_1 and S_3 are turned on. Since M_2 was turned on before, the voltage across the inductor L_o would be $V_{in}-V_{C1}-V_{C2}-V_o$. So, the inductor's current variation in this interval can be calculated as:

$$\Delta i_{L_o,11} = \frac{DT_s}{L_o} (V_{in} - V_{C1} - V_{C2} - V_o) \quad (1)$$

where V_{C1} , V_{C2} , and V_o are voltage for first and second flying capacitor and output voltage, respectively. Also, T_s is the

switching period. The inductor current, charges both capacitors C_1 and C_2 . Interval 11 ends at t_{11} , when S_1 and S_3 are turned off.

Interval 12 [$t_{11} t_{12}$]: At t_{11} , S_1 and S_3 are turned off and only M_2 remains on until t_2 . In this interval, the inductor current flows through M_2 and the body diode of M_3 . As a result, the voltage across the inductor would be $-V_o$, and the current variation is:

$$\Delta i_{L_o,12} = \frac{(0.25-D)T_s}{L_o} (-V_o) \quad (2)$$

This interval finishes at t_{12} , when S_2 and S_4 are turned on.

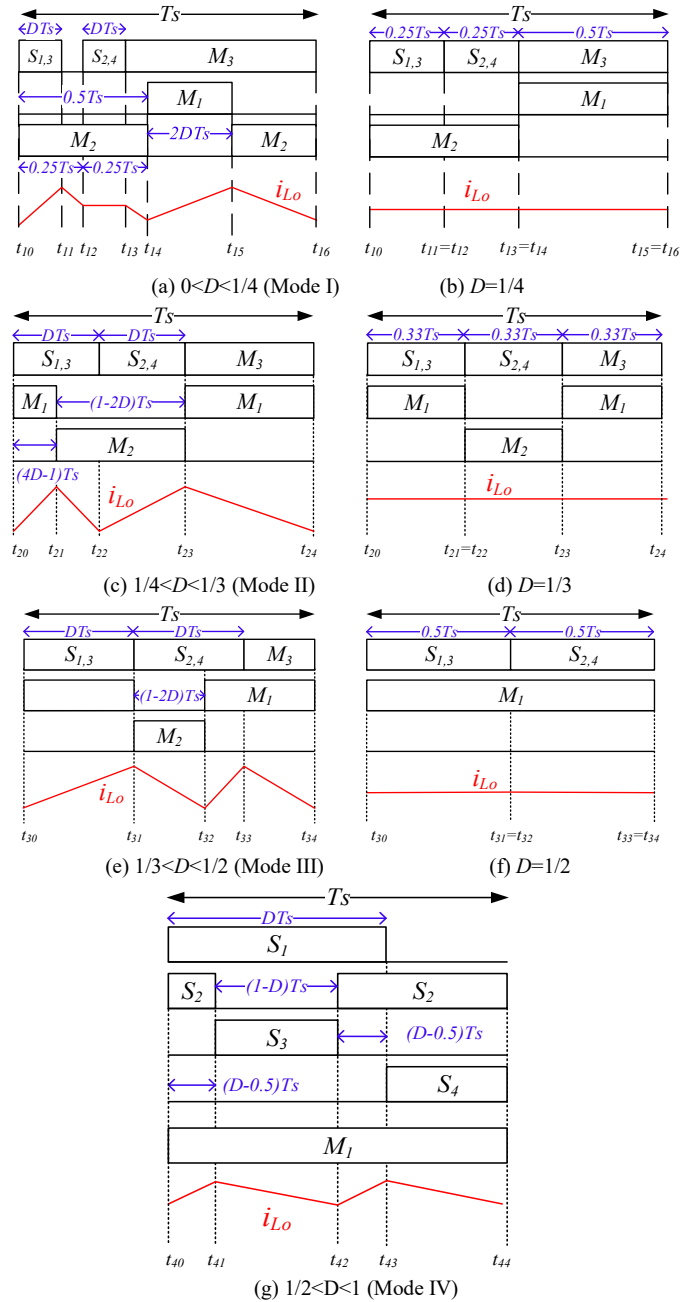


Fig. 3 The pulse pattern and output inductor's current at different modes.

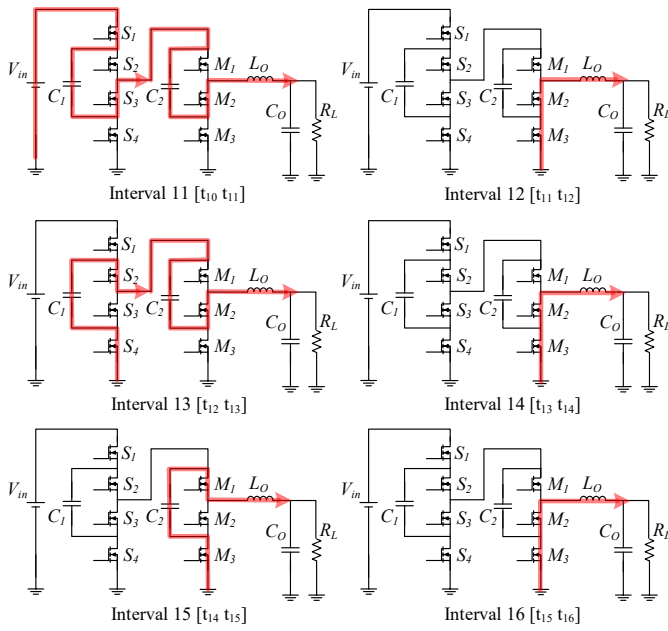


Fig. 4 The current flow path of the converter in a switching cycle in Mode I.

Interval 13 [t₁₂ t₁₃]: At t₁₂, S₂ and S₄ are turned on and M₂ is still on. So, in this interval, the voltage across the inductor is V_{C1}-V_{C2}-V_O, and the inductor's current change is:

$$\Delta i_{L_{O,13}} = \frac{DT_s}{L_o} (V_{C1} - V_{C2} - V_O) \quad (3)$$

The inductor current discharges C₁ and charges C₂. The interval ends at t₁₃, when S₂ and S₄ are turned off.

Interval 14 [t₁₃ t₁₄]: At t₁₃, S₂ and S₄ are turned off and M₃ is turned on. Also, M₂ is on. Therefore, the inductor's current flows through M₃ and M₂ leading to -V_O across the inductor. So, its current variation is:

$$\Delta i_{L_{O,14}} = \frac{(0.25-D)T_s}{L_o} (-V_O) \quad (4)$$

This interval finishes at t₁₄, when M₂ is turned off and M₁ is turned on.

Interval 15 [t₁₄ t₁₅]: At t₁₄, M₂ is turned off and M₁ is turned on. So, the voltage across the inductor is V_{C2}-V_O leading to the current variation equal to:

$$\Delta i_{L_{O,15}} = \frac{2DT_s}{L_o} (V_{C2} - V_O) \quad (5)$$

The inductor current discharges C₂. The interval ends at t₁₅, when M₁ is turned off and M₂ is turned on again.

Interval 16 [t₁₅ t₁₆]: At t₁₅, M₁ is turned off and M₂ is turned on. This interval is the same as interval 14 when only M₂ and M₃ are on. So, the voltage across the inductor is -V_O and the current variation is:

$$\Delta i_{L_{O,16}} = \frac{(0.5-2D)T_s}{L_o} (-V_O) \quad (6)$$

The interval ends at t₁₆=T_s, when M₃ is turned off and S₁ and S₃ are turned on again.

When the duty cycle is zero, the converter is off, and when it increases from zero to 1/4, the converter's operation is the same as the six intervals explained above. As duty cycle D approaches 1/4, intervals 2, 3, and 6 shrink, and whenever it becomes equal to 1/4, these intervals totally vanish. The waveforms for D=1/4 are presented in Fig. 3(b). At this condition, the voltage across the inductor is zero in all intervals, as a result the current ripple is zero. When the duty cycle keeps increasing and passes 1/4, the converter's operation enters Mode II.

B. MODE II: 1/4 ≤ D ≤ 1/3

The pulse pattern and inductor's current in one switching cycle for the 1/4 ≤ D ≤ 1/3 are presented in Fig. 3(c). In this mode:

- 1) Switches S₁ and S₃ are turned on simultaneously at the beginning of the switching cycle and turn off after DT_s.
- 2) Switches S₂ and S₄ are also turned on at t=DT_s and are turned off at t=2DT_s.
- 3) Switch M₁ is turned on at t=2DT_s and remains on for duration of 2DT_s completing some of its duration in the next switching cycle.
- 4) Switch M₂ operates complementary with M₁ meaning that whenever M₁ is off, M₂ is on and vice versa. So, it is turned on at t=(4D-1)T_s and is turned off at t=2DT_s.
- 5) Finally, switch M₃ is turned on when S₂ and S₄ are turned off (t=2DT_s), and it is turned off at the end of the switching cycle.

Therefore, one switching cycle could be divided into four intervals that are explained in detail below and the current flow paths in each interval are depicted in Fig. 5.

Interval 21 [t₂₀ t₂₁]: At t₂₀, S₁ and S₃ are turned on and M₁ is already on from the previous switching cycle, the voltage across the inductor L_O would be V_{in}-V_{C1}-V_O. Hence, the inductor's current variation can be calculated as:

$$\Delta i_{L_{O,21}} = \frac{(4D-1)T_s}{L_o} (V_{in} - V_{C1} - V_O) \quad (7)$$

The inductor current charges the first flying capacitor C₁. The interval ends at t₂₁, when M₁ is turned off.

Interval 22 [t₂₁ t₂₂]: At t₂₁, M₁ is turned off and M₂ is turned on. Until t₂₂, S₁, S₃, and M₂ stay on. In this interval, the inductor current charges both C₁ and C₂.

Therefore, the voltage across the inductor is V_{in}-V_{C1}-V_{C2}-V_O, and the current variation is:

$$\Delta i_{L_{O,22}} = \frac{(1-3D)T_s}{L_o} (V_{in} - V_{C1} - V_{C2} - V_O) \quad (8)$$

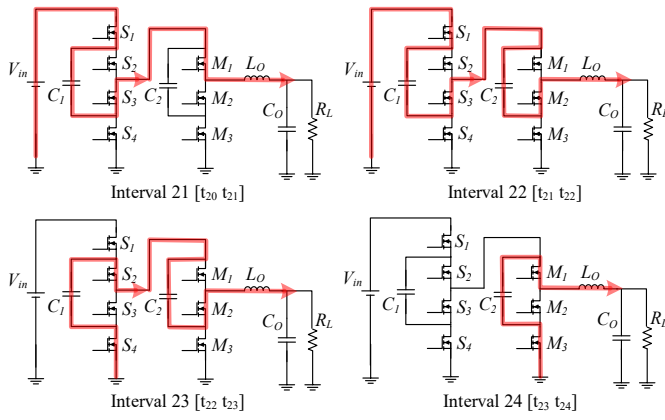


Fig. 5 The current flow path of the converter in a switching cycle in Mode II.

This interval finishes at t_{22} , when S_2 and S_4 are turned on and S_1 and S_3 are turned off.

Interval 23 [$t_{22} t_{23}$]: At t_{22} , S_2 and S_4 are turn on and S_1 and S_3 are turned off. M_2 is still on. So, in this interval, the voltage across the inductor is $V_{C1}-V_{C2}-V_O$, and the inductor's current change is:

$$\Delta i_{L_{O_23}} = \frac{DT_s}{L_o} (V_{C1} - V_{C2} - V_O) \quad (9)$$

The inductor current discharges C_1 and charges C_2 , and it ends at t_{23} , when S_2 and S_4 are turned off.

Interval 24 [$t_{23} t_{24}$]: At t_{23} , S_2 , S_4 and M_2 are turned off. At the same time M_1 and M_3 are turned on. As a result, C_2 discharges and the inductor's current flow through M_1 and M_3 leading to $V_{C2}-V_O$ across the inductor. Therefore, its current variation is:

$$\Delta i_{L_{O_24}} = \frac{(1-2D)T_s}{L_o} (V_{C2} - V_O) \quad (10)$$

This interval finishes at T_s , when M_3 is turned off but M_1 stays on.

When the duty cycle is greater than 1/4 and less than 1/3 the converter operates in the four intervals shown in Fig. 4. As the duty cycle increases, interval 2 shortens. However, when $D=1/3$, this interval completely vanishes (Fig. 3 (d)). At this condition, the voltage across the inductor is zero in all intervals, as a result the current ripple becomes zero. As the duty cycle continues to increase beyond 1/3, the converter enters Mode III.

C. MODE III: $1/3 \leq D \leq 1/2$

The pulse pattern and inductor's current in one switching cycle for the $1/3 \leq D \leq 1/2$ are presented in Fig. 3 (e). In this mode:

- 1) Switches S_1 and S_3 are turned on simultaneously at the beginning of the switching cycle and are turned off after DT_s .
- 2) Switches S_2 and S_4 are also turned on at $t=DT_s$ and are turned off at $t=2DT_s$.
- 3) Switch M_1 is turned on at $t=(1-D)T_s$ and remains on for $2DT_s$ completing some of its duration in the next switching cycle. In this mode, M_1 is turned off at the same time as S_1 and S_3 .
- 4) Switch M_2 operates complementary with M_1 meaning that whenever M_1 is off, M_2 is on and vice versa. So, it is turned on at $t=DT_s$ and is turned off at $t=(1-D)T_s$.
- 6) Finally, switch M_3 is turned on when S_2 and S_4 are turned off ($t=2DT_s$), and it is turned off at the end of the switching cycle.

Therefore, one switching cycle could be divided into four intervals that are explained in detail below and the current flow in each interval is depicted in Fig. 6.

Interval 31 [$t_{30} t_{31}$]: At t_{30} , S_1 and S_3 are turned on. Since M_1 is already on from the previous switching cycle, the voltage across the inductor is $V_{in}-V_{C1}-V_O$. So, the inductor's current variation can be calculated as:

$$\Delta i_{L_{O_31}} = \frac{DT_s}{L_o} (V_{in} - V_{C1} - V_O) \quad (11)$$

The inductor current charges the flying capacitor C_1 . This interval ends at t_{31} , when S_1 and S_3 are turned off.

Interval 32 [$t_{31} t_{32}$]: At t_{31} , S_1 , S_3 and M_1 are turned off and S_2 , S_4 and M_2 are turned on. In this interval, the inductor current flows through both flying capacitors discharging C_1 and charging C_2 . Therefore, the voltage across the inductor is $V_{C1}-V_{C2}-V_O$, and the current variation is:

$$\Delta i_{L_{O_32}} = \frac{(1-2D)T_s}{L_o} (V_{C1} - V_{C2} - V_O) \quad (12)$$

This interval finishes at t_{32} , when M_2 is turned off and M_1 is turned on.

Interval 33 [$t_{32} t_{33}$]: At t_{32} , M_1 is turned on. S_2 and S_4 are still on from the previous interval. Therefore, the voltage across the inductor is $V_{C1}-V_O$, and the inductor's current change is:

$$\Delta i_{L_{O_33}} = \frac{(3D-1)T_s}{L_o} (V_{C1} - V_O) \quad (13)$$

The inductor current discharges C_1 . Interval 33 ends at t_{33} , when S_2 and S_4 are turned off.

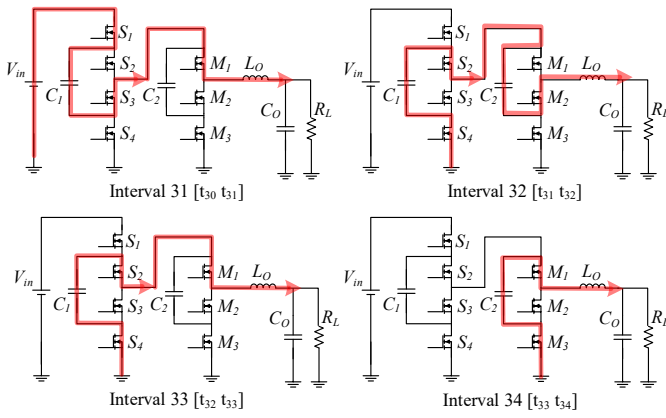


Fig. 6 The current flow path of the converter in a switching cycle in Mode III.

Interval 34 [t_{33} t_{34}]: At t_{33} , S_2 and S_4 are turned off and M_1 stays on. Additionally, M_3 is turned on. As a result, C_2 discharges and the inductor current flows through M_1 and M_3 leading to $V_{C2}-V_O$ across the inductor. So, its current variation is:

$$\Delta i_{L_{O-34}} = \frac{(1-2D)T_s}{L_o} (V_{C2} - V_O) \quad (14)$$

This interval finishes at T_s , when M_3 is turned off but M_1 stays on.

As can be observed from Fig. 3(e) and Fig. 3(f), when the duty cycle changes from $1/3$ to $1/2$, intervals 2 and 4 lessen and finally become zero when $D=0.5$. At this condition, the voltage across the inductor is zero in all intervals, as a result the current ripple will be zero. As the duty cycle continues to increase beyond 0.5 up to 1 the converter enters Mode IV.

D. MODE IV: $1/2 \leq D \leq 1$

The pulse pattern and inductor current in one switching cycle for $1/2 \leq D \leq 1$ are presented in Fig. 3 (g). In this mode:

- 1) Switch S_1 is turned on at the beginning of the switching cycle and is turned off after DT_s .
- 2) Switch S_2 is also turns on at $t=T_s/2$ and is turned off after DT_s , completing some of its duration in the next switching cycle. So, it is turned off at $t=(D-1/2)T_s$.
- 3) Switch S_3 operates complementary with S_2 , so it is turned on at $t=(D-1/2)T_s$ and is turned off at $t=T_s/2$.
- 4) Switch S_4 operates complementary with S_1 , so it is turned on at $t=DT_s$ and turned off at the end of the switching cycle.
- 5) Switch M_1 is always on and bypasses the second stage.
- 6) Switch M_2 and M_3 are always turned off.

Therefore, one switching cycle could be divided into four intervals that are explained in detail below and the current flow paths in each interval are depicted in Fig. 7.

Interval 41 [t_{40} t_{41}]: At t_{40} , S_1 is turned on and S_2 was already on. Since M_1 stays on throughout the switching cycle, the voltage across the inductor is $V_{in}-V_O$. So, the inductor current variation can be calculated as:

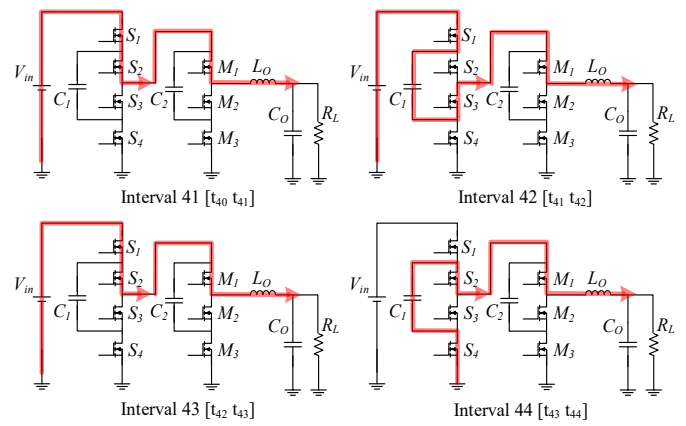


Fig. 7 The current flow path of the converter in a switching cycle in Mode IV.

$$\Delta i_{L_{O-41}} = \frac{(D-0.5)T_s}{L_o} (V_{in} - V_O) \quad (15)$$

The inductor current flows through S_1 , S_2 and M_1 . The interval ends at t_{41} , when S_2 is turned off.

Interval 42 [t_{41} t_{42}]: At t_{41} , S_2 is turned off and S_3 is turned on. In this interval, the inductor's current flows through C_1 charging the capacitor. Therefore, the voltage across the inductor is $V_{in}-V_{C1}-V_O$, and the current variation is:

$$\Delta i_{L_{O-42}} = \frac{(1-D)T_s}{L_o} (V_{in} - V_{C1} - V_O) \quad (16)$$

This interval finishes at t_{42} , when S_2 is turned on while S_1 keeps staying on.

Interval 43 [t_{42} t_{43}]: At t_{42} , S_2 is turned on while S_1 and M_1 are still on. So, this interval is the same as the first one and the voltage across the inductor is $V_{in}-V_O$, and the inductor's current change is:

$$\Delta i_{L_{O-43}} = \frac{(D-0.5)T_s}{L_o} (V_{in} - V_O) \quad (17)$$

This interval ends at t_{43} , when S_1 is turned off.

Interval 44 [t_{43} t_{44}]: At t_{43} , S_1 is turned off while S_2 and M_1 continue to be on. At the same time S_4 is also turned on. As a result, C_1 discharges and the inductor's current flows through M_1 , S_2 and S_4 leading to $V_{C1}-V_O$ across the inductor. So, its current variation is:

$$\Delta i_{L_{O-44}} = \frac{(1-D)T_s}{L_o} (V_{C1} - V_O) \quad (18)$$

This interval finishes at T_s , when S_4 is turned off but S_2 continues to stay on.

When the duty cycle goes over $1/2$, intervals 2 and 4 diminish, and eventually disappear when $D=1$.

It is noted that the operation in this mode is similar to the conventional 3-level Buck converter.

As can be seen in Fig. 3, by moving from one mode to another, the pulse pattern evolves continuously, exhibiting no sudden transitions or irregularities. For example, with $D < 0.25$ the converter is in Mode I and the pulse pattern is the same as Fig. 3(a). When duty cycle increases to $D = 0.25$, the pulse pattern becomes the same as Fig. 3(b). Eventually, if the duty cycle increases further ($D > 0.25$) the converter enters to Mode II and the pulse pattern becomes the same as Fig. 3 (c). It can be seen that this transition is completely continuous and smooth. This is true for the transition between the other modes.

III. VOLTAGE GAIN AND INDUCTOR CURRENT RIPPLE ANALYSIS

In this section, the output voltage, the flying capacitors' voltage, the inductor's current, and switches voltage stress equations are derived for all four operation modes.

A. ANALYSIS FOR MODE I ($0 \leq D \leq 1/4$)

In the steady state the summation of inductor's current ripples in six intervals is zero which is known as volt-second balance:

$$\Delta i_{L_{o,11}} + \Delta i_{L_{o,12}} + \Delta i_{L_{o,13}} + \Delta i_{L_{o,14}} + \Delta i_{L_{o,15}} + \Delta i_{L_{o,16}} = 0 \quad (19)$$

Therefore, substituting equations (1)-(6) into (19) computes output voltage to:

$$V_o = DV_{in} \quad (20)$$

Since D is between 0 and 1/4, the output voltage is between 0V and 25% of the input voltage.

The initial value of inductor current at the beginning of each switching cycle is defined as i_l , which is depicted in Fig. 8. Accordingly, the charge-second relation for C_l using i_l is:

$$DT_S \left(i_l + \frac{\Delta i_{L_{o,11}}}{2} \right) = DT_S \left(i_l + \Delta i_{L_{o,11}} + \Delta i_{L_{o,12}} + \frac{\Delta i_{L_{o,13}}}{2} \right) \quad (21)$$

The current waveform for this capacitor is depicted in Fig. 9, where its timing and current amplitudes are indicated. Using equations (1)-(3), and (20) in (21), gives:

$$V_{C12} = V_{in}/4 \quad (22)$$

where V_{C12} is the DC voltage value of capacitor C_2 in Mode I.

In a same way, for the second flying capacitor the charge-second balance is:

$$DT_S \left(i_l + \frac{\Delta i_{L_{o,11}}}{2} \right) + DT_S \left(i_l + \Delta i_{L_{o,11}} + \Delta i_{L_{o,12}} + \frac{\Delta i_{L_{o,13}}}{2} \right) = 2DT_S \left(i_l - \Delta i_{L_{o,16}} - \frac{\Delta i_{L_{o,15}}}{2} \right) \quad (23)$$

By substituting ripple current equations in equation (23) the first flying capacitors voltage can be written as:

$$V_{C11} = (D + 0.25)V_{in} \quad (24)$$

where V_{C11} is the DC voltage value of capacitor C_1 in Mode I. When $D = 0.25$, $V_{C11} = 0.5V_{in}$.

Now substitution of (20), (21), and (24) into (1), (3) and (5) results in:

$$\Delta i_{L_{o,11}} = \frac{DT_S V_{in}}{L_o} (0.5 - 2D) \quad (25)$$

$$\Delta i_{L_{o,13}} = \frac{DT_S V_{in}}{L_o} (D + 0.25 - 0.25 - D) = 0 \quad (26)$$

$$\Delta i_{L_{o,15}} = \frac{2DT_S V_{in}}{L_o} (0.25 - D) \quad (27)$$

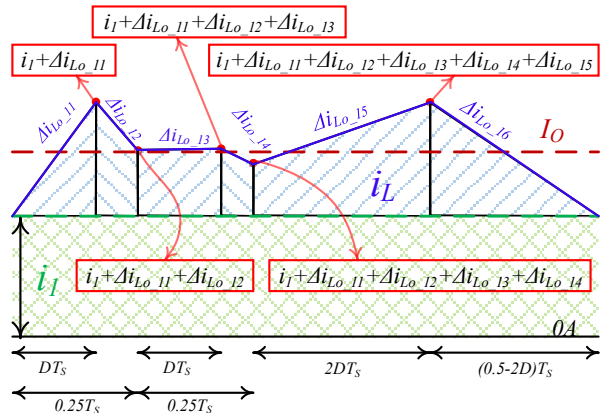


Fig. 8 Inductor current waveform for $0 \leq D \leq 1/4$

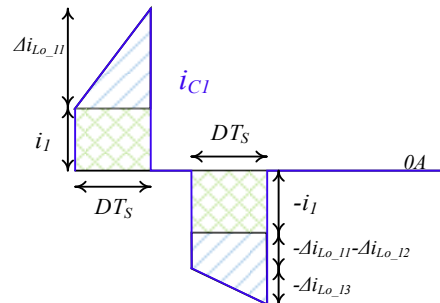


Fig. 9: The first flying capacitor current for $0 \leq D \leq 1/4$

The above equations show that $\Delta i_{L_{o,13}}$ is always zero when $0 \leq D \leq 1/4$, and when the duty cycle reaches 1/4, $\Delta i_{L_{o,11}}$ and $\Delta i_{L_{o,15}}$ also become zero. Moreover, at this moment ($D = 1/4$) the time duration for the second, fourth, and sixth intervals goes down to zero making $\Delta i_{L_{o,12}}$, $\Delta i_{L_{o,14}}$, and $\Delta i_{L_{o,16}}$, equal to zero.

Hence, it can be concluded that the inductor current ripple at $D = 1/4$ is zero.

B. ANALYSIS FOR MODE II ($1/4 \leq D \leq 1/3$)

Similar to previous mode, inductor's volt-second balance in Mode II is:

$$\Delta i_{L_{o,21}} + \Delta i_{L_{o,22}} + \Delta i_{L_{o,23}} + \Delta i_{L_{o,24}} = 0 \quad (28)$$

Substituting equations (7)-(10) into (28) gives the output voltage as $V_o = DV_{in}$, which is the same as equation (20).

The charge-second equation for C_1 is:

$$(4D - 1)T_S(i_1 + \Delta i_{L_{o,21}}/2) + (1 - 3D)T_S(i_1 + \Delta i_{L_{o,21}} + \Delta i_{L_{o,22}}/2) = DT_S(i_1 + \Delta i_{L_{o,21}} + \Delta i_{L_{o,22}} + \Delta i_{L_{o,23}}/2) \quad (29)$$

Using (7)-(10), and (20) in (29), results in:

$$V_{C22} = \frac{D^2(2D-1)}{14D^2-8D+1} V_{in} \quad (30)$$

where V_{C22} is the DC voltage of capacitor C_2 in Mode II. At $D=1/3$, $V_{C22}=V_{in}/3$.

The charge-second relation for C_2 is:

$$(1 - 3D)T_S(i_1 + \Delta i_{L_{o,21}} + \Delta i_{L_{o,22}}/2) + DT_S(i_1 + \Delta i_{L_{o,21}} + \Delta i_{L_{o,22}} + \Delta i_{L_{o,23}}/2) = (1 - 2D)T_S(i_1 + \Delta i_{L_{o,21}} + \Delta i_{L_{o,22}} + \Delta i_{L_{o,23}} + \Delta i_{L_{o,24}}/2) \quad (31)$$

Similarly, substituting (7)-(10), and (20) in (31), results in:

$$V_{C21} = \frac{-8D^3+17D^2-8D+1}{14D^2-8D+1} V_{in} \quad (32)$$

where V_{C21} is the DC voltage of capacitor C_1 in Mode II. At $D=1/3$, $V_{C21}=2V_{in}/3$.

By using (20), (30), and (32), equations (7)-(10) can be rewritten as:

$$\Delta i_{L_{o,21}} = \frac{D(1-2D)(3D-1)(4D-1)T_S}{L_o(14D^2-8D+1)} V_{in} \quad (33)$$

$$\Delta i_{L_{o,22}} = \frac{D(1-2D)(1-3D)(4D-1)T_S}{L_o(14D^2-8D+1)} V_{in} \quad (34)$$

$$\Delta i_{L_{o,23}} = \frac{D(3D-1)(1-2D)(4D-1)T_S}{L_o(14D^2-8D+1)} V_{in} \quad (35)$$

$$\Delta i_{L_{o,24}} = \frac{D(1-2D)(1-3D)(4D-1)T_S}{L_o(14D^2-8D+1)} V_{in} \quad (36)$$

Accordingly, when duty cycle becomes equal to 1/3, the inductor current variation in all the four intervals becomes zero.

C. ANALYSIS FOR MODE III ($1/3 < D \leq 1/2$)

Following the same convention as the previous two modes, the inductor's volt-second balance is:

$$\Delta i_{L_{o,31}} + \Delta i_{L_{o,32}} + \Delta i_{L_{o,33}} + \Delta i_{L_{o,34}} = 0 \quad (37)$$

Substituting equations (11)-(14) into (37) gives the output voltage as $V_O=DV_{in}$, which is the same as equation (20).

The charge-second equation for C_1 can be written as:

$$DT_S(i_1 + \Delta i_{L_{o,31}}/2) = (1 - 2D)T_S(i_1 + \Delta i_{L_{o,31}} + \Delta i_{L_{o,32}}/2) + (3D - 1)T_S(i_1 + \Delta i_{L_{o,31}} + \Delta i_{L_{o,32}} + \Delta i_{L_{o,33}}/2) \quad (38)$$

Substituting (11)-(13) and (20) in (38), results in:

$$V_{C32} = \frac{D^2}{4D-1} V_{in} \quad (39)$$

where V_{C32} is the DC voltage of capacitor C_2 in Mode III. At $D=0.5$, $V_{C32}=0.25V_{in}$.

The charge-second relation for C_2 is:

$$(1 - 2D)T_S(i_1 + \Delta i_{L_{o,31}} + \Delta i_{L_{o,32}}/2) = (1 - 2D)T_S(i_1 + \Delta i_{L_{o,31}} + \Delta i_{L_{o,32}} + \Delta i_{L_{o,33}} + \Delta i_{L_{o,34}}/2) \quad (40)$$

Using (11)-(14) and (20) in (40), results in:

$$V_{C31} = \frac{2D^2}{4D-1} V_{in} \quad (41)$$

where V_{C31} is the voltage of capacitor C_1 in Mode III. At $D=0.5$, $V_{C31}=0.5V_{in}$.

By using equations (20), (39), and (41), equations (11)-(14) can be rewritten as:

$$\Delta i_{L_{o,31}} = \frac{D(2D-1)(3D-1)T_S}{L_o(1-4D)} V_{in} \quad (42)$$

$$\Delta i_{L_{o,32}} = -\frac{(2D-1)(3D-1)T_S}{L_o(1-4D)} V_{in} \quad (43)$$

$$\Delta i_{L_{o,33}} = \frac{(2D-1)(3D-1)T_S}{L_o(1-4D)} V_{in} \quad (44)$$

$$\Delta i_{L_{o,34}} = -\frac{D(2D-1)(3D-1)T_S}{L_o(1-4D)} V_{in} \quad (45)$$

In equations (42)-(45) when duty cycle is equal to 1/3 and 1/2, the inductor current variation in all the four intervals becomes zero.

D. ANALYSIS OF MODE IV ($1/2 < D \leq 1$)

Following the same pattern as the previous three modes the inductor's volt-second balance is:

$$\Delta i_{L_{o,41}} + \Delta i_{L_{o,42}} + \Delta i_{L_{o,43}} + \Delta i_{L_{o,44}} = 0 \quad (46)$$

Substituting equations (15)-(18) into (46) gives the output voltage as $V_O=DV_{in}$, which is the same as (20).

Based on the inductor's current symmetry:

$$\Delta i_{L_{o,41}} + \Delta i_{L_{o,42}} = 0 \quad (47)$$

Simplifying equation (47) using (15) and (16), results in:

$$V_{C41} = \frac{1}{2} V_{in} \quad (48)$$

where V_{C41} is the voltage of capacitor C_1 in Mode IV.

By using (20) and (48), equations (15)-(18) can be rewritten as:

$$\Delta i_{L_{o,41}} = \frac{(2D-1)(1-D)T_S}{2L_o} V_{in} \quad (49)$$

$$\Delta i_{L_{o,42}} = \frac{(2D-1)(D-1)T_S}{2L_o} V_{in} \quad (50)$$

$$\Delta i_{L_{o,43}} = \frac{(2D-1)(1-D)T_S}{2L_o} V_{in} \quad (51)$$

$$\Delta i_{L_{o,44}} = \frac{(2D-1)(D-1)T_s}{2L_o} V_{in} \quad (52)$$

According to equations (49)-(52) at $D=1/2$ and $D=1$, the inductor current change in all intervals becomes zero.

A. PERFORMANCE DESCRIPTION OVERVIEW

This section will demonstrate the advantages of the proposed gate drive strategy and how it can achieve a very wide output voltage variation range and still maintain very small inductor current ripple. In this section it is assumed that the output voltage is 12V and the input voltage changes from 20V to 60V ($V_o=12V$, $V_{in}=20V-60V$) which is applicable in many applications. As calculated in the previous section, the voltage conversion ratio in all modes is the same as a conventional buck converter which is also plotted in Fig. 10. Moreover, the flying capacitors voltages and the maximum voltage across the

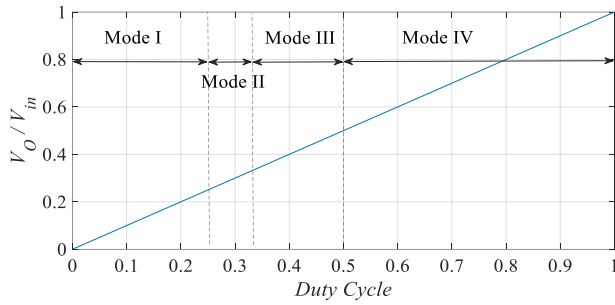


Fig. 10 Voltage conversion range of the converter versus duty cycle.

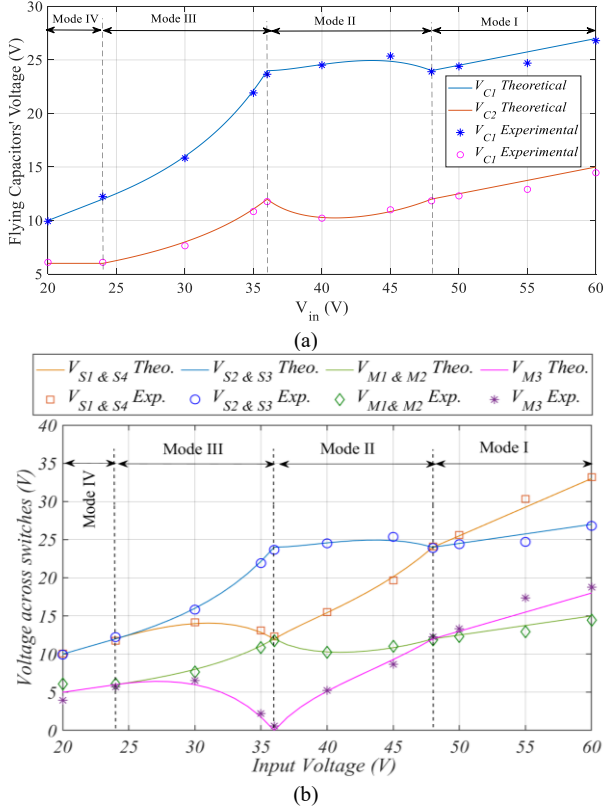


Fig. 11 Theoretical and Experimental results for (a) Flying capacitors' voltage, and (b) switches' voltage stress versus input voltage.

switches are depicted in Fig. 11 along with experimental results, for all four modes. In Fig. 11 (a) the capacitors' voltages changes continuously when the converter operation mode changes. The measured capacitor voltages at different input voltages (20V to 60V) are also shown in Fig. 11 (a). It shows that the measured and calculated values are very close to each other. Both voltage gain and flying capacitors voltage changes continuously as the converter's operation mode changes. This shows that the transient between the modes is smooth without any abrupt changes and discontinuity in the voltages.

The voltage stress for all these 7 switches can be obtained as following based on Fig. 3, 4, 5, and 6.

$$V_{S1\&S4_max} = V_{in} - V_{C1} \quad (53)$$

$$V_{S2\&S3_max} = V_{C1} \quad (54)$$

$$V_{M1\&M2_max} = V_{C2} \quad (55)$$

$$V_{M3_max} = V_{in} - V_{C1} - V_{C2} \quad (56)$$

Fig. 11 (b), shows the voltage stress of these seven switches over the entire input voltage range (20V to 60V). The measured voltage stress is also provided in the figure. It is observed that generally, the voltage stress of the switches rises with input voltage. However, at $V_{in}=60V$, the peak voltage stress for the first stage MOSFETs (S_1 , S_2 , S_3 , and S_4) is 33V, and for the second stage MOSFETs (M_1 , M_2 , and M_3) is 19V. Therefore, low cost and low voltage rating switches (40V and 30V MOSFETs for the first and the second stages, respectively) can be adopted for this converter. In this figure, the experimental results reveal that the voltages stress of the MOSFETs at different points perfectly align with theoretical analysis.

Inductor's current ripples in a conventional and three-level buck converters are presented in (57) and (58).

$$\Delta i_{L_Buck} = \frac{V_{in}T_s}{L_o} D(1 - D) \quad (57)$$

$$\Delta i_{L_3LB} = \begin{cases} \frac{V_{in}T_s}{L_o} D(0.5 - D) & 0 \leq D \leq 0.5 \\ \frac{V_{in}T_s}{L_o} (1 - D)(D - 0.5) & 0.5 \leq D \leq 1 \end{cases} \quad (58)$$

Based on (57), the peak current ripple in a buck converter is:

$$\Delta i_{L_Buck_peak} = \frac{V_{in}T_s}{4L_o} \quad (59)$$

So, the current ripple equations of the conventional buck (57), three-level buck (58), and the 7-switch ZIV converters are normalized as follows based on (59):

$$\Delta i_{L_Buck_N} = 4D(1 - D) \quad (60)$$

$$\Delta i_{L_3LB_N} = \begin{cases} 4D(0.5 - D) & 0 \leq D \leq 0.5 \\ 4(1 - D)(D - 0.5) & 0.5 \leq D \leq 1 \end{cases} \quad (61)$$

$$\Delta i_{L_{ZIV_N}} = \begin{cases} 4D(0.5 - 2D) & 0 \leq D \leq 0.25 \\ \frac{4D(1-2D)(3D-1)(4D-1)}{(14D^2-8D+1)} & 0.25 \leq D \leq 0.33 \\ \frac{4D(2D-1)(3D-1)}{(1-4D)} & 0.33 \leq D \leq 0.5 \\ 4(1-D)(D-0.5) & 0.5 \leq D \leq 1 \end{cases} \quad (62)$$

where $\Delta i_{L_{Buck_N}}$, $\Delta i_{L_{3L_Buck_N}}$, and $\Delta i_{L_{ZIV_N}}$ are the normalized current ripple of conventional buck, three-level buck and the 7-switch ZIV converters, respectively, which are plotted in Fig. 12(a). As mentioned before, one of the main advantages of this pulse arrangement method is that it keeps the inductor current ripple small over the entire voltage conversion range. In Fig. 12(a), it can be observed that the proposed method has produced a much lower inductor current ripple than that of the conventional buck converter.

As compared with the three-level Buck converter, when $0.5 \leq D \leq 1$, the converter operates the same as a three-level buck converter, consequently, they both have the same inductor current ripple value in this range. However, from $D=0$ to $D=0.5$, the proposed method has a significantly lower inductor current ripple. This becomes more substantial when considering that in most of the applications the converter generally operates in $0.2 < D < 0.6$ range (based on the input and output voltages indicated at the beginning of this section).

The theoretical peak-to-peak inductor current ripple value and measured peak-to-peak inductor current values under two load conditions (21A, or 100% load, and 5A, or 25% full load) are plotted over entire input voltage range (20V to 60V). It is observed that at light load (5A) the current ripple is very close to that of ideal case. However, at full load (21A), the inductor current ripple is increased by around 2A. This is caused by lower inductance value at higher current (inductor value drop of around 30%), as well as higher voltage ripples of the flying capacitors.

In this new pulse pattern control, the voltage across the inductor is kept minimum although it is not always zero during modes. However, the term ‘‘ZIV’’ is being used here to refer to the original converter topology.

The inductor value of these three converters is compared in Fig. 13 at the same condition. In this figure, L_{Buck} , L_{3LBuck} , and L_{ZIV} are the required inductor value of conventional buck, three-level buck, and the 7-switch ZIV converters in order to achieve the same inductor current ripple. In this condition, when the proposed gate drive strategy is applied, the required inductor value in the ZIV converter is less than 12% of the conventional Buck converter when $0.2 \leq D \leq 0.55$ (or a reduction of 88%) When the output voltage is close to the input voltage ($D=1$) or the output voltage is close to zero ($D=0$), the required inductance value is 50% of that of Buck converter. It is noted that the operation at D close to 0 and D close to 1 is not common.

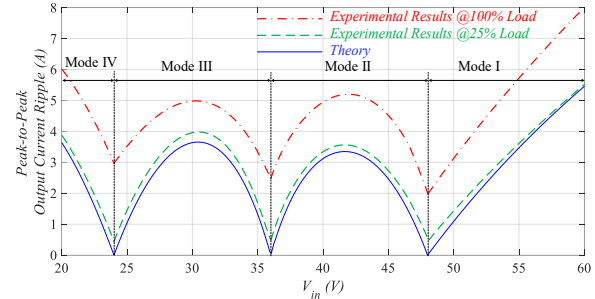
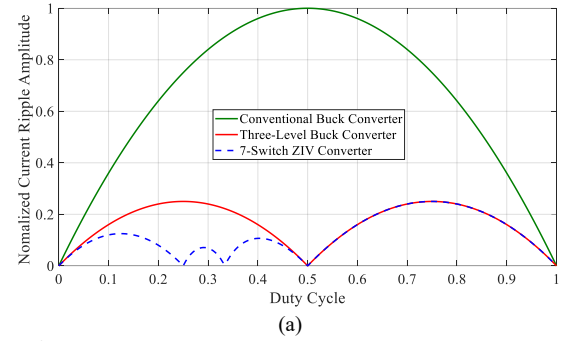


Fig. 12 (a) Peak-to-peak inductor current ripple comparison among the 7-Switch, three-level, and conventional buck converters. (b) Experimental and theoretical results comparison for the ZIV converter.

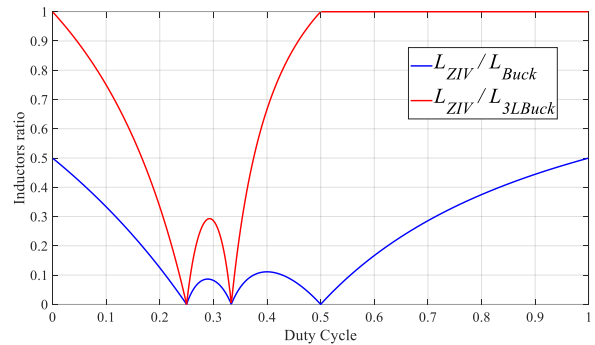


Fig. 13 Required inductor value comparison in a conventional buck, three-level buck and the 7-switch ZIV converters.

When compared with three-level buck converter, the required inductance value in the ZIV converter is less than 30% of the three-level Buck converter when $0.2 \leq D \leq 0.35$ (or a reduction of 70%). The comparison shown in Fig. 13 demonstrated that significant inductance value reduction is achieved by the proposed new gate driving technology.

IV. EXPERIMENTAL RESULTS

An experimental prototype is built to verify the operation of the proposed PWM gate driving strategy and to demonstrate its excellent performance. The specifications of the prototype are listed in Table I. The output voltage is fixed at 12V, and the input voltage changes from 20V to 60V to cover all four modes. The experimental waveforms at full load (21A) are presented in

Table I Prototype specifications

Parameter	Value
V_{in}	20-60V
V_o	12V
I_o	21A
P_o	250W
F_s	100kHz
C_{in}	$7 \times 10\mu\text{F}/100\text{V}$ (effective capacitance $\sim 21\mu\text{F}$)
C_1	$7 \times 10\mu\text{F}/50\text{V}$ (effective capacitance $\sim 28\mu\text{F}$)
C_2	$7 \times 10\mu\text{F}/50\text{V}$ (effective capacitance $\sim 28\mu\text{F}$)
C_o	$10 \times 10\mu\text{F}/50\text{V}$ (effective capacitance $\sim 40\mu\text{F}$)
L_o	2.2uH, XGL6060-222ME
$S1-S4$	BSZ025N04LS, 40V/2.5mΩ
$M1-M3$	SiSA04DN, 30V/2.15mΩ

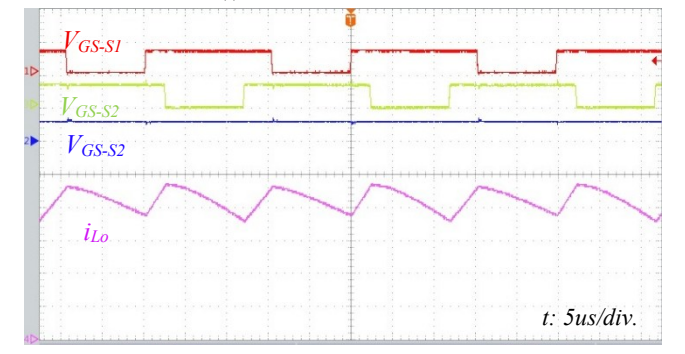
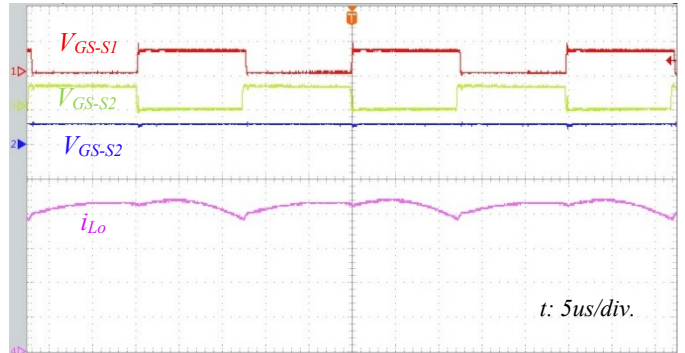
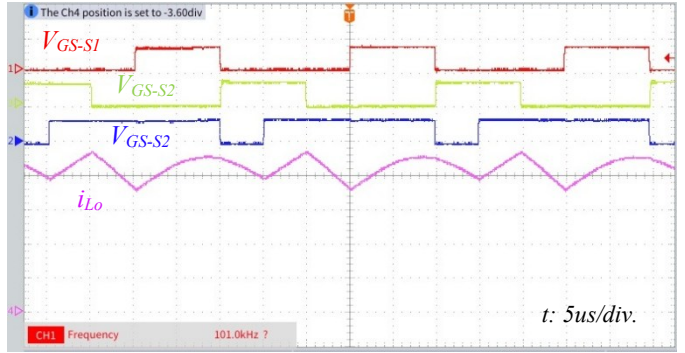
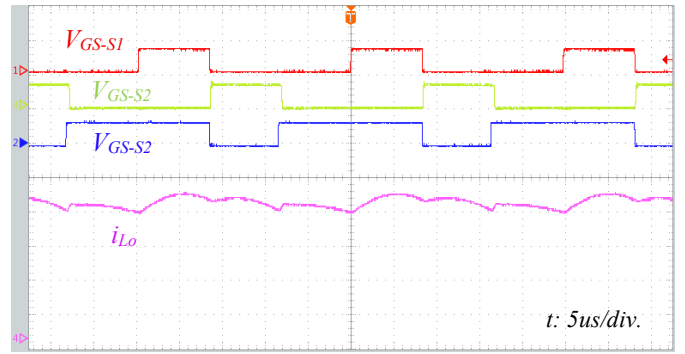
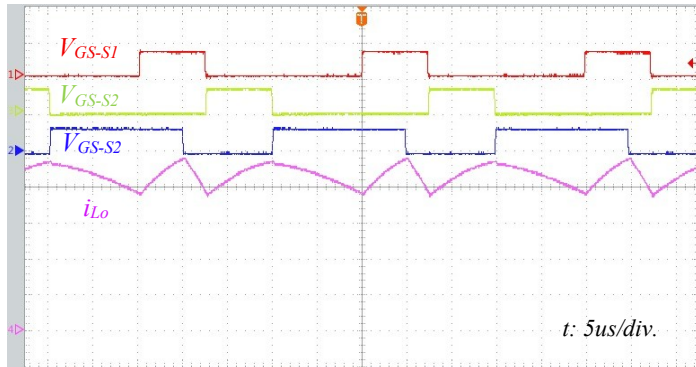
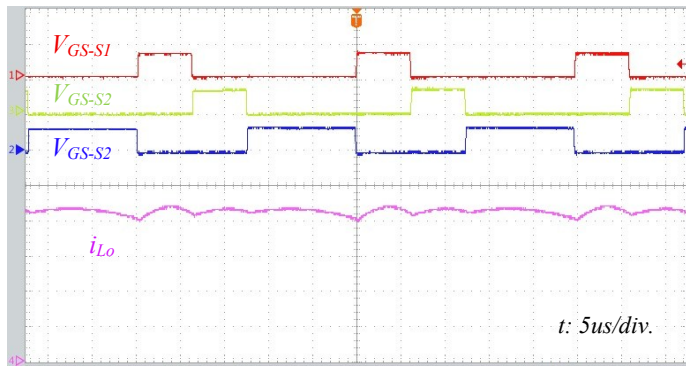
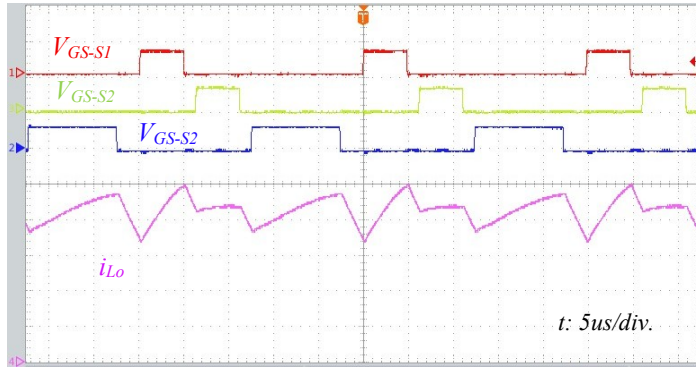


Fig. 14 Experimental waveforms for V_{GS-S1} [5V/div.], V_{GS-S2} [5V/div.], V_{GS-M1} [5V/div.], and i_{Lo} [5A/div.] at 250W output power and various duty cycles ($t=2\mu\text{s}/\text{div.}$).

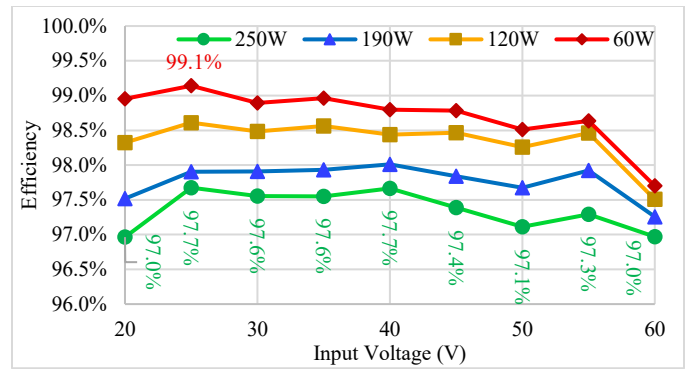
IEEE POWER ELECTRONICS REGULAR PAPER/LETTER/CORRESPONDENCE

Fig. 14, for $D=0.2, 0.25, 0.3, 0.33, 0.4, 0.5,$ and $0.6,$ to show the waveforms at all four modes as well as at boundaries of these modes. In this figure, the gate pulse of switches $S_1, S_2,$ and M_1 are shown along with the output inductor current (i_{Lo}), so it would be easier to compare the results with those explained in Fig. 3.

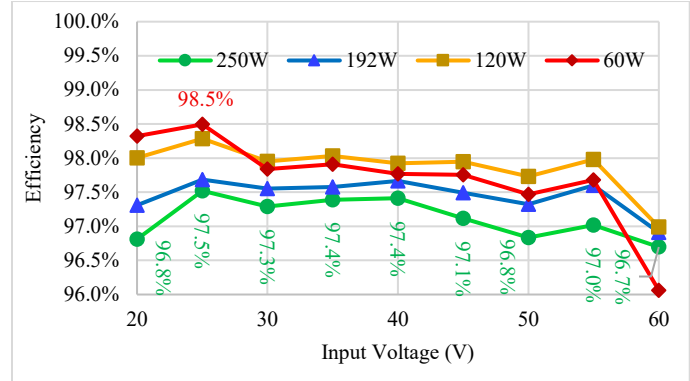
Fig. 14 (a), (c), (e), and (g) show the waveforms at modes I, II, III, and IV, respectively. In addition, the boundary conditions are shown in Fig. 14 (b), (d), and (f) for $D=0.25, 0.33,$ and $0.5,$ respectively. Since the capacitance of the X7R type multi-layer ceramic capacitors derates with the DC bias, the effective capacitance for C_1 and C_2 is lower than $7 \times 10\mu\text{F}.$ When the flying capacitor's value gets smaller, its voltage ripple increases. The capacitor's voltage ripple in conjunction with the switches deadtime causes the current waveform to become curvy in some intervals, especially at the boundary points. However, comparing these results with those presented in Fig. 3 reveals that the experimental results verify theoretical analysis.

The measured efficiencies of the converter at different output power levels (60W, 120W, 190W, and 250W) are plotted in Fig. 15 over entire input voltage range. In Fig. 15 (a) the power train efficiency is plotted, which does not include the control power loss. Consequently, as the load decreases efficiency improves. The average power train efficiency at full load (250W) is 97.35%, and at light load (60W) it is 98.71%. Also, the peak efficiency is 99.1%. Fig. 15 (b) shows total efficiency (including control power loss). The average efficiency at full load is 97.12% and at light load (60W) is 97.70%. The peak efficiency is 98.5%. It is observed that the efficiency variation is very small (less than 0.6%) when the input voltage varies from 20V to 60V (3 to 1 variation range) and load power changes from 60W (25%) to 250W. This performance is enabled by the advantages of the ZIV topology and the very low inductor voltage.

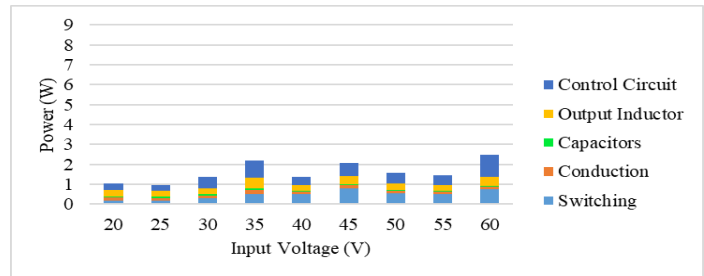
Fig. 15 (c)-(f) shows the power loss breakdown of the converter versus input voltage through light load to full load. The power loss of the output inductor and capacitors are almost constant throughout the input voltage variation, and they increase with output power level. Switches conduction loss slightly reduces as the input voltage increases. Because, as explained in Section II, as the input voltage increases (duty cycle decreases) the first stage switches conduction time becomes shorter, so the conduction loss drops a little. At the same condition, the switching loss slightly increases. Because according to Fig. 11 (b), the maximum voltage across the switches increases with input voltage. This maximum voltage mainly happens at the turn-on or turn-off moment, leading to more switching loss at higher input voltage. Both conduction and switching losses increase as the output power increases.



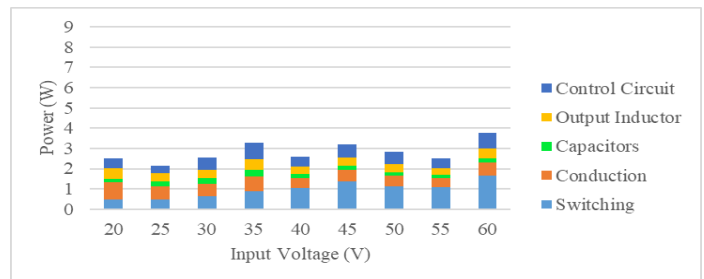
(a) power train efficiency



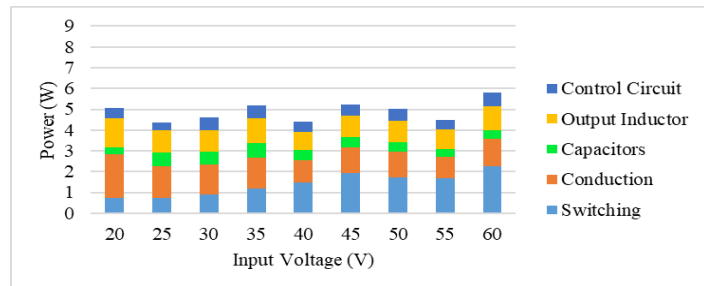
(b) total efficiency



(c) power loss breakdown of the ZIV converter at $P_o=60\text{W}$



(d) power loss breakdown of the ZIV converter at $P_o=120\text{W}$



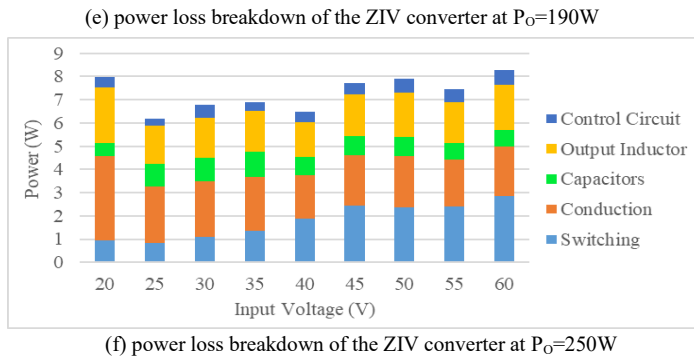


Fig. 15 Efficiency and loss breakdown of the ZIV converter with the new control method.

V. PERFORMANCE COMPARISON

A. COMPARISON WITH INDUCTIVE AND CAPACITIVE SOLUTIONS

A thorough comparison is done in [2] between an RSCC and an LLC converter. The comparison shows the RSCC has more power density although it has much more switching devices. However, the LLC converter is more efficient. Based on the analysis presented in here, the ZIV converter is compared with these two converters in Table II. The LLC and RSC converters have a fixed conversion ratio, and since the voltage conversion ratio in the LLC, RSC, and the proposed converter are different, the comparison among these three converters is done at the condition where $V_{in}=48V$ and $I_O=21A$ in order to have a fair comparison. It can be observed that in a same condition, the ZIV with the proposed gate pulse strategy presents better peak and full load efficiency with a better power density and full range voltage regulation.

Table II, A comparison between the ZIV converter and the RSCC and LLC converter in [2]

	Peak Efficiency @ $V_{in}=48V$	Efficiency at $I_O=21A$ (@126W)	Power density	Voltage regulation?
LLC in [2]	96.6%	~95.5% (@126W)	93.8W/in ³	No
RSC in [2]	95%	~93.5(@168W)	544W/in ³	No
This work	97.8%	96.7% (@252W)	1025W/in³	Yes

B. COMPARISON WITH BUCK CONVERTERS WITH SAME VCR

The efficiency of the proposed ZIV converter is compared against two GaN-based buck converters and a three-level buck converter (TLBC) from EPC [41-42], as shown in Fig. 16. Buck I (EPC9205) operates at $V_{in}=48V$, $V_O=12V$, $I_O=2-15A$, with a switching frequency of 700 kHz and a 2.2uH inductor, achieving a peak efficiency of 95.9% and 95.3% at full load (Fig. 16(a)). Buck II operates at 500 kHz with a 3.3uH inductor, while the TLBC operates at 320 kHz (640 kHz effective) using a 1.5uH inductor, resulting in 50% lower inductor volume. Compared with Buck II, the TLBC exhibits a 25% reduction in power loss and more than 1% higher peak efficiency due to

reduced switching stress and lower effective switching frequency, achieving 96.8% peak efficiency and 96% efficiency at full load (Fig. 16(b)).

Fig 16 (c) compares the efficiency of the ZIV converter with the TLBC, Buck I, and Buck II under identical operating conditions. The ZIV converter demonstrates superior efficiency across the entire output current range of 3–21A. This improvement is attributed to operation at a ZIV point with a conversion ratio of 1/4, where the inductor current ripple is eliminated. In contrast, the current ripple in the TLBC and conventional buck converters is approximately 25% and 60% of the maximum buck ripple, respectively. Since reduced current ripple is a key factor in the efficiency advantage of the TLBC over Buck II, the further ripple minimization in the ZIV converter results in higher efficiency than all other topologies. As summarized in Table III, the ZIV converter achieves the highest peak, full-load, and average efficiency, exceeding Buck I, Buck II, and the TLBC by 1.9%, 2.2%, and 1.2%, respectively, despite operating over a wider output current range.

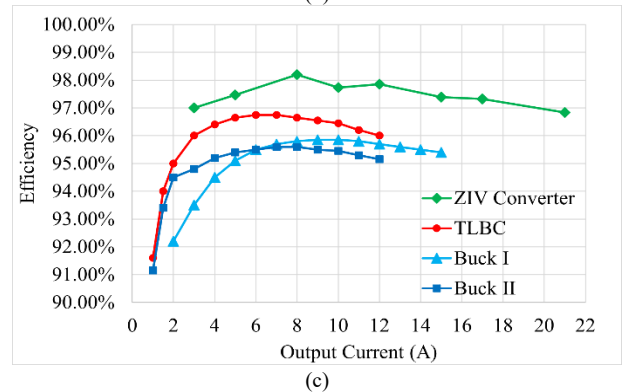
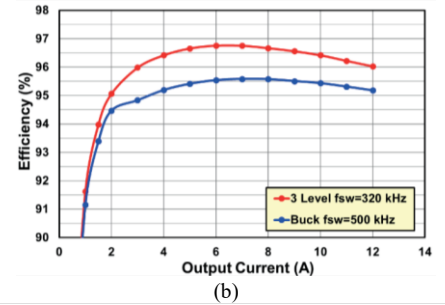
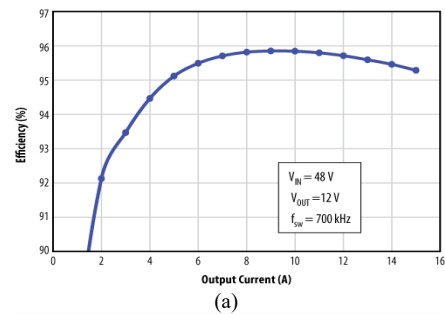


Fig. 16, (a) Efficiency curve of Buck I [41], (b) efficiency curve of TLBC [42] and Buck II [42], (c) efficiency comparison of the ZIV converter, Buck I [41], Buck II [42], and TLBC [42].

Table III, Efficiency comparison of the ZIV converter with buck converters

$V_{in}=48V, V_o=12V$			
	Peak Efficiency	Full Load Efficiency	Average Efficiency
Buck I [41]	95.9%	95.4% @15A	95.6% [5A-15A]
Buck II [42]	95.6%	95.2% @12A	95.3% [2A-12A]
TLBC [42]	96.8%	96% @12A	96.3% [2A-12A]
This work	98.2%	97.4% @15A 96.8% @21A	97.5% [3A-21A]

C. COMPARISON WITH CAPACITIVE SOLUTIONS

A comparison among the switched capacitor converters that can partially/fully regulate the output voltage is presented in Table IV. As explained in the paper, the main target of the paper was to extend voltage conversion ratio and retain high efficiency and high-power density. Therefore, efficiency (peak and full load), power density and voltage conversion range of some of the recently introduced SCCs are compared in this table. Moreover, the number of components, such as switches (S), diodes (D), inductors (L), and capacitors (C), switching frequency, and rated output current are listed in this table. As explained before, the ZIV converter in [5], with the conventional pulse pattern has achieved high efficiency and very high-power density, but its conversion range is extremely limited. Similarly, RSCCs in [6] and [20] have achieved very high efficiency but a narrow range for output voltage regulation. It is notable that [20] has utilized a small number of components, but its power density is not mentioned.

In contrast, the one in [21] has reached the full conversion range, and [23] has even gone beyond that and is able to boost the input voltage as well. However, these two RSCCs suffer from low efficiency, although they employ a few numbers of components. In addition, the power density in [21] is low. Although the converters in [33-34] are composed of an SCC and a buck converter with 40 switches and 12 inductors, they have high power density and achieved 450A output current which is exceptional. Nevertheless, they could not maintain high efficiency and the output voltage conversion range is narrow. The 7-switch ZIV converter with the proposed pulse pattern can fully regulate the output voltage. The average efficiency at full load (through the whole input voltage range) is 97.12%, and the peak efficiency is 98.5%. With the two paralleled phases, the nominal output power is 500W and considering the power part dimensions (1.37"×1.37"×0.26"), the power density is 1025W/in³.

The 7-switch ZIV converter can be used in multi phases to deliver higher power. Fig. 17 shows the parallel connection of two phases. In this configuration, the operation of the converters is the same as before. The only difference is less RMS current in the input capacitors, if the two converters operate with 180° phase shift. Therefore, the efficiency for the 2-phase configuration is the same as Fig. 15 (or might be slightly better because of less loss at C_{in}). The prototype photo

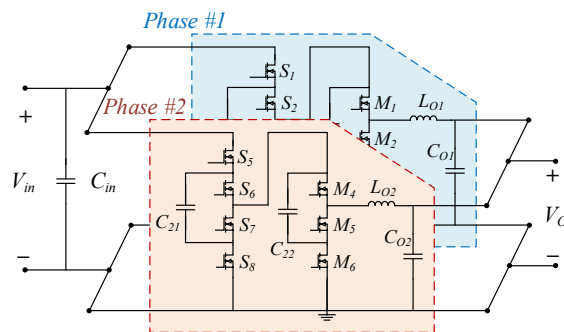


Fig. 17 Two paralleled ZIV converters

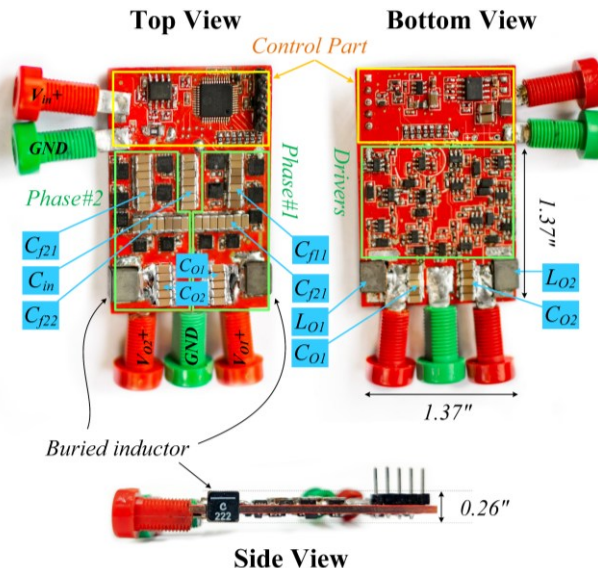


Fig. 18 Photograph of two paralleled phases of the ZIV converter

of the 2-phase ZIV converter is shown in Fig. 18. Power and control parts are indicated in this figure, as well as the components, terminals, and size of the converter.

VI. CONCLUSION

A PWM gate drive strategy for the 7-switch ZIV (Zero-Inductor-Voltage) converter is proposed. With this PWM gate drive strategy, the output voltage can be regulated from 0 to V_{in} (or voltage gain from 0 to 1). In addition, the inductor current ripple is also minimized. The operation of the PWM gate drive strategy is analyzed in detail and the inductor current ripple is calculated accurately. No additional components are needed.

With the proposed gate drive pulse pattern, the ZIV converter operated at four different modes based on the required duty cycle value. As shown in the paper, during the changeover between different modes, the transition is smooth and there is no discontinuity in the currents and voltages value. The other merit of this method is that it keeps the output inductor's current ripple small, in a way that the high efficiency of the ZIV converter is preserved. Also, with lower voltage across the inductor, smaller inductance is used which enhances the power density. Moreover, to handle a higher amount of power, multiple phases of the converter can be connected in parallel

Table IV Comparison among the switched capacitor converters with partially/fully output voltage control

Reference	Topology	Efficiency		Power Density (power part) W/in^3	Conversion Range	Component count				Switching Frequency	Rated Current
		Full Load	Peak Value @ $V_{in}:V_o$			S	D	L	C		
[5]	ZIV	97.3%	99.2% @48:12	2500	[0.2 to 0.3]	7	0	1	2	80kHz	35A
[6]	RSCC	98%	98.6% @300:200	NA	[0.33, 0.66]	6	0	2	3	350kHz	15A
[13]	STC	88%	88% @48:6	<50	[0 to 0.5]	4	4	2	4	200kHz	6A
[14]	SCC+Buck	85%	90% @24:1	NA	[0 to 0.2]	8	0	2	3	1MHz	6A
[16]	RSCC+Buck	95.7%	97.4% @36:5	NA	[0 to 0.5]	17	1	6	6	140kHz	20A
[18]	STC	97.52%	98.96% @48:12	470	0.125	16	0	6	5	275kHz	50A
[19]	RSCC	85%	97% @8:1	NA	1/8, 3/8, 5/8, 7/8	12	0	3	1	30-350kHz	5A
[20]	RSCC	98.8%	>99% @400:200	NA	[0.46 to 0.54]	4	0	1	1	20kHz	15A
[21]	RSCC	80%	91.4% @2.5:1.15	497	[0 to 1]	4	0	1	1	4MHz	1.1A
[23]	RSCC	91%	95% @12:15	NA	[0 to 2]	7	0	1	1	70kHz	1.5A
[24]	RSCC	85%	95% @48:12	<60	[0 to 0.33]	2	5	2	3	67-180kHz	8.5A
[26]	RSCC	81%	91% @48:5	190	[0 to 0.35]	5	0	1	1	75kHz	10A
[31]	SCC+ Buck	87.7%	96% @48:1.5	577	[0 to 0.17]	40	0	12	5	500kHz	300A
[32]	SCC+ Buck	87.2%	93.3% @48:1.5	688	[0 to 0.17]	40	0	12	5	500kHz	450A
[33-34]	SCC+ Buck	87%	91% @48:1	1000	[0 to 0.17]	40	0	12	5	1MHz	450A
[35]	SCC+ Buck	94.5%	95% @48:1	<50	[0 to 0.17]	8	0	2	5	300kHz	10A
[36]	SCC+ Buck	94%	95.34% @48:12	<100	[0 to 0.33]	7	2	3	3	100kHz	17A
[37]	RSCC+Buck	95%	96.8% @48:12	481	[0 to 0.3]	9	0	3	3	100kHz	270A
[39]	SCC+ Buck	90.4%	94.9% @48:1.5	1062	[0 to 0.11]	22	0	9	4	280kHz	105A
[40]	SCC	88%	90% @48:3	768	[0 to 0.5]	14	0	2	10	750kHz	45A
This Work	ZIV	97.12%	98.5% @24:12	1025	[0 to 1]	7	0	1	2	100kHz	21A

with interleaving operation. Thus, a two-phase prototype of the converter with the proposed method is investigated in this study as well.

Both analysis and experimental prototypes demonstrated that with the new PWM gate drive strategy, the 7-switch ZIV topology can achieve wide output voltage variation range and higher efficiency and higher power density as compared with existing technologies.

REFERENCES

[1] J. Liang, L. Wang, M. Fu, J. Liang and H. Wang, "Overview of Voltage Regulator Modules in 48 V Bus-Based Data Center Power Systems," in CPSS Transactions on Power Electronics and Applications, vol. 7, no. 3, pp. 283-299, September 2022.

[2] Z. Tian et al., "Research on High Buck DC-DC Converters Based on Resonant Switched Capacitor and LLC Circuits," in IEEE Access, vol. 13, pp. 3390-3402, 2025.

[3] T. Ge, Z. Ye, R. A. Abramson and R. C. N. Pilawa-Podgurski, "A 48-to-12 V Cascaded Resonant Switched-Capacitor Converter Achieving 4068 W/in³ Power Density and 99.0% Peak Efficiency," 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), Phoenix, AZ, USA, 2021, pp. 1335-1342.

[4] S. Webb, T. Liu and Y. -F. Liu, "Zero Inductor-Voltage Multilevel Bus Converter," in IEEE Transactions on Power Electronics, vol. 36, no. 10, pp. 11565-11578, Oct. 2021.

[5] S. Webb and Y. -F. Liu, "A Quasi Output Voltage Regulation Technique for the Zero Inductor Voltage Converter," 2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 2020, pp. 930-937.

[6] H. Setiadi and H. Fujita, "An Asymmetric Control Method for Switched-Capacitor-Based Resonant Converters," in IEEE Transactions on Power Electronics, vol. 36, no. 9, pp. 10729-10741, Sept. 2021.

[7] Z. Ye, Y. Lei and R. C. N. Pilawa-Podgurski, "The Cascaded Resonant Converter: A Hybrid Switched-Capacitor Topology with High Power Density and Efficiency," in IEEE Transactions on Power Electronics, vol. 35, no. 5, pp. 4946-4958, May 2020.

[8] Dong Cao and Fang Zheng Peng, "Zero-current-switching multilevel modular switched-capacitor dc-dc converter," 2009 IEEE Energy Conversion Congress and Exposition, San Jose, CA, USA, 2009, pp. 3516-3522.

[9] S. Jiang, S. Saggini, C. Nan, X. Li, C. Chung and M. Yazdani, "Switched Tank Converters," in IEEE Transactions on Power Electronics, vol. 34, no. 6, pp. 5048-5062, June 2019.

[10] Y. Li, X. Lyu, D. Cao, S. Jiang and C. Nan, "A 98.55% Efficiency Switched-Tank Converter for Data Center Application," in IEEE Transactions on Industry Applications, vol. 54, no. 6, pp. 6205-6222, Nov.-Dec. 2018.

[11] D. Cao, X. Lu, X. Yu and F. Z. Peng, "Zero voltage switching double-wing multilevel modular switched-capacitor DC-DC converter with voltage regulation," 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 2013, pp. 2029-2036.

[12] Y. Li, B. Curuvija, X. Lyu and D. Cao, "Multilevel modular switched-capacitor resonant converter with voltage regulation," 2017 IEEE Applied

IEEE POWER ELECTRONICS REGULAR PAPER/LETTER/CORRESPONDENCE

- Power Electronics Conference and Exposition (APEC), Tampa, FL, USA, 2017, pp. 88-93.
- [13] M. Uno and A. Kukita, "PWM Switched Capacitor Converter With Switched-Capacitor-Inductor Cell for Adjustable High Step-Down Voltage Conversion," in *IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 425-437, Jan. 2019.
- [14] W. Xue, X. Yu, Y. Zhang and J. Ren, "A 24V-to-1V Triple Series-Capacitor Buck Converter With Low-Voltage Power Switches," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 72, no. 1, pp. 308-312, Jan. 2025.
- [15] A. Dago *et al.*, "A High-Power-Density Quasi-Resonant Switched-Capacitor DC-DC Converter With Single Semiperiod Tank Current Modulation," in *IEEE Transactions on Power Electronics*, vol. 39, no. 2, pp. 2100-2114, Feb. 2024.
- [16] J. Qi, X. Wu and K. Sun, "A Quasi-Parallel Resonant Switched Capacitor DC-DC Converter With Wide Input Voltage Range Regulation and Enhanced Dynamic Performances," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 13, no. 4, pp. 4869-4881, Aug. 2025.
- [17] D. -Y. You, H. -J. Chiu and S. -H. Kuo, "Ladder-Type Resonant Switched-Capacitor Converter Achieving 99.1% Peak Efficiency and 4750 w/in³ Power Density for High-Current Application," in *IEEE Transactions on Power Electronics*, vol. 39, no. 7, pp. 8040-8053, July 2024.
- [18] F. Shao, K. Yao, X. Ruan, Z. Xing, R. Mao and L. Li, "A ZVS Resonant Switched Capacitor Converter With 2n:1 Voltage Conversion Ratio," in *IEEE Transactions on Power Electronics*, doi: 10.1109/TPEL.2025.3627579, early access.
- [19] E. Hamo, A. Cervera and M. M. Peretz, "Multiple Conversion Ratio Resonant Switched-Capacitor Converter with Active Zero Current Detection," in *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 2073-2083, April 2015.
- [20] K. Sano and H. Fujita, "Performance of a High-Efficiency Switched-Capacitor-Based Resonant Converter With Phase-Shift Control," in *IEEE Transactions on Power Electronics*, vol. 26, no. 2, pp. 344-354, Feb. 2011.
- [21] G. Ripamonti, M. Ursino, S. Saggini, S. Michelis and F. Faccio, "Regulated Resonant Switched-Capacitor Point-of-Load Converter Architecture and Modeling," in *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 4815-4827, April 2021.
- [22] K. Kesarwani, R. Sangwan and J. T. Stauth, "Resonant-Switched Capacitor Converters for Chip-Scale Power Delivery: Design and Implementation," in *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6966-6977, Dec. 2015.
- [23] A. Cervera, M. Evzelman, M. M. Peretz and S. Ben-Yaakov, "A High-Efficiency Resonant Switched Capacitor Converter with Continuous Conversion Ratio," in *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1373-1382, March 2015.
- [24] N. Zhang, S. Li, C. Hao and S. Zheng, "A Step-Down Series-Parallel Dual-Resonant Switched-Capacitor Converter With Extended Voltage Gain Range and Complete Soft Charging," in *IEEE Transactions on Industry Applications*, vol. 60, no. 2, pp. 2935-2948, March-April 2024.
- [25] Y. Guan *et al.*, "A High-Performance 3:1 Conversion Ratio DC-DC Converter: Analysis Method and Modular Adoption," in *IEEE Transactions on Power Electronics*, vol. 39, no. 4, pp. 4412-4425, April 2024.
- [26] B. G. Eleftheriades and A. Prodić, "A Soft-Switched High-Conversion-Ratio Quasi-Resonant Flying Capacitor DC-DC Converter," in *IEEE Open Journal of Power Electronics*, vol. 6, pp. 432-448, 2025.
- [27] Y. Lei and R. C. N. Pilawa-Podgurski, "A General Method for Analyzing Resonant and Soft-Charging Operation of Switched-Capacitor Converters," in *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5650-5664, Oct. 2015.
- [28] Y. Lei, R. May and R. Pilawa-Podgurski, "Split-Phase Control: Achieving Complete Soft-Charging Operation of a Dickson Switched-Capacitor Converter," in *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 770-782, Jan. 2016.
- [29] R. C. N. Pilawa-Podgurski, D. M. Giuliano and D. J. Perreault, "Merged two-stage power converter architecture with soft charging switched-capacitor energy transfer," 2008 IEEE Power Electronics Specialists Conference, Rhodes, Greece, 2008, pp. 4008-4015.
- [30] D. M. Giuliano, M. E. D'Asaro, J. Zwart and D. J. Perreault, "Miniaturized Low-Voltage Power Converters With Fast Dynamic Response," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 3, pp. 395-405, Sept. 2014.
- [31] J. Baek, P. Wang, Y. Elasser, Y. Chen, S. Jiang and M. Chen, "LEGO-PoL: A 48V-1.5V 300A Merged-Two-Stage Hybrid Converter for Ultra-High-Current Microprocessors," 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, 2020, pp. 490-497.
- [32] J. Baek, Y. Elasser and M. Chen, "3D LEGO-PoL: A 93.3% Efficient 48V-1.5V 450A Merged-Two-Stage Hybrid Switched-Capacitor Converter with 3D Vertical Coupled Inductors," 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), Phoenix, AZ, USA, 2021, pp. 1321-1327.
- [33] J. Baek *et al.*, "Vertical Stacked LEGO-PoL CPU Voltage Regulator," in *IEEE Transactions on Power Electronics*, vol. 37, no. 6, pp. 6305-6322, June 2022.
- [34] Y. Elasser *et al.*, "Vertical Stacked 48V-1V LEGO-PoL CPU Voltage Regulator with 1A/mm² Current Density," 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), Houston, TX, USA, 2022, pp. 1259-1266.
- [35] G. -S. Seo, R. Das and H. -P. Le, "Dual Inductor Hybrid Converter for Point-of-Load Voltage Regulator Modules," in *IEEE Transactions on Industry Applications*, vol. 56, no. 1, pp. 367-377, Jan.-Feb. 2020.
- [36] S. Han, Y. Wang, Y. Guan and D. Xu, "Analysis and Design of a Modular Switched Capacitor Converter with Adjustable Output Voltage in DC Microgrid," in *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 12, no. 1, pp. 232-241, March 2022.
- [37] S. Han, J. Tan, Y. Wang, Y. Guan and D. Xu, "Multifrequency Single-Stage Hybrid Switched-Capacitor Converter," in *IEEE Transactions on Power Electronics*, vol. 39, no. 3, pp. 3438-3451, March 2024.
- [38] S. Khatua, D. Kastha and S. Kapat, "A Dual Active Bridge Derived Hybrid Switched Capacitor Converter Based Two-Stage 48 V VRM," in *IEEE Transactions on Power Electronics*, vol. 36, no. 7, pp. 7986-7999, July 2021.
- [39] Y. Zhu, T. Ge, Z. Ye and R. C. N. Pilawa-Podgurski, "A Dickson-Squared Hybrid Switched-Capacitor Converter for Direct 48 V to Point-of-Load Conversion," 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), Houston, TX, USA, 2022, pp. 1272-1278.
- [40] N. M. Ellis and R. C. N. Pilawa-Podgurski, "A Symmetric Dual-Inductor Hybrid Dickson Converter for Direct 48V-to-PoL Conversion," 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), Houston, TX, USA, 2022, pp. 1267-127.
- [41] Efficient Power Conversion, "Development Board EPC9205 Quick Start Guide," EPC9502 Datasheet, 2018.
- [42] D. Reusch, S. Biswas and M. de Rooij, "GaN Based Multilevel Intermediate Bus Converter for 48 V Server Applications," PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2018, pp. 1-8.