Source Reactance Lossless Switch (SRLS) for Soft-Switching Converters with Constant Switching Frequency

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***Abstract*—The mechanism of zero current switching and zero voltage switching is analyzed. The concept of Source Reactance Lossless Switch (SRLS) is proposed. The switch can be implemented in SRLS voltage rectifier and SRLS current rectifier. Using SRLS technique, several dc-to-dc resonant converters with constant switching frequency control are proposed, in which zero current switching and/or zero voltage switching can be maintained from full load to no load. Steady-state analysis is presented for two basic topologies, Parallel-SRLS resonant converter and Series-SRLS resonant converter. Experimental results are presented to verify the analysis.**

I. Introduction

HIGH SWITCHING frequency is needed to reduce the size of the power supply. Unfortunately, in Pulse Width Modulation (PWM) converters, high frequency switching is accompanied by high switching loss. The resonant converters are suitable to operate at high switching frequency since the switching loss is very low as compared with the PWM converters.

For the conventional resonant converters, [1]–[12], i.e., Parallel, Series, Series-Parallel converters, the switching loss is small because zero current switching (ZCS) or zero voltage switching (ZVS) can be maintained over a very wide range. The main limitation for these converters is that they use the frequency modulation (FM) technique to control the output voltage. One limitation of the frequency modulation control is that the filter inductor and filter capacitor have to be designed according to the lowest possible switching frequency. Another drawback is that the spectrum of the noise generated by the switching converter varies over a wide frequency range. In some circumstances, the switching frequency of the power supply must be kept at certain value to avoid interference with the other parts of the electronic equipment. It is, therefore, desirable to keep the switching frequency constant.

The PWM controlled resonant converters [13]–[19], also refer to as constant frequency clamped-mode resonant converters and phase-controlled resonant converters, have been proposed to keep the switching frequency constant. A dead time is introduced during which the resonant tank is short circuited. The output voltage is regulated by changing the dead time. Unfortunately, the desirable characteristic of low switching loss in the PWM controlled Series resonant converter can only be maintained at very limited line voltage and load current range [17]. In PWM controlled Parallel- and Series-Parallel resonant converters [15], [18], [19], switching losses for at least two electronic switches are present which are dominant at high switching frequency. Two of the full bridge switches experience high di/dt and dv/dt switching stresses and fast recovery diodes are needed.

It is, therefore, desirable to synthesize new resonant converter topologies that are controlled by constant switching frequency and, at the same time, are able to maintain zero current switching and/or zero voltage switching for all the switches over the entire line voltage and load current variation range to minimize the switching loss.

In this paper, the mechanism of zero current switching and zero voltage switching is analyzed. Based on the analysis, two lossless switches, named as Source Reactance Lossless Switch (SRLS) according to their composition, are proposed in Section II. One lossless switch operates at zero current switching and the other operates at zero voltage switching. Two basic resonant converters which are synthesized using the SRLS technique, namely, Parallel-SRLS and Series-SRLS resonant converters are proposed in Section III. Their output voltage can be controlled at constant switching frequency and the low switching loss characteristic for all the switches is maintained from no load to full load. Their steady-state characteristics are analyzed in Section IV, which shows that the added inductor or capacitor not only guarantees the zero current switching or zero voltage switching, respectively, but also is beneficial for the control characteristic of these converters. Several other topologies are proposed in Section V. In Section VI, two prototypes, Parallel-SRLS resonant converter and Series-SRLS resonant converter, are built to show the feasibility of the proposed technique and the validity of the analysis. Conclusions are made in Section VII.

II. Concept of Source Reactance Lossless Switch (SRLS)

Consider the switch arrangement shown in Fig. 1. At turn on, the current i_T can only rise slowly because of L_S. Zero current turn on is achieved. To turn off the switch at zero

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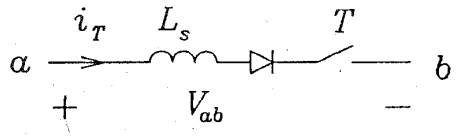


Fig. 1. Zero current switching.

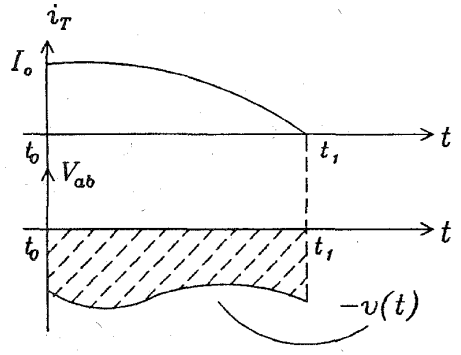


Fig. 2. Typical waveform at turn off for Fig. 1.

current, the energy stored in L_S must be, at first, transferred. One way to do so is to oscillate L_S with a resonant capacitor C_r (not shown in Fig. 1) during the on state of the switch. This is what the Zero Current Switching Quasi-Resonant Converter did [20]. However, the penalty for this is that large resonant current flows through the switch, which brings about large conduction loss.

An alternative and more efficient way to transfer the energy stored in L_S is to apply a negative voltage across the terminals "a" and "b" (Fig. 1). When the energy in L_S is completely absorbed by the negative source, the current in the switch becomes zero. Therefore, zero current turn off is achieved. Suppose that when T is conducting, the current is I_o at $t = t_0$ (Fig. 2). The energy stored in L_S is $W_{L_s} = \frac{1}{2} L_s I_o^2$. At $t = t_0$, a negative voltage, $-v(t)$, is applied across terminals "a" and "b". The current i_T is governed by the following equation

$$-v(t) = L_S \frac{di_T}{dt} \quad \text{with} \quad i_T(t_0) = I_o. \tag{1}$$

The solution is

$$i_T(t) = I_o - \frac{1}{L_S} \int_{t_0}^{t} v(t)\, dt. \tag{2}$$

In order that the energy stored in the inductor L_S be completely transferred so as to make the inductor current reduce to zero at t_1, the amplitude and the duration of the negative voltage should be large enough such that

$$\int_{t_0}^{t_1} v(t)\, dt \geq I_o L_s. \tag{3}$$

The physical meaning of (3) is that the Volt-Second area of the negative voltage, shown as the shaded area in Fig. 2, should be equal to or larger than the flux linkage of inductor L_S. The negative voltag can have any shape, as long as it satisfies (3).

By applying the duality principle, we consider the switching mechanism of the circuit shown in Fig. 3. The presence of the capacitor C_P makes the switch voltage v_T rise slowly

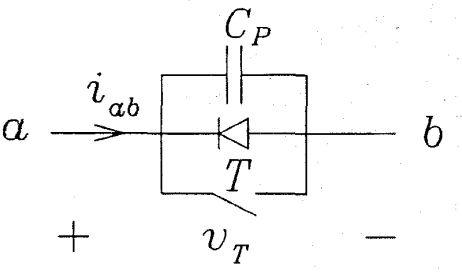


Fig. 3. Zero voltage switching.

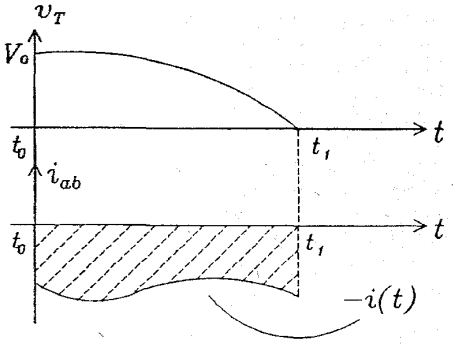


Fig. 4. Typical waveform at turn on for Fig. 3.

when the switch T is turned off. Thus, zero voltage turn off is achieved. In order to turn on the switch at zero voltage, the energy stored in C_P should at first be discharged before T is triggered on. One way to do this is to oscillate the C_P with a resonant inductor L_r (not shown in Fig. 3) during the off state of the switch. The oscillation makes the voltage across C_P decay to zero and then clamped at zero by the antiparallel diode. This is what the Zero-Voltage-Switching Quasi-Resonant-Converter did [21]. However, the penalty for this is high resonant voltage that appears across the switch.

An alternative and better method to discharge the parallel capacitor C_P is to apply a negative current through the branch "ab" before T is triggered on. If C_P is completely discharged by the negative current, T is turned on at zero voltage. Assume that before T is turned on, the voltage across C_P is V_o (Fig. 4). The energy stored in C_P is $W_{C_p} = \frac{1}{2} C_p V_o^2$. At $t = t_0$, a negative current, $-i(t)$, is applied through branch "ab". The relation between $i(t)$ and $v_T(t)$ is

$$C_p \frac{dv_T}{dt} = -i(t), \quad \text{with} \quad v_T(t_0) = V_o. \tag{4}$$

The solution is

$$v_T(t) = V_o - \frac{1}{C_p} \int_{t_0}^{t} i(t)\, dt. \tag{5}$$

In order to completely discharge the capacitor C_P so as to make the capacitor voltage reduce to zero at t1, the magnitude and the duration of the negative current should be large enough so that the following condition is satisfied

$$\int_{t_0}^{t_1} i(t)\, dt \geq C_p V_o. \tag{6}$$

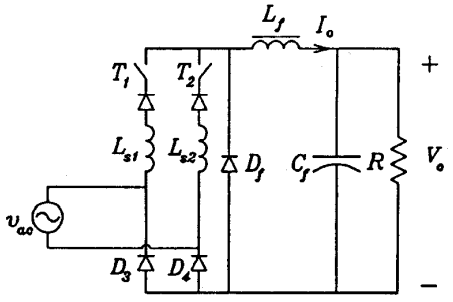


Fig. 5. SRLS voltage rectifier,

Equation (6) means that the Amp-Second area of the negative current, shown as the shaded area in Fig. 4, should be equal to or larger than the charges stored in capacitor C_P in order to achieve zero voltage turn on. Again, the shape of the negative current can be arbitrary, as long as it satisfies (6).

In the above two cases, the zero current switching and zero voltage switching are achieved by a negative source (voltage or current) and a reactive element (inductor or capacitor). This kind of switch is, therefore, named as **Source Reactance Lossless Switch (SRLS)**. This type of lossless switch is different from the present technique where zero current switching and zero voltage switching are achieved by resonance between inductor and capacitor.

A. SRLS Voltage Rectifier

The zero current switching configuration of Fig. 1 can be used in a controlled voltage rectifier, as shown in Fig. 5. The inductances, L_{S1} and L_{S2}, along with the alternating input voltage source, will provide zero current switching for T_1 and T_2. The energy stored in L_{S1} is absorbed by the negative part of the alternating voltage source, while the positive part of v_{ac} serves as the "negative" voltage needed to achieve zero current turn off for T_2. The output voltage V_o can be controlled by controlling the turn-on instant of the switches with respect to the input voltage source. The detailed operation is discussed in Section III.

The inductances L_{S1} and L_{S2} in the circuit shown in Fig. 5, play an important role in the operation. They are introduced intentionally to achieve zero current switching for the rectifier switches. The value of the inductance might be comparatively large to improve the characteristics of SRLS converters as shown in the analysis of Section IV. On the other hand, in the conventional single phase semiconverter [22], [23], the leakage inductances affect the operation of the circuit and have to be made as small as possible. The circuit in Fig. 5 is, therefore, given the name SRLS voltage rectifier to emphasize the zero current switching characteristic of T_1 and T_2.

B. SRLS Current Rectifier

A zero voltage switching controlled current rectifier can be obtained when the switch configuration of Fig. 3 is used, as shown in Fig. 6. It is the dual circuit of Fig. 5 and is called SRLS current rectifier. When diodes D_1 and D_4 or D_2 and D_3 conduct, the input current is rectified and flows through load. The voltage across the current source is the output voltage with the polarity determined by whether D_1 and D_4 or D_2 and

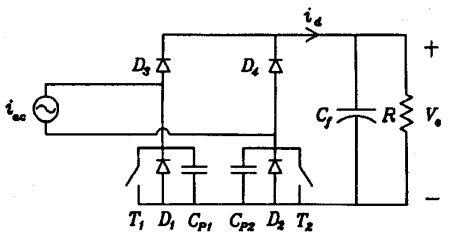


Fig. 6. SRLS current rectifier.

D_3 conduct. When the switch pair T_1 and D_2 or T_2 and D_1 conducts, the current source is short circuited and its voltage is zero. The output current is also zero at this interval. Therefore, by changing the conduction time of T_1 and T_2, the average output current and, consequently, the output voltage can be regulated.

The presence of C_{P1} and C_{P2} ensures the zero voltage turn off of T_1 and T_2. The energy stored in C_{P1} is transferred to the negative part of the current source to achieve zero voltage turn on for T_1. The positive part of i_{ac} is used to discharge the capacitor C_{P2} to achieve zero voltage turn on for T_2. Therefore, zero voltage switching is achieved by the alternating current source and the capacitor. It is noted that the waveform of i_{ac} can be arbitrary. Its operation will be discussed in more detail in the next section.

The SRLS current rectifier is the dual circuit of the SRLS voltage rectifier and it is a new topology. Zero voltage switching is achieved for the rectifier switches. The self turn-off devices must be used. It is also noted that the diode D_1 and D_2 are reverse biased by T_1 and T_2, respectively. Thus, the problem caused by the reverse recovery of diode is eliminated and low speed diode can be used. This characteristic is desirable when MOSFET is employed as switches since it makes full use of the antiparallel diode and the junction capacitor constitutes part of C_P.

III. Basic Converter Topologies Using SRLS Technique

As described above, the switches in the SRLS voltage rectifier operates at zero current switching mode, while the switches in the SRLS current rectifier operates at zero voltage switching mode. The switching loss is, therefore, very small. The requirement to achieve this desirable characteristic is an alternating voltage that can absorb the energy stored in the inductor or an alternating current that can discharge the energy stored in the capacitor.

A. Parallel-SRLS Resonant Converter

When the SRLS voltage rectifier is fed by a high frequency Parallel resonant inverter, as shown in Fig. 7, Parallel-SRLS resonant converter is obtained. The inductances L_{S1} and L_{S2} in series with each rectifier switch are substituted by a single inductor L_S and put at the input of the rectifier (Fig. 7). There are several benefits in doing so: (1) the number of components is reduced, (2) it is easier to implement L_S as there is no dc component for L_S and (3) when isolation transformer is used, its leakage inductance can be utilized as part of L_S.

When the switching frequency f_S is larger than the resonant frequency f_r, $f_r = 1/(2\pi\sqrt{L_r C_r})$, the key waveforms of the

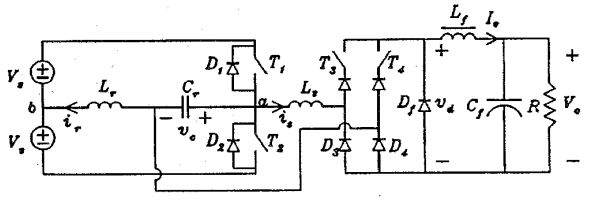


Fig. 7. Parallel-SRLS resonant converter.

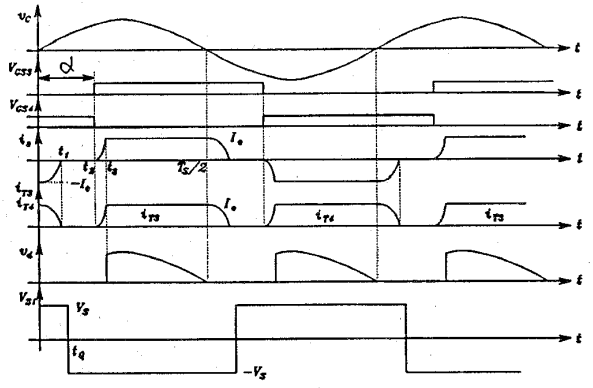


Fig. 8. Key waveforms for Parallel-SRLS resonant converter.

Parallel-SRLS resonant converter are given in Fig. 8, where V_{S1} is the voltage across point "a" and "b" in Fig. 7. The waveform of v_C is quasi-sinusoidal. The starting time is selected at $v_c = 0$. There is a time shift t_Q between v_c and V_{S1}, as shown in Fig. 8. Four operating states exist in each half cycle. Before the capacitor voltage vC changes polarity, T_4 and D_3 conduct and $i_s = -I_o$.

State 1 $[0, t_1]$: D_f, T_4, and D_3 conduct. The equivalent circuit is shown in Fig. 9(a), where the V_{S1} is the voltage between point "a" and "b" in Fig. 7. The conducting devices for the SRLS voltage rectifier are also identified in the figure. The voltage v_C forces i_S changes from $-I_o$ to zero. The current in T_4 also falls. At $t = t_1, i_S$ reaches zero and T_4 is turned off at zero current. In order to achieve zero current turn off for T_4, T_3 can not be triggered until $t = t_1$.

State 2 $[t_1, t_2]$: Neither T_3 nor T_4 conducts and i_S is zero. The output current freewheels through D_f, as shown in Fig. 9(b).

State 3 $[t_2, t_3]$: At $t = t_2$, i.e., at turn on delay angle α, T_3 is triggered on. The relation between t_2 and α is

$$t_2 = \frac{\alpha}{360} T_s. \tag{7}$$

The current i_S, as well as the current in T_3, rises through T_3 and D_4, as shown in Fig. 9(c).

State 4 $[t_3, T_S/2]$: At $t = t_3, i_S$ reaches the output current and D_f is turned off. The power is delivered to the load via T_3 and D_4. The equivalent circuit is given in Fig. 9(d). The first half cycle ends when v_C falls to zero again. The next half cycle repeats the similar procedure.

In the case of Parallel resonant inverter, the amplitude of the capacitor voltage v_C is usually high enough so that the energy stored in L_S when T_3 or T_4 conducts can be absorbed and zero current switching for T_3 and T_4 can be obtained from full load to no load as the condition for zero current

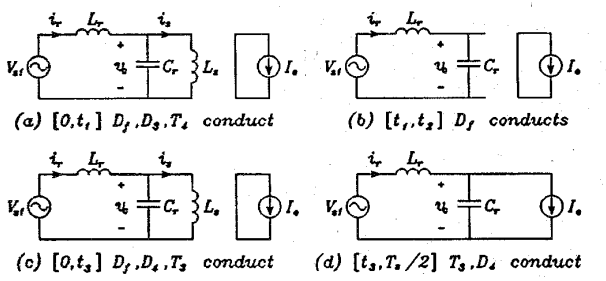


Fig. 9. Equivalent circuit of Parallel-SRLS resonant converter at each half cycle.

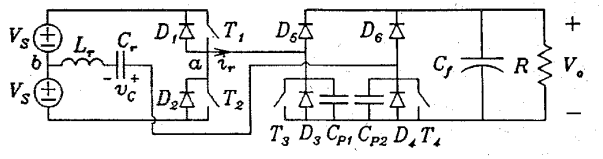


Fig. 10. Series-SRLS resonant converter.

switching is independent of the load current. The inductor L_S is used to shape the current waveform so as to achieve zero current switching for T_3 and T_4 and is effective only during the transition intervals of T_3 and T_4.

The switching condition of the inverter switch T_1 and T_2 of the Parallel-SRLS resonant converter is determined by the relative quantity of the switching frequency f_S and resonant frequency f_r. When the converter operates at below resonance, i.e., $f_s < f_r, T_1$ and T_2 operate at zero current turn off. If the converter operates at above resonance, i.e., $f_s > f_r$, zero voltage turn on for T_1 and T_2 is obtained. In both cases, T_3 and T_4 operate at zero current switching. By changing the turn on time of T_3 and T_4 with respect to v_C, the output voltage can be controlled at constant switching frequency.

B. Series-SRLS Resonant Converter

Fig. 10 gives the topology of Series-SRLS dc-to-dc resonant converter, where Series resonant inverter is used. As the output of the Series resonant inverter is an alternative current, the SRLS current rectifier is employed. In the case of switching frequency f_S higher than the resonant frequency $f_r, f_r = 1/(2\pi\sqrt{L_r C_r})$, key waveforms are given in Fig. 11, where V_{S1} is the voltage across point "a" and "b" in Fig. 10. The waveform of i_r is quasi-sinusoidal. The starting point is chosen at $i_r = 0$. There is a time shift t_R between i_r and V_{S1} as shown in the figure. In the steady state, there are four operating states during each half cycle. Just before the inductor current ir changes polarity, D_3 and D_6 conducts and T_3 is supplied with gate signal. The power is delivered to the load and $v_p = -V_o$.

State 1 $[0, t_1]$: T_3 is turned on at zero voltage. The current ir flows through T_3 and C_{P2} to discharge C_{P2}. The equivalent circuit is given in Fig. 12(a), where V_{S1} is the voltage between point "a" and "b" in Fig. 10. The conducting devices for the SRLS current rectifier are also shown in the figure. The voltage v_P changes from $-V_o$ and reaches zero at $t = t_1$. At the same time the voltage across T_4 falls from V_o to zero. In order to obtain zero voltage turn on for T_4, T_3 should not be turned off until $t = t_1$.

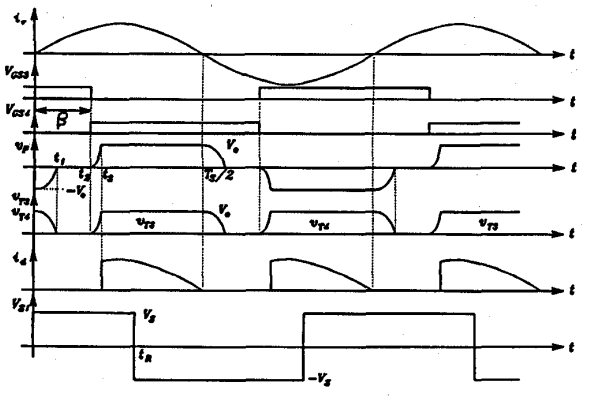


Fig. 11. Key waveforms for Series-SRLS resonant converter.

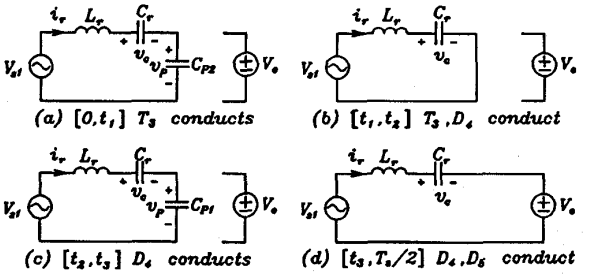


Fig. 12. Equivalent circuit of Series-SRLS resonant converter at each half cycle

State 2 $[t_1, t_2]$: The resonant current circulates through T_3 and D_4 and the output current is zero, as shown in Fig. 12(b).

State 3 $[t_2, t_3]$: At $t = t_2$, i.e., at turn off delay angle β, T_3 is turned off. The relation between t_2 and β is defined by:

$$t_2 = \frac{\beta}{360} T_s. \tag{8}$$

The inductor current ir flows through C_{P1} and D_4 and the voltage v_P, i.e. v_{T3}, rises slowly. The equivalent circuit is given in Fig. 12(c).

State 4 $[t_3, T_S/2]$: At $t = t_3, v_P$ equals to the value of the output voltage V_o and D_4 and D_5 conduct. The inductor current flows to the load. The power is transferred to the output at this state, as shown in Fig. 12(d). The first half cycle ends when i_r falls to zero again. The next half cycle is similar.

For the Series resonant inverter, the amplitude of the inductor current i_r is usually high enough to discharge capacitor C_{P1} or C_{P2} completely and zero voltage turn on can be achieved for the rectifier switch T_3 and T_4 from no load to full load because the condition to achieve zero voltage switching is independent of the load current. The capacitors, C_{P1} and C_{P2}, are employed to shape the voltage waveforms of T_3 and T_4 and are effective only during the switching transition periods of T_3 and T_4.

The switching condition for the inverter switch T_1 and T_2 of the Series-SRLS resonant converter is determined by the relative value of f_S and f_r. Zero voltage turn on is obtained when $f_s > f_r$. While zero current turn off is obtained when $f_s < f_r$. In bath cases, T_3 and T_4 operate at zero voltage switching. By changing the turn off delay angle β with respect to i_r, the output voltage can be regulated.

IV. Steady-State Analysis

The steady-state characteristics of the Parallel-SRLS resonant converter and Series-SRLS resonant converter are analyzed in this section. The following assumptions are made to simplify the analysis

1) the filter inductor and capacitor are large;
2) the switches are ideal;
3) there is no loss in the circuit;
4) the effect of the snubber is neglected;
5) switching frequency is higher than the resonant frequency.

Per unit system is employed so that the derived result is applicable to general case. The base quantities are chosen as

$$V_{base} = V_s, \quad Z_{base} = \sqrt{L_r/C_r}, \quad I_{base} = V_{base}/Z_{base},$$
$$\omega_{base} = 1/\sqrt{L_r C_r}, \quad f_{base} = \omega_{base}/(2\pi) = f_r,$$
$$T_{base} = 1/f_{base}, \quad L_{base} = Z_{base}/\omega_{base} = L_r,$$
$$C_{base} = 1/(Z_{base}\omega_{base}) = C_r$$

In the derivation that follows, all the quantities are in per unit.

A. Parallel-SRLS Resonant Converter

The circuit for analysis and the related symbols are shown in Fig. 7, the key waveforms are shown in Fig. 8 and the equivalent circuit during various states are shown in Fig. 9. From the above discussion, the turn on delay angle for T_3 is α degrees lagging the zero crossing point (from negative to positive) of the capacitor voltage v_C and the turn on signal for T_4 is 180° later. Only the first half cycle is considered because the next half cycle is the same except the polarity. State 1 begins when $v_C = 0$ with the initial condition

$$v_C(0) = 0, \quad i_r(0) = I_{r0}, \quad i_s(0) = -I_o. \tag{9}$$

State 1 $[0, t_1]$: The equivalent circuit is given in Fig. 9(a). The voltage applied to the resonant tank is V_{S1}. At first, T_1 or D_1 conducts and $V_{s1} = V_S$. At $t = t_Q, T_2$ or D_2 conducts and $V_{s1} = -V_S$. Therefore,

$$V_{s1} = \begin{cases} V_s, & 0 \le t \le t_Q \\ -V_s, & t_Q < t \le \frac{1}{2} T_s. \end{cases} \tag{10}$$

The state equations for State 1 are

$$C_r \frac{dv_C}{dt} = 2\pi(i_r - i_s) \tag{11a}$$
$$L_r \frac{di_r}{dt} = 2\pi(V_{S1} - v_C) \tag{11b}$$
$$L_s \frac{di_s}{dt} = 2\pi v_C \tag{11c}$$

with the initial condition (9), the solution of (11) can be found as

$$v_C(t) = (1 - \cos 2\pi\omega_1 t)\frac{L_s}{L_s + L_r} V_{s1} + \frac{\omega_1 L_s L_r (I_{r0} + I_o)}{L_s + L_r} \sin 2\pi\omega_1 t \tag{12a}$$

$$i_r(t) = \frac{L_s(I_{r0}+I_o)}{L_s+L_r}\cos 2\pi\omega_1 t + \frac{L_s V_{s1}}{\omega_1 L_r(L_s+L_r)} \cdot \sin 2\pi\omega_1 t + \frac{2\pi V_{s1} t}{L_s+L_r} + \frac{L_r I_{r0}+L_s I_o}{L_s+L_r} \quad (12b)$$

$$i_s(t) = -\frac{L_r(I_{r0}+I_o)}{L_s+L_r}\cos 2\pi\omega_1 t - \frac{V_{s1}}{\omega_1(L_s+L_r)} \cdot \sin 2\pi\omega_1 t + \frac{2\pi V_{s1} t}{L_s+L_r} + \frac{L_r I_{r0}-L_s I_o}{L_s+L_r} \quad (12c)$$

where

$$\omega_1 = \sqrt{(L_s+L_r)/(L_s L_r C_r)}. \quad (13)$$

At $t = t_1, i_s(t) = 0, T_4$ stops conducting and the circuit enters State 2 with the initial condition derived by (12)

$$i_r(t_1) = I_{r1}, \quad v_c(t_1) = V_{c1}, \quad i_s(t_1) = 0. \quad (14)$$

State 2 $[t_1, t_2]$: The equivalent circuit for this state is shown in Fig. 9(b). The state equations are:

$$C_r\frac{dv_C}{dt} = 2\pi i_r \quad (15a)$$

$$L_r\frac{di_r}{dt} = 2\pi(V_{s1}-v_C) \quad (15b)$$

$$L_s\frac{di_s}{dt} = 0. \quad (15c)$$

Its solution is

$$v_C(t) = I_{r1}\sin 2\pi\omega_r(t-t_1) + V_{C1}\cos 2\pi\omega_r(t-t_1) + V_{s1}[1-\cos 2\pi\omega_r(t-t_1)] \quad (16a)$$

$$i_r(t) = I_{r1}\cos 2\pi\omega_r(t-t_1) - \frac{V_{C1}-V_{s1}}{Z_r} \cdot \sin 2\pi\omega_r(t-t_1) \quad (16b)$$

$$i_s(t) = 0. \quad (16c)$$

At $t = t_2$, where t_2 is the control variable defined by the turn off delay angle α, (7), T_3 is triggered on and the circuit enters State 3 with the initial conditions obtained from (16)

$$v_C(t_2) = V_{C2}, \quad i_r(t_2) = I_{r2}, \quad i_s(t_2) = 0. \quad (17)$$

State 3 $[t_2, t_3]$: The equivalent circuit is shown in Fig. 9(c). The state equations are the same as those of State 1, but the initial conditions are different. The solution with initial condition (17) is:

$$v_C(t) = \left(V_{C2} - \frac{L_s V_{s1}}{L_s+L_r}\right)\cos 2\pi\omega_1(t-t_2) + \frac{\omega_1 L_s L_r I_{r2}}{L_s+L_r} \cdot \sin 2\pi\omega_1(t-t_2) + \frac{L_s V_{s1}}{L_s+L_r} \quad (18a)$$

$$i_r(t) = -\frac{V_{C2}-\frac{L_s V_{s1}}{L_s+L_r}}{\omega_1 L_r}\sin 2\pi\omega_1(t-t_2) + \frac{L_s I_{r2}}{L_s+L_r} \cdot \cos 2\pi\omega_1(t-t_2) + \frac{2\pi V_{s1}(t-t_2)}{L_s+L_r} + \frac{I_{r2}L_r}{L_s+L_r} \quad (18b)$$

$$i_s(t) = [1-\cos 2\pi\omega_1(t-t_2)]\frac{L_r L_{r2}}{L_s+L_r} + \frac{V_{C2}-\frac{L_s V_{s1}}{L_s+L_r}}{\omega_1 L_s} \cdot \sin 2\pi\omega_1(t-t_2) + \frac{2\pi V_{s1}(t-t_2)}{L_s+L_r}. \quad (18c)$$

At $t = t_3$, the current in L_S reaches the output current. The circuit enters State 4 with the initial condition derived from (18)

$$v_C(t_3) = V_{C3}, \quad i_r(t_3) = I_{r3}, \quad i_s(t_3) = I_o. \quad (19)$$

State 4 $[t_3, T_S/2]$: Fig. 9(d) shows the equivalent circuit for this state. The power is delivered from the resonant branch to the load. The state equations are

$$C_r\frac{dv_C}{dt} = 2\pi(i_r - I_o) \quad (20a)$$

$$L_r\frac{di_r}{dt} = 2\pi(V_{s1}-v_C) \quad (20b)$$

$$L_s\frac{di_s}{dt} = 0. \quad (20c)$$

Its solution is

$$v_C(t) = (I_{r3}-I_o)Z_r\sin 2\pi\omega_r(t-t_3) + (V_{C3}-V_{s1}) \cdot \cos 2\pi\omega_r(t-t_3) + v_{s1} \quad (21a)$$

$$i_r(t) = -\frac{V_{C3}-v_{s1}}{Z_r}\sin 2\pi\omega_r(t-t_3) + (I_{r3}-I_o) \cdot \cos 2\pi\omega_r(t-t_3) + I_o \quad (21b)$$

$$i_s(t) = I_o. \quad (21c)$$

At steady-state operation, there is a particular t_Q such that when $t = \frac{1}{2}T_s, v_C(t) = 0$, and $i_r(t) = -I_o$.

The output voltage V_O can be calculated by averaging the capacitor voltage $v_C(t)$ from t_3 to $T_S/2$, (21a), and is derived as follows:

For $t_Q \le t_3$:

$$V_o = \frac{(I_{r3}-I_o)Z_r}{\pi\omega_r T_s}\left[1-\cos 2\pi\omega_r\left(\frac{1}{2}T_s - t_3\right)\right] + \frac{V_{C3}+V_s}{\pi\omega_r T_s}\sin 2\pi\omega_r\left(\frac{1}{2}T_s - t_3\right) - \frac{2V_s\left(\frac{1}{2}T_s - t_3\right)}{T_s}. \quad (22a)$$

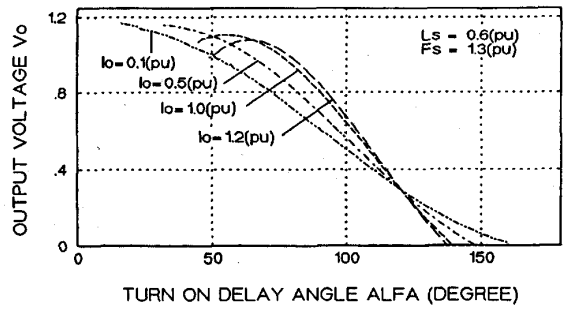
For $t_Q > t_3$:

$$V_o = \frac{(I_{r3}-I_o)Z_r}{\pi\omega_r T_s}[1-\cos 2\pi\omega_r(t_Q-t_3)] + \frac{V_{C3}-V_s}{\pi\omega_r T_s}\sin 2\pi\omega_r(t_Q-t_3) + \frac{(I_{r30}-I_o)Z_r}{\pi\omega_r T_s}\left[1-\cos 2\pi\omega_r\left(\frac{1}{2}T_s - t_Q\right)\right] + \frac{V_{C30}+V_s}{\pi\omega_r T_s}\sin 2\pi\omega_r\left(\frac{1}{2}T_s - t_Q\right) + \frac{2V_s\left(2t_Q - \frac{1}{2}T_s - t_3\right)}{T_s} \quad (22b)$$

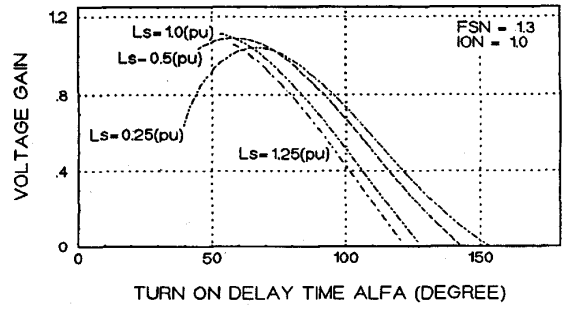
where

$$I_{r30} = I_o + (I_{r3}-I_o)\cos 2\pi\omega_r(t_Q-t_3) - \frac{V_{c3}-V_s}{Z_r} \cdot \sin 2\pi\omega_r(t_Q-t_3) \quad (23a)$$

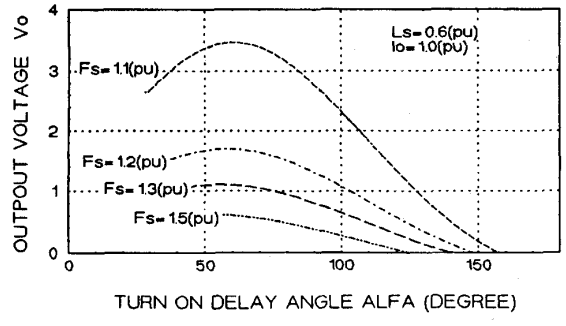
$$V_{C30} = (I_{r3}-I_o)Z_r\sin 2\pi\omega_r(t_Q-t_3) + (V_{C3}-V_s) \cdot \cos 2\pi\omega_r(t_Q-t_3). \quad (23b)$$



(a)



(b)



(c)

Fig. 13. Characteristics of the Parallel-SRLS resonant converter (a) Effect of I_o (b) Effect of L_S (c) Effect of f_S.

Based on the above equations, the characteristics of the Parallel-SRLS resonant converter can be analyzed. In the analysis, the input voltage is taken as one per unit. Fig. 13(a) gives the output voltage versus turn on delay angle a at different output current. It shows that by changing the α, the output voltage can be kept constant when load current changes while keeping the switching frequency fixed. It is noted that there is a minimum a below which the desirable characteristic of zero current turn off for T_3 and T_4 is lost. This is because of the presence of State 1 when the current in one switch, such as T_4, should, at first, decay to zero before the other switch, such as T_3, is able to conduct. This is a significant difference with the characteristic of the conventional controlled rectifier [22], [23].

The effect of L_S on the output voltage is also studied and the result is given in Fig. 13(b). For smaller L_S, when α increases, the output voltage increases at first and then decreases. The smaller the L_S is, the larger the difference between the peak output voltage and the initial value when $\alpha = \alpha_{\min}$. This fact is not desirable for the design of control circuit. For larger L_S, such as $L_s = 1.0, 1.25(pu)$, one particular α corresponds to one value of output voltage. Also, larger value of L_S yields the smaller variation range of α necessary to regulate the output voltage from maximum to zero. It can also be observed from Fig.13(b) that there is a particular L_S which corresponds to the highest attainable voltage gain.

The introduction of the L_S is essential to achieve zero current switching for T_3 and T_4. On the other hand, Fig.13(b) illustrates that larger L_S also plays the beneficial role (every a corresponds to a single value of V_O) for the control to output characteristic. It may be noted that in the conventional semi-converter, the leakage inductances affect the output voltage and normally is kept as small as possible.

Fig. 13(c) gives the effect of the switching frequency f_S on the output voltage. When f_S is close to the resonant frequency f_r, the voltage gain is high and it is more sensitive to the variation of switching frequency. The higher the f_S, the smaller the variation range of a necessary to regulate the output voltage from maximum to zero.

B. Series-SRLS Resonant Converter

The circuit for analysis and the relevant symbols are given in Fig. 10. The key waveforms are shown in Fig. 11 and the equivalent circuit during various states are shown in Fig. 12. From the above discussion, the turn off delay angle for T_3 is β degrees lagging the zero crossing point of the inductor current i_r and the turn off signal for T_4 is 180 degrees later. Only the first half cycle is analyzed since the next half cycle is the same except the polarity. State 1 begins when $i_r(0) = 0$ with the initial condition:

$$v_C(0) = V_{C0}, \quad i_r(0) = 0, \quad v_P(0) = -V_o. \tag{24}$$

State 1 $[0, t_1]$: The equivalent circuit is given in Fig. 12(a). Switch T_3 is turned on at zero voltage and the resonant current flows through T_3 to discharge C_{P2}. The voltage applied to the resonant tank is V_{S1}. At first, when D_1 or T_1 conducts. After T_1 is turned off at $t = t_R$, the switch pair T_2, D_2 conducts and $V_{s1} = -V_s$. Therefore,

$$V_{s1} = \begin{cases} V_s, & 0 \le t \le t_R \\ -V_s, & t_R < t \le \frac{1}{2} T_s. \end{cases} \tag{25}$$

The state equations for State 1 are

$$L_r \frac{di_r}{dt} = 2\pi(V_{s1} - v_C - v_p) \tag{26a}$$

$$C_r \frac{dv_C}{dt} = 2\pi i_r \tag{26b}$$

$$C_p \frac{dv_p}{dt} = 2\pi i_r. \tag{26c}$$

The solution of (26) can be found as

$$i_r(t) = \frac{V_o + V_{s1} - V_{C0}}{Z_1} \sin 2\pi\omega_1 t \tag{27a}$$

$$v_c(t) = \frac{C_p(V_{C0} - V_o - V_{s1})}{C_p + C_r} \cos 2\pi\omega_1 t$$

$$+\frac{C_pV_{s1}+C_rV_{C0}+C_pV_o}{C_p+C_r} \tag{27b}$$

$$v_p(t)=\frac{C_r(V_{C0}-V_o-V_{s1})}{C_p+C_r}\cos 2\pi\omega_1 t + \frac{C_rV_{s1}-C_pV_o-C_rV_{C0}}{C_p+C_r} \tag{27c}$$

where

$$\omega_1=\sqrt{(C_r+C_p)/C_rC_pL_r}$$
$$Z_1=\sqrt{L_r(C_r+C_p)/C_rC_p}. \tag{28}$$

At $t=t_1, C_{P2}$ is completely discharged, $v_p(t_1)=0$. D_4 conducts. The circuit enters State 2 with the initial conditions derived from (27)

$$v_C(t_1)=V_{C1},\quad i_r(t_1)=I_{r1},\quad v_p(t_1)=0. \tag{29}$$

State 2 $[t_1,t_2]$: The equivalent circuit is shown in Fig. 12(b). The state equations are

$$L_r\frac{di_r}{dt}=2\pi(V_{s1}-v_C) \tag{30a}$$
$$C_r\frac{dv_C}{dt}=2\pi i_r \tag{30b}$$
$$C_p\frac{dv_p}{dt}=0. \tag{30c}$$

Its solution is

$$i_r(t)=I_{r1}\cos 2\pi\omega_r(t-t_1)-\frac{V_{C1}-V_{s1}}{Z_r}\cdot\sin 2\pi\omega_r(t-t_1) \tag{31a}$$
$$v_c(t)=I_{r1}Z_r\sin 2\pi\omega_r(t-t_1)+V_{C1}-V_{s1})\cdot\cos 2\pi\omega_r(t-t_1)+V_{s1} \tag{31b}$$
$$v_p(t)=0. \tag{31c}$$

At $t=t_2$, where t_2 is the turn off delay time defined by (8), the switch T_3 is turned off. The circuit enters State 3 with the initial conditions

$$i_r(t_2)=I_{r2},\quad v_C(t_2)=V_{C2},\quad v_p(t_2)=0. \tag{32}$$

State 3 $[t_2\quad t_3]$: The equivalent circuit is given in Fig. 12(c). The state equations are the same as those of State 1. However, the initial conditions are expressed by (32). The solution for State 3 is

$$i_r(t)=I_{r2}\cos 2\pi\omega_1(t-t_2)-\frac{V_{C2}-V_{s1}}{Z_1}\cdot\sin 2\pi\omega_1(t-t_2) \tag{33a}$$
$$v_C(t)=\frac{I_{r2}}{\omega_1C_r}\sin 2\pi\omega_1(t-t_2)+\frac{C_pV_{s1}+C_rV_{C2}}{C_p+C_r}+\frac{C_p(V_{C2}-V_{s1})}{C_p+C_r}\cos 2\pi\omega_r(t-t_2) \tag{33b}$$
$$v_p(t)=\frac{I_{r2}}{\omega_1C_p}\sin 2\pi\omega_1(t-t_2)+\frac{C_rV_{s1}-C_rV_{C2}}{C_p+C_r}+\frac{C_r(V_{C2}-V_{s1})}{C_p+C_r}\cos 2\pi\omega_1(t-t_2). \tag{33c}$$

where ω_1 and Z_1 are defined by (28).

This state ends at $t=t_3$ when v_P reaches the output voltage V_o and the diode D_5 is turned on. The initial conditions for the next state are

$$i_r(t_3)=I_{r3},\quad v_C(t_3)=V_{C3},\quad v_p(t_3)=V_o. \tag{34}$$

State 4 $[t_3,T_s/2]$: The equivalent circuit for this state is shown in Fig. 12(d). The power is transferred to the load at this state via D_5 and D_4. The state equations are:

$$L_r\frac{di_r}{dt}=2\pi(V_{s1}-V_o-v_C) \tag{35a}$$
$$C_r\frac{dv_C}{dt}=2\pi i_r \tag{35b}$$
$$C_p\frac{dv_p}{dt}=0. \tag{35c}$$

Its solution is

$$i_r(t)=I_{r3}\cos 2\pi\omega_r(t-t_3)-\frac{V_{C3}+V_o-V_{s1}}{Z_r}\cdot\sin 2\pi\omega_r(t-t_3) \tag{36a}$$
$$v_c(t)=(V_{C3}+V_o-V_{s1})\cos 2\pi\omega_r(t-t_3)+I_{r3}Z_r\cdot\sin 2\pi\omega_r(t-t_3)+V_{s1}-V_o \tag{36b}$$
$$v_p(t)=V_o. \tag{36c}$$

In steady-state operation, there is a particular t_R such that when $t=\frac{1}{2}T_s, v_C(\frac{1}{2}T_s)=-V_{C0}$ and $i_r(\frac{1}{2}T_s)=0$.

The steady-state output current can be calculated by averaging the resonant current from t_3 to $T_S/2$, (36a), and can be calculated as

For $t_R\le t_3$

$$I_o=\frac{I_{r3}}{\pi\omega_rT_s}\sin 2\pi\omega_r\left(\frac{1}{2}T_s-t_3\right)-\frac{V_{C3}+V_o+V_s}{\pi Z_r\omega_rT_s}\cdot\left[1-\cos 2\pi\omega_r\left(\frac{1}{2}T_s-t_3\right)\right]. \tag{37a}$$

For $t_R>t_3$

$$I_o=\frac{I_{r3}}{\pi\omega_rT_s}\sin 2\pi\omega_r(t_R-t_3)-\frac{V_{C3}+V_o-V_s}{\pi Z_r\omega_rT_s}\cdot[1-\cos 2\pi\omega_r(t_R-t_3)]+\frac{I_{r30}}{\pi\omega_rT_s}\sin 2\pi\omega_r\left(\frac{1}{2}T_s-t_R\right)-\frac{V_{C30}+V_o+V_{s1}}{\pi Z_r\omega_rT_s}\cdot\left[1-\cos 2\pi\omega_r\left(\frac{1}{2}T_s-t_R\right)\right] \tag{37b}$$

where

$$I_{r30}=I_{r3}\cos 2\pi\omega_r(t_R-t_3)-\frac{V_{C3}+V_o-V_s}{Z_r}\cdot\sin 2\pi\omega_r(t_R-t_3) \tag{38a}$$
$$V_{C30}=(V_{C3}+V_o-V_s)\cos 2\pi\omega_r(t_R-t_3)+I_{r3}Z_r\cdot\sin 2\pi\omega_r(t_R-t_3)+V_s-V_o. \tag{38b}$$

From the above equations, the characteristics of the Series-SRLS resonant converter can be obtained. The input voltage is taken as one per unit value in the calculation. Fig. 14(a) shows the relationship between the output current and the control input β at different output voltage. By changing the turn off delay angle β, the output voltage can be kept constant when the load current changes. It also shows that for a particular output

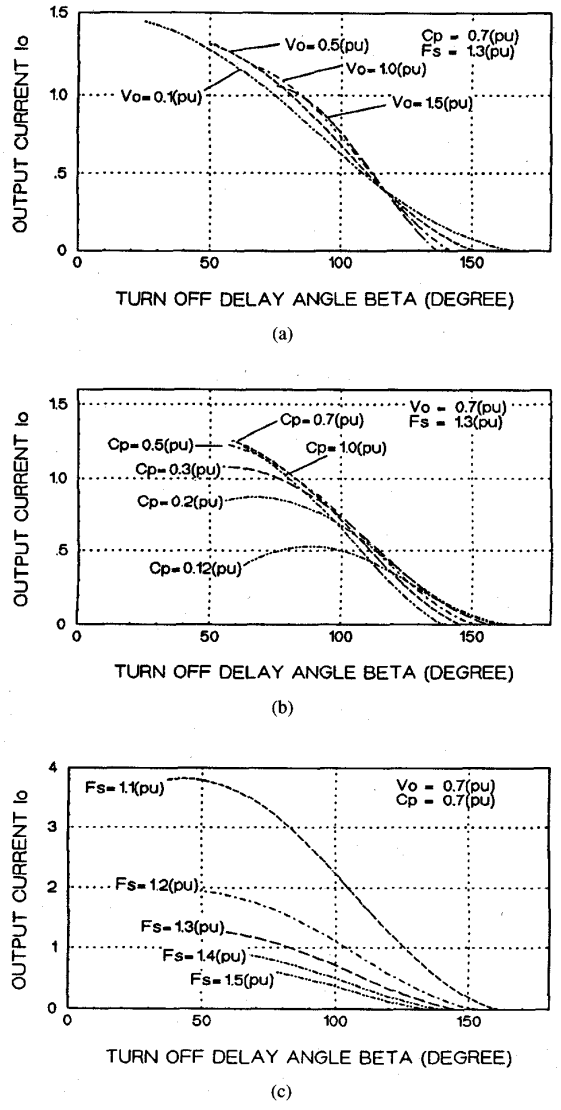


Fig. 14. Characteristics of the Series-SRLS resonant converter. (a) Effect of V_O (b) Effect of C_P (c) Effect of f_S.

voltage, there is a minimum delay angle, $\beta_{\min}$, below which the desirable zero voltage turn on for T_3 and T_4 is lost. This is because of the presence of the State 1, when the capacitor, such as C_{P2}, is discharged by the inductor current ir through one rectifier switch, such as T_3. Only after the capacitor, e.g., C_{P2}, is completely discharged, the gate signal of the switch, e.g., T_3 can be removed. The higher the output voltage, the more charges stored in the capacitor and, therefore, the larger the $\beta_{\min}$.

Fig. 14(b) shows the effect of C_P on the control characteristic of Series-SRLS resonant converter. When C_P increases, the maximum attainable output current also increases. However, when C_P becomes too large, the current gain drops instead. For larger C_P, there is a unique value of output current for each turn off delay angle β. From the discussion above and in Section III, it is shown clearly that on one hand, the capacitors

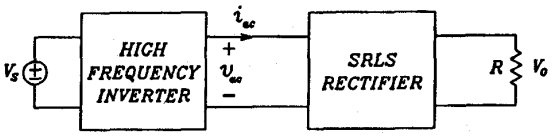


Fig. 15. Block diagram of dc-to-dc resonant converter using SRLS technique.

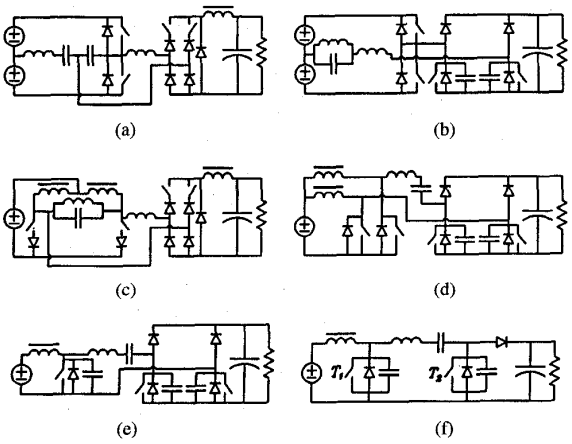


Fig. 16. Several other resonant converters using SRLS technique.

C_{P1} and C_{P2} are essential for zero voltage switching of the rectifier switch T_3 and T_4, on the other hand, the addition of these capacitors also improves the control characteristic of the converter.

The effect of switching frequency f_S on the control characteristic is shown in Fig. 14(c). Higher current gain can be obtained when the switching frequency f_S is close to the resonant frequency f_r. However, when f_S is close to f_r, the current gain is more sensitive to the drift of the switching frequency.

V. Other Converter Topologies Using SRLS Technique

Fig. 15 gives the general diagram of dc-to-dc resonant converter using SRLS technique. If the output of the inverter is an ac voltage, SRLS voltage rectifier is used and the rectifier switches turn on and off at zero current. When the inverter output is an alternating current, SRLS current rectifier should be employed and zero voltage switching for the rectifier switch is achieved. The output voltage can be controlled by changing the turn on delay, α, or turn off delay, β, of the SRLS rectifier.

Fig. 16 gives several other resonant converters that can be synthesized by the Source Reactance Lossless Switch technique. The output voltage of these converters can be regulated by changing the turn on or turn off delay angle of SRLS rectifier. Zero current switching or zero voltage switching for all switches can be maintained when load current changes from zero to maximum and the input voltage changes from the highest to the lowest value.

Fig. 16(a) shows the voltage fed Series-Parallel-SRLS converter. The inverter is Series-Parallel type, or LCC type [10], [11], and SRLS voltage rectifier is used since the output of LCC type inverter is a voltage. When the inverter consists of the so-called LLC type resonant inverter [24], LLC-SRLS

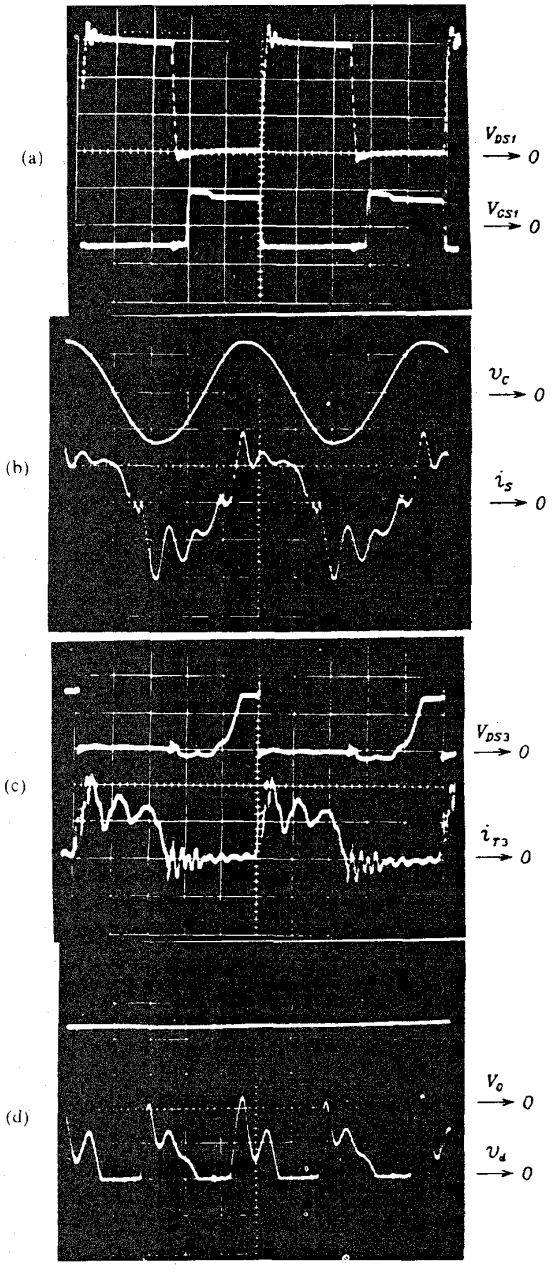


Fig. 17. Measured waveforms for Parallel-SRLS converter. (a) upper trace: V_{DS1} 10 V/div, lower trace: V_{GS1} 10 V/div. (b) upper trace: V_C 10 V/div, lower trace: i_S 1 A/div. (c) upper trace: V_{DS3} 5 V/div, lower trace: i_{T3} 1 A/div. (d) upper trace: V_o 5 V/div, lower trace: v_d 10 V/div. Horizontal: 2 μS/div.

resonant dc-to-dc converter is obtained, as shown in Fig. 16(b). In this case, the SRLS current rectifier is used. Fig. 16(c) is the current fed Parallel-SRLS converter where SRLS voltage rectifier is used. Fig. 16(d) shows the current fed Series-SRLS resonant converter, where SRLS current rectifier is employed since the output of the inverter is a current. Another interesting topology is the Class-E-SRLS converter, as shown in Fig. 16(e), where the Class-E power amplifier [25] is used

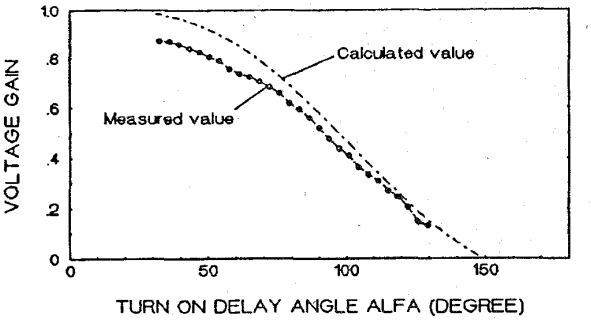


Fig. 18. Measured waveforms for Series-SRLS converter. (a) Upper trace: V_{GS1} 10 V/div, lower trace: V_{DS1} 10 V/div. (b) Upper trace: V_p 10 V/div, lower trace: i_r 1 A/div. (c) Upper trace: V_{GS3} 5 V/div, lower trace: V_{DS3} 1 A/div. (d) Upper trace: V_o 10 V/div, lower trace: i_d 2.5 A/div. Horizontal: 2 μS/div.

as the inverter and SRLS current rectifier is used. Zero voltage switching for all the switches can be achieved.

In the foregoing circuit configuration, symmetrical rectifier is assumed. When the inverter is capable of providing asymmetrical output, asymmetrical rectifier can also be used. Fig. 16(f) gives the topology of asymmetrical Class-E-SRLS converter where only one switch is used in the SRLS current rectifier. By changing the conduction time of T_2, the output voltage can be regulated. Again, zero voltage switching for all the swithces can be maintained from no load to full load.

VI. Experimental Results

Two experimental prototypes, one is the Parallel-SRLS resonant converter and the other is the Series-SRLS resonant converter, are breadboarded. The objective is to illustrate the feasibility of the proposed technique and to verify the analysis. The MOSFET is used as the switch in the experiment.

The testing circuit for Parallel-SRLS resonant converter is shown in Fig. 7. The circuit parameters are $L_r = 13.5\,\mu\text{H}, L_S = 7.2\,\mu\text{H}, C_r = 0.34\,\mu\text{F}, V_S = 15$ V. The resonant frequency f_r is calculated as 74.3 KHz. The switching frequency is chosen as 100 KHz. The internal anti-parallel diode of MOSFET is used for D_1 and D_2. Fig. 17(a) gives the waveforms of the gate voltage V_{GS1} and the device voltage V_{DS1} for MOSFET T_1. Zero voltage switching is observed clearly. Fig. 17(b) gives the waveforms of the capacitor voltage v_C and the input current of the SRLS voltage rectifier, i_S. Because of the high frequency oscillation, which is caused partly by the parasitic capacitance and partly by the probe, the waveform of i_S is distorted. However, the quasi-square shape can still be identified. Fig. 17(c) shows the current through T_3 and the voltage across T_3. Zero current turn off is clearly observed. Because of L_S, i_{T3} rises slowly at turn on. Fig. 17(d) shows the output voltage V_o and the rectified voltage v_d.

Fig. 18 gives the measured voltage gain versus the turn on delay angle α of the Parallel-SRLS converter, where the output current is kept at 1A. Also given in Fig. 18 is the calculated value. The small difference is because of the various losses in the circuit, such as the Q loss of the inductor, rectifier voltage

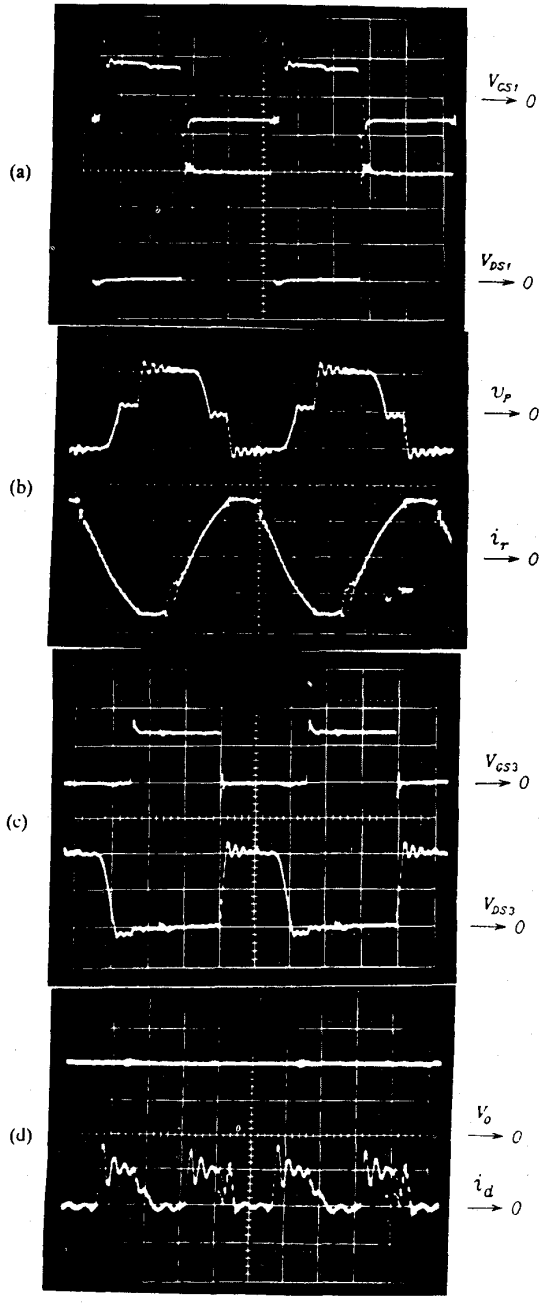


Fig. 19. Measured waveforms for Series-SRLS converter. (a) Upper trace: V_{GS1} 10V/div, lower trace: V_{DS1} 10V/div. (b) Upper trace: V_P 10V/div, lower trace: i_r 1A/div. (c) Upper trace: V_{GS3} 5V/div, lower trace: V_{DS3} 1A/div. (d) Upper trace: V_o 10V/div, lower trace: i_d 2.5A/div.

drop, etc.. It is demonstrated that by changing the α, the output voltage can be effectively controlled.

A Series-SRLS resonant converter is also breadboarded. The testing circuit is shown in Fig. 10. The circuit parameters are: $L_r = 12\,\mu\text{H}, C_r = 0.099\,\mu\text{F}, C_P = 0.033\,\mu\text{F}$. The resonant frequency, f_r, is calculated as 146 KHz. The switching frequency is chosen as 200 KHz. D_1, D_2, D_3 and D_4 consist of the MOSFET's antiparallel diode. Fig. 19(a) gives the measured waveforms of V_{GS1} and V_{DS1} for MOSFET T_1. Zero voltage turn on is clearly observed. Fig. 19(b) shows the waveforms of the inductor current i_r and the input voltage of the SRLS current rectifier, v_P. Quasi-square waveform of v_P is clearly shown. Fig. 19(c) gives the waveform of V_{GS3} and V_{DS3} for T_3. Zero voltage switching for the rectifier switch is observed clearly. Fig. 19(d) shows the output voltage V_o and the rectified current i_d.

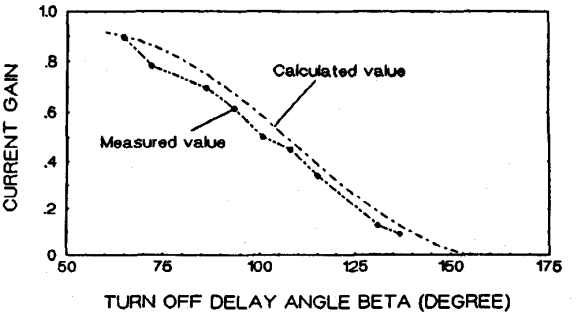


Fig. 20. Measured current gain versus β at V_o =10 (V).

Fig. 20 gives the measured current gain versus the turn off delay angle β, where the output voltage V_o is kept at 10 V. The theoretical value is also plotted in Fig. 20. The current base I_{base} is calculated as 1.35 A. The small difference is caused by nonideality of the prototype. It demonstrates that by changing the turn off delay angle β, the output voltage can be kept constant when load current changes.

VII. Conclusion

The basic concept of the Source Reactance Lossless Switch (SRLS) has been presented. The mechanism of the zero current switching and zero voltage switching using energy removal by source voltage or current is analyzed.

In the SRLS voltage rectifier, the switches operate at zero current switching condition, while in the SRLS current rectifier, the switches operate at zero voltage switching condition.

When SRLS voltage rectifier or SRLS current rectifier is used in the conventional resonant converters, new resonant converter topologies are obtained. The operations of the two basic SRLS converters, i.e., Parallel-SRLS resonant converter and Series-SRLS resonant converter are studied in detail. Their output voltage can be regulated by changing the turn on or turn off delay angle of the rectifier switch while keeping the switching frequency constant. Zero current switching and/or zero voltage switching characteristic for all the switches in these two converters can be maintained from no load to full load.

The steady-state characteristics of the Parallel-SRLS and Series-SRLS resonant converters are analyzed. Control to output characteristics are given. The effect of the series inductance (in Parallel-SRLS resonant converter) and the effect of the parallel capacitor (in Series-SRLS resonant converter) are also studied. Their influence on the control to output characteristics are also outlined.

Several other converter topologies using SRLS technique are also proposed. Their output voltage can be controlled at

fixed switching frequency and zero current switching and/or zero voltage switching can be achieved for all the switches in the converter.

Two experimental prototypes, Parallel-SRLS resonant converter and Series-SRLS resonant converter, are breadboarded. The objective is to demonstrate the feasibility of the proposed topologies. The experimental results obtained verify the analysis.

The work presented in this paper has revealed many good features of SRLS technique for application in resonant converters with fixed switching frequency. Further work on various aspects of these converters, in particular, a comparative evaluation of the various proposed topologies, will be the subject matter of future investigation.

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