An Improved Zero Voltage Switching Flyback Converter Topology

Youhao Xi Praveen K. Jain Geza Joos
Concordia University
Dept. of Electrical and Computer Engineering
1455 de Maisonneuve Blvd. West
Montreal, Quebec, Canada H3G 1M8

Yan Fei Liu
Nortel Power Group
P.O.Box 3511, Station C
Ottawa, Ontario
Canada K1Y 4H7

Abstract—An improved zero voltage switching flyback converter topology is presented in this paper. This converter employs an auxiliary circuit that provides ZVS for both the main and auxiliary switches, and it permits the operation of the converter at very high frequencies. Operating principle, steady state analysis, and design procedure for the auxiliary circuit of the proposed converter, are given. A 50 W, 200 kHz prototype converter is built to verify the performance. Experiments of the proposed converter show an improvement of about 2% in the overall efficiency as compared to the previous ZVS flyback converter.

I. Introduction

In advanced telecommunication and computer systems, power supplies are required to have high power density and high efficiency. To achieve high power density, the power supplies are operated at higher switching frequencies. However, when the switching frequency increases, the losses associated with the turn-on and turn-off of the power switching devices in the hard switching MOSFET converters also increase, limiting the operation of the converters above 50 kHz.

The active clamp flyback and forward converter topologies have been reported in the literature [1-5]. ZVS can be achieved in these topologies. However, they have the following shortcomings.

(i) An isolated, variable duty cycle gate drive for the clamp switch is required,
(ii) A modified PWM control technique to properly program the associated delays between the gate drives of the main and clamp switches are necessary to achieve ZVS,
(iii) ZVS is lost under light load conditions,
(iv) The current mode control can not be used, and
(v) The patent related legal issues make it difficult to use.

A ZVS flyback converter topology has been recently proposed in [6]. It employed an auxiliary circuit and it can overcome the aforementioned shortcomings. However, in this circuit, the energy associated with the leakage inductance of the auxiliary transformer was not recovered, and the auxiliary switch had hard switching. These problems limit the operation of the converter at very high frequencies.

In this paper, a modified auxiliary circuit is employed in the proposed ZVS flyback converter so that both the main and auxiliary switches can achieve zero voltage switching. Detailed analysis of the circuit is presented in this paper. A design procedure is provided. A 50 W, 200 kHz prototype circuit is built to verify the analysis and design. The experimental results show about 2% increase in the overall efficiency as compared to the previous converter.

II. An Improved ZVS Flyback Converter Topology

Fig. 1 shows an improved ZVS flyback converter topology employing an auxiliary circuit that is drawn in the dashed line block.

In Fig. 1, T_r is the power transformer with a turn's ratio of n and a magnetizing inductance of L_m, $Q1$ is the main switch, D_o is the output rectifier, C_o is the output capacitor, R_L is the load, and C_{in} is the input capacitor. All these comprise a standard flyback converter.

The auxiliary circuit consists of an auxiliary switch $Q2$, a snubber capacitor C_{snb}, a resonant inductor L_a, a resonant capacitor C_a, an auxiliary transformer T_a with three windings $N1$, $N2$ and $N3$, and two auxiliary rectifier diodes $D1$ and $D2$.

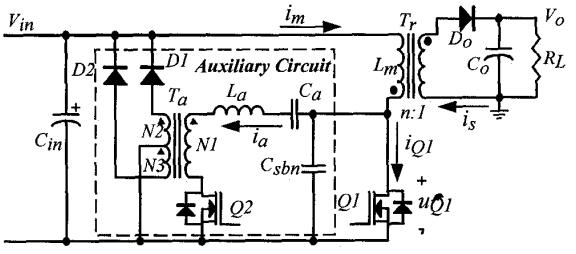


Fig. 1. The proposed ZVS flyback converter topology.

III. Operating Principle and Steady State Analysis

Fig. 2 shows key waveforms of the proposed circuit of Fig. 1. For each switching cycle, T_s, the converter operates in seven intervals. The converter is assumed to be in discontinuous conduction mode.

The steady state analysis is performed under the following assumptions:

0-7803-4489-8/98/$10.00 © 1998 IEEE

(i) $N1/N2 << 1$, $N1/N3 << 1$,
(ii) $L_m >> L_a$,
(iii) ON resistances of the switches are zero Ohms,
(iv) all capacitors are lossless, and
(v) all diodes are ideal devices.
Under these assumptions, a detailed description of the converter in various intervals is given below.

A. Interval 1

Fig. 3(a) shows the circuit operation during this interval. At the beginning of this interval, the auxiliary switch *Q2* is turned on. A resonant tank consisting of L_a, C_a and C_{snb} is formed. *Q2* has a ZCS turn-on because it is in series with L_a. A resonant current i_a flows through C_a, L_a, N_2 and *Q2*. The drain voltage of *Q1* decreases and is governed by

$$u_{Q1}(t) = \frac{C_a V_0}{C_a + C_{snb}} \cos[\omega_n (t - t_1)] + \frac{C_{snb} V_0}{C_a + C_{snb}} \quad (1)$$

where V_0 is the steady state drain voltage of *Q1* at the beginning of this interval, and

$$\omega_n = 1/\sqrt{L_a C_{snb} C_a / (C_{snb} + C_a)} \quad (2)$$

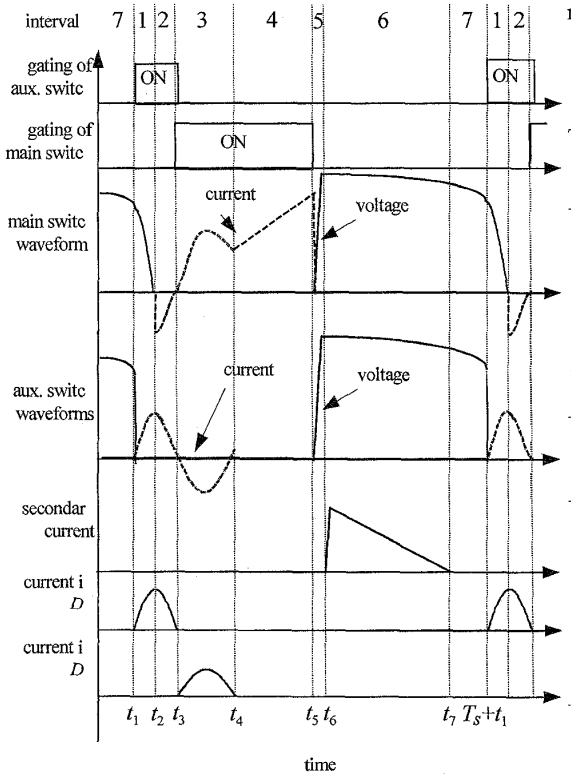


Fig. 2. Key waveforms of the proposed ZVS flyback converter topology

The resonant current is given by

$$i_a(t) = \frac{\omega_n C_a C_{snb}}{C_{snb} + C_a} V_0 \sin[\omega_n (t - t_1)] \quad (3)$$

This current discharges C_{snb} and charges the resonant tank. Owing to transformer coupling by T_a, a current proportional to i_a flows through *N2* and *D2*. In this way the energy stored in C_{snb} is fed back into the input dc line.

At the end of this interval, u_{Q1} reaches zero voltage. The duration of this interval is determined by

$$t_2 - t_1 = \sqrt{L_a \frac{C_{snb} C_a}{C_{snb} + C_a}} \cos^{-1}\left(-\frac{C_{snb}}{C_a}\right) \quad (4)$$

(4) implies that C_a should be larger than C_{snb}. Thus, zero drain voltage of u_{Q1} can always be achieved regardless the line/load conditions.

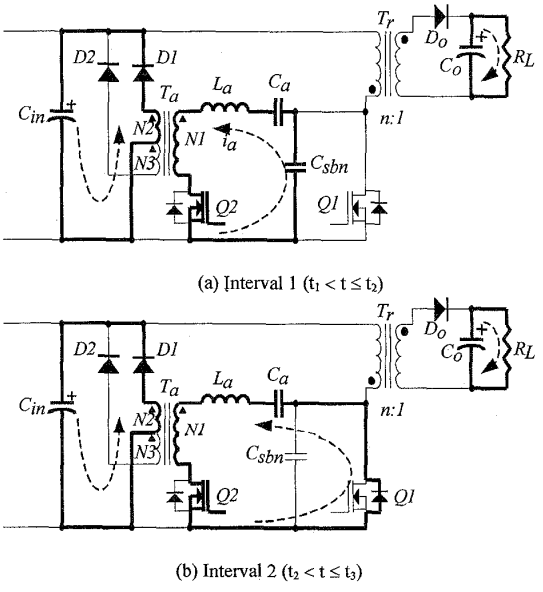
During this interval, C_o provides the load current.

B. Interval 2

Fig. 3(b) shows the circuit operation during this interval. At the beginning of this interval, i_a starts to flow through the body diode of *Q1*, and u_{Q1} is clamped at zero. Now, the resonant tank excludes C_{snb} and the new resonant frequency is determined by

$$\omega_a = 1/\sqrt{L_a C_a} \quad (5)$$

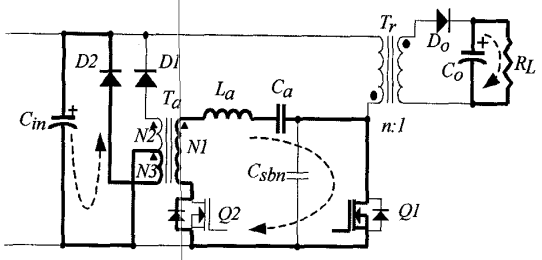
The resonant current is found to be



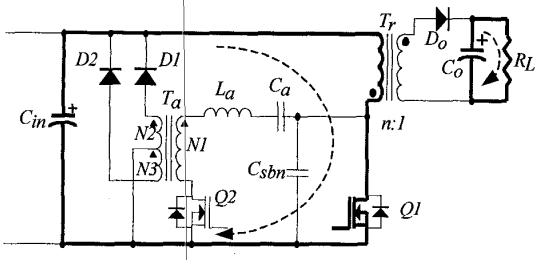
(a) Interval 1 ($t_1 < t \le t_2$)

(b) Interval 2 ($t_2 < t \le t_3$)

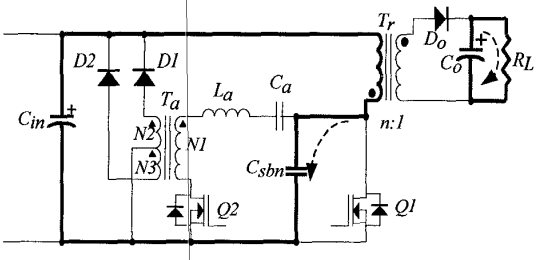
Fig. 3. Modes of operation of the converter of Fig. 1 (*to be continued below*). The dashed line arrows indicate the current directions.



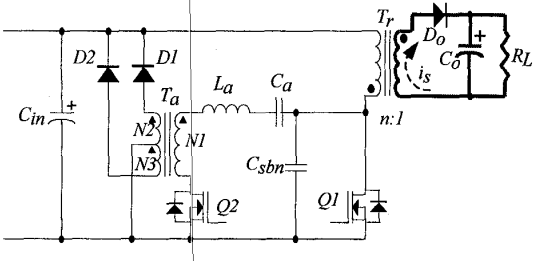
(c) Interval 3 ($t_3 < t \le t_4$)



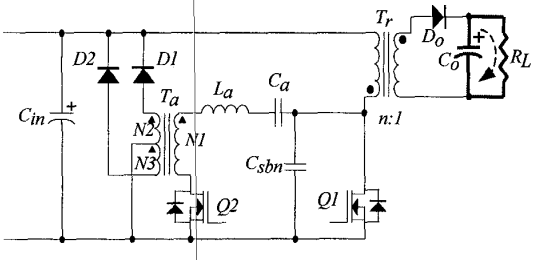
(d) Interval 4 ($t_4 < t \le t_5$)



(e) Interval 5 ($t_5 < t \le t_6$)



(f) Interval 6 ($t_6 < t \le t_7$)



(g) Interval 7 ($t_7 < t \le t_1 + T_s$)

Fig. 3. Modes of operation of the converter of Fig. 1 (*continued*). The dashed line arrows indicate the current directions.

$$i_a(t) = A\cos[\omega_a(t-t_2)] - B\sin[\omega_a(t-t_2)] \quad (6)$$

where,

$$A = V_0\sqrt{\frac{(C_a - C_{snb})C_{snb}}{L_a C_a}} \quad (7.a)$$

$$B = \frac{C_{snb}}{\sqrt{L_a C_a}}V_0 \quad (7.b)$$

A current proportional to i_a flows into the input dc line though *N2* and *D1*.

During this interval, C_o provides the load current. At the end of this interval, i_a crosses zero and starts to reverse its direction. The duration of this interval is determined by

$$t_3 - t_2 = \sqrt{L_a C_a}\tan^{-1}\left(\sqrt{\frac{C_a - C_{snb}}{C_a}}\right) \quad (8)$$

C. Interval 3

Fig. 3(c) shows the circuit operation during this interval. At the beginning of this interval, *Q1* is turned on under zero voltage condition, hence it achieves a lossless turn-on. i_a deviates to the main channel of *Q1* from its body diode, and this current is still governed by (6). A current proportional to i_a flows into the input dc line though *N3* and *D2*.

Since i_a flows in the reversed direction, *Q2* does not suffer from any voltage stress when it is turned off in this interval. Hence, *Q2* can achieve a lossless turn-off.

As *Q1* is ON, L_m sees a constant voltage V_{in}, and the current in L_m starts to rise linearly and is governed by

$$i_m(t) = \frac{V_{in}}{L_m}(t - t_3) \quad (9)$$

the drain current of *Q1* is

$$i_{Q1}(t) = i_m(t) - i_a(t) \quad (10)$$

During this interval, C_o provides the load current. At the end of this interval, i_a reaches its second zero. Since *Q2* is OFF, the resonant process is interrupted.

D. Interval 4

Fig. 3(d) shows the circuit operation during this interval. At the beginning of this interval, the resonant process interrupted and the operation of the circuit is just like a standard flyback converter. The primary current of the power transformer, i_m, continues to rise until the duty cycle of the main switch completes. The drain current of *Q1* consists of only i_m as given by (9).

During this interval, C_o provides the load current.

E. Interval 5

Fig. 3(e) shows the circuit operation during this interval. At the beginning of this interval, *Q1* is turned off. Because of C_{snb}, the speed of rise of u_{Q1} is slowed down. Thus *Q1* can achieve a ZVS turn-off.

The rising u_{Q1} is governed by [7]

$$u_{Q1}(t)=V_{in}\left\{1+\frac{\omega_0 D}{f_s}\sin[\omega_0(t-t_5)]-\cos[\omega_0(t-t_5)]\right\} \tag{11}$$

where,

$$\omega_0 = 1/\sqrt{L_m C_{snb}} \tag{12}$$

The secondary winding of T_r sees a voltage proportional to (u_{Q1}-V_{in}). Before the secondary voltage reaches V_o, D_o is still reversed biased. Then C_o provides the load current during this interval.

At the end of this interval, u_{Q1} reaches V_o. The duration of this interval is determined by solving (11).

F. Interval 6

Fig. 3(f) shows the circuit operation during this interval. At the beginning of this interval, the secondary voltage reaches V_o. D_o becomes forward biased and starts to conduct. Thus, like in a standard flyback circuit, the energy store in the core of T_r is transferred to the output. The secondary current also charges C_o.

As the secondary winding sees a constant voltage V_o, the drain voltage of *Q1* is clamped at

$$u_{Q1}(t) = V_{in} + nV_o \tag{13}$$

The secondary current decreases linearly, as governed by

$$i_s(t) = I_{sp} - \frac{n^2 V_o}{L_m}(t-t_6) \tag{14}$$

where I_{sp} is the peak of the secondary current given by

$$I_{sp} = n\sqrt{\left(\frac{V_{in}D}{f_s L_m}\right)^2 - \frac{C_{snb}}{L_m}(V_{in}+nV_o)^2} \approx \frac{nV_{in}D}{f_s L_m} \tag{15}$$

At the end of this interval, i_s reaches zero. The duration of this interval is determined by solving (16).

G. Interval 7

Fig. 3(g) shows the circuit operation during this interval. At the beginning of this interval, the stored energy in T_r is completely transferred to the load. Then D_o becomes reverse biased again. Thus, the circuit maintains in the discontinuous conduction mode operation.

C_o supplies all of the output current. The drain voltage of *Q1* is no longer clamped, and a resonance starts in the network consisting of L_m, C_{snb} and the input dc line. This resonance results in the tail of u_{Q1}, as governed by

$$u_{Q1}(t) = V_{in} + nV_o\cos[\omega_0(t-t_7)] \tag{16}$$

At the end of this interval, $t = T_s+t_1$, u_{Q1} reaches a voltage V_0, which is the steady state initial voltage per switching cycle, as given by

$$V_0 = V_{in} + nV_o\cos[\omega_0(T_s+t_1-t_7)] \tag{17}$$

The current associated with this process is given by

$$i_m(t) = -nV_o\sqrt{\frac{C_{snb}}{L_m}}\sin[\omega_0(t-t_7)] \tag{18}$$

Since L_m is much larger than L_a, by comparing (18) to (3), i_m is negligible and hence ignored in the analysis of Interval 1.

At the end of Interval 7, a new switching cycle starts and the process repeats from Intervals 1 through 7.

IV. Design Procedure of the Auxiliary Circuit

The selection criteria for the main power circuit are not given here, as it is a conventional circuit that has been extensively published in the literature. The design procedure to select the various components of the auxiliary circuit of Fig. 1 is given below.

It is assumed that the following parameters are known:

(i) D_{max} and D_{min}, the nominal maximum and minimum duty cycle of *Q1*, respectively,
(ii) f_s, the switching frequency
(iii) L_m, the magnetizing inductance of T_r,
(iv) n, the turn's ratio of T_r,
(v) V_o, the nominal output voltage, and
(vi) the nominal input voltage range.

A. Auxiliary Switch Duty Cycle, D_{aux}

D_{aux} is limited by

$$(1-2D_{min}) \geq D_{aux} \geq (1-2D_{max}) \tag{19}$$

This ensures the auxiliary circuit not to affect the normal operation of the power circuit. The value given in a control chip such as the UC3855, where D_{aux} is set between 0.07 to 0.10, can be used.

B. Snubber Capacitor, C_{snb}

C_{snb} controls the rise time of u_{Q1} in the turn-off

transient of $Q1$. The rise time should be limited so as not to affect the resetting of the core of T_r. Thus C_{snb} is limited by

$$C_{snb} \le \frac{(1-2D_{\max}-D_{aux})D_{\max}V_{in\_\min}}{f_s^2 L_m (V_{in\_\min}+nV_o)} \quad (20)$$

where, $V_{in\_\min}$ is the minimum input voltage.

C. Resonant Tank, L_a and C_a

Interval 3 should be limited by the minimum duty cycle of the main switch. Hence, the following equation should be satisfied:

$$L_a \le \frac{D_{\min}^2}{\pi^2 f_s^2 C_a} \quad (21)$$

On the other hand, (6) and (7) indicate that, in order to reduce the conduction losses in $Q2$, L_a should be large. Hence, the allowable maximum value governed by (21) should be selected for L_a.

Since the total duration of Intervals 1 and 2 is equal to the auxiliary duty cycle, the following equation should be satisfied:

$$t_3 - t_1 = D_{aux} / f_s \quad (22)$$

Substituting (4) and (8) into (22) and solving it for C_a, one may obtain the value of the resonant capacitor. Fig. 4 shows the design curves for C_a.

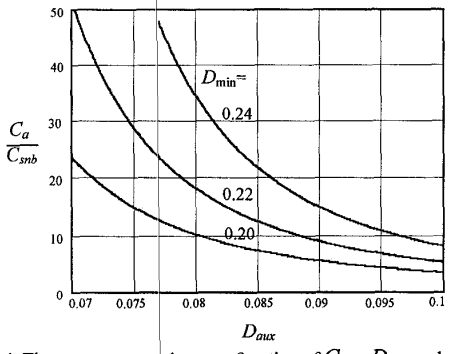


Fig. 4. The resonant capacitor as a function of C_{snb}, D_{aux} and $D_{\min}$.

D. Auxiliary Transformer, T_a

The auxiliary transformer should have a high turn's ratio so as to minimize the reflected input voltage seen in the primary side. On the other hand, the core size should be as small as possible.

E. Auxiliary Diodes, D1 and D2

These diodes are fast recovery diodes. Their voltage rating is equal to twice the maximum input voltage and the current rating is determined by the peak of i_a and the turns ratio of T_a.

F. A Design Example

A design example is given below. Table I shows the principal specifications and parameters of the main power circuit of the prototype flyback converter.

Table II shows the parameters of the auxiliary circuit in the prototype converter, which are selected according to the selection criteria presented above.

TABLE I
PRINCIPAL SPECIFICATIONS AND PARAMETERS OF THE MAIN POWER CIRCUIT OF THE PROTOTYPE FLYBACK CONVERTER

specification		parameter	
$V_{in\_\min}$	90V	L_m	50μH
$V_{in\_\max}$	160V	n	18
P_o	50W (V_o=5V)	C_o	2000μF
$D_{\max}/D_{\min}$	0.45/0.20	$Q1$	IRFP450
f_s	220kHz	Controller	UC3855AN

TABLE II
COMPONENTS OF THE AUXILIARY CIRCUIT IN THE PROTOTYPE FLYBACK CONVERTER

parameter		parameter	
D_{aux}	0.08	$N1/N2/N3$	3/36/36
C_{snb}	2.2nF	$Q2$	IRF740
L_a &C_{snb}	4.0μH & 22nF	$D1$, $D2$	HFA08TB

V. EXPERIMENTAL RESULTS

A prototype ZVS flyback converter has been built based on the design example. The principal specifications and parameters of the converter are shown in Tables I and II. The input dc voltage range is 90 to 160 V.

Fig. 5 shows the waveforms of the auxiliary switch $Q2$. It is clearly that the turnoff losses existing in the previous ZVS flyback converter [7] has been removed in this circuit.

Fig. 6 shows the waveforms of the main switch $Q1$. It is seen that lossless switching is achieved at both turn-on and turnoff transients.

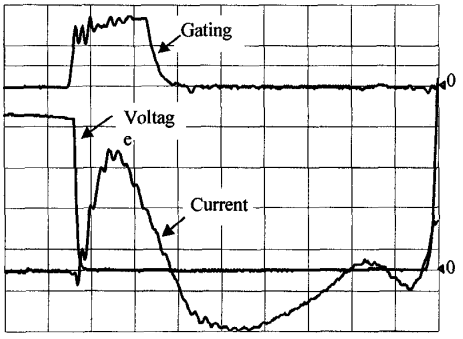


Fig. 5. The waveforms of drain voltage and current of the auxiliary swtich. Operating conditions: P_o =50 W, V_{in} = 125 V, f_s = 220 kHz. Scales: vertical-50 V/div. for the drain voltage, 10 V/div. for the gating signal, and 1A/div. for the drain

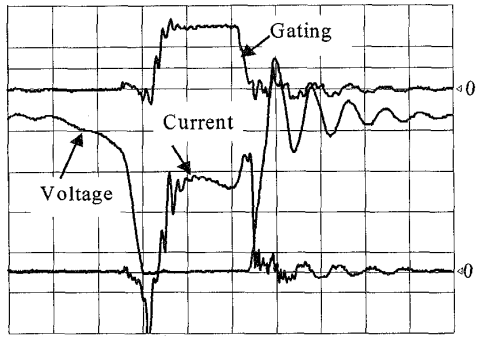


Fig. 6. The waveforms of drain voltage and current of the main swtich. Operating conditions are the same as those in Fig. 5. Scales: vertical-the same as Fig. 5; horizontal: 0.5 μs/div.

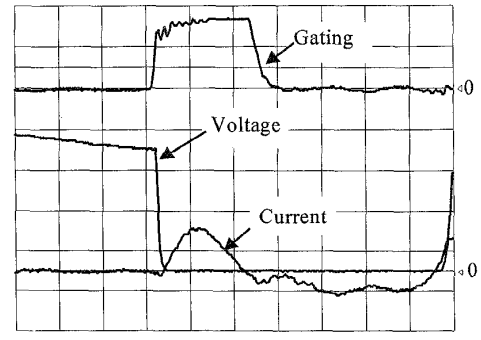


Fig. 9. The waveforms of drain voltage and current of the auxiliary swtich. Operating conditions: P_o =25 W, V_{in} = 125 V, f_s = 220 kHz. Scales: the same as Fig. 5.

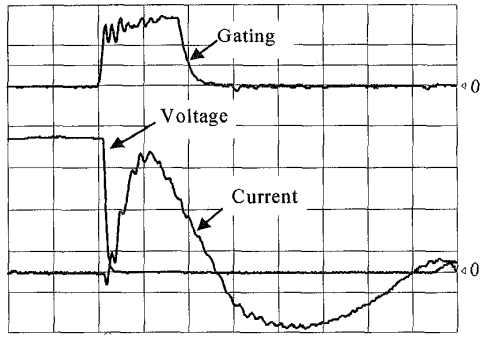


Fig. 7. The waveforms of drain voltage and current of the auxiliary swtich. Operating conditions: P_o =50 W, V_{in} = 90 V, f_s = 220 kHz.. Scales: the same as Fig. 5.

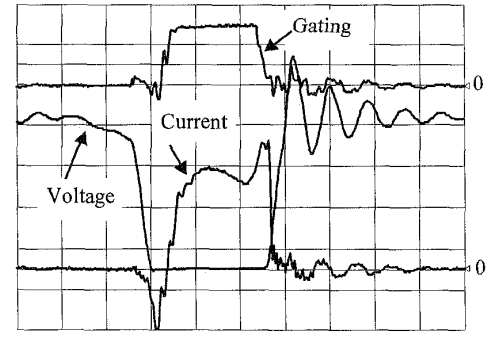


Fig. 10. The waveforms of drain voltage and current of the main swtich. Operating conditions: P_o =50 W, V_{in} = 90 V, f_s = 220 kHz. Scales: the same as Fig. 6.

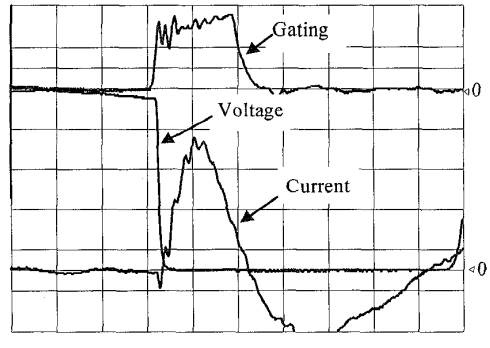


Fig. 8. The waveforms of drain voltage and current of the auxiliary swtich. Operating conditions: P_o =50 W, V_{in} = 150 V, f_s = 220 kHz.. Scales: the same as Fig. 5.

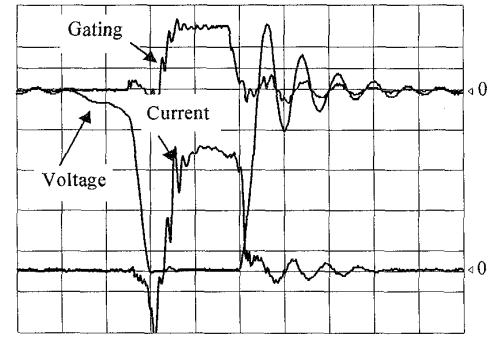


Fig. 11. The waveforms of drain voltage and current of the main swtich. Operating conditions: P_o =50 W, V_{in} = 160 V, f_s = 220 kHz. Scales: Scales: the same as Fig. 6.

Figs. 7 to 11 shows the main and auxiliary switches' waveforms under different operating conditions. It is seen that ZVS is always achieved.

Fig. 12 shows the overall efficiency as a function of input voltage under full load conditions. Comparing with the previous ZVS flyback circuit, about 2% better efficiency is obtained with the proposed circuit.

Fig. 13 shows the overall efficiency as a function of load. It is seen that the proposed circuit always has higher efficiency than the previous flyback circuit.

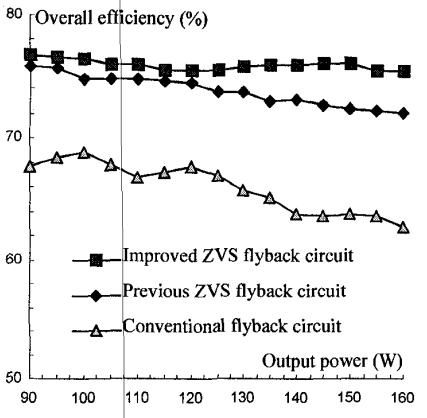


Fig. 12. The overall efficiency as a function of input voltage under full load conditions. Operating conditions: P_o =50 W, f_s = 220 kHz.

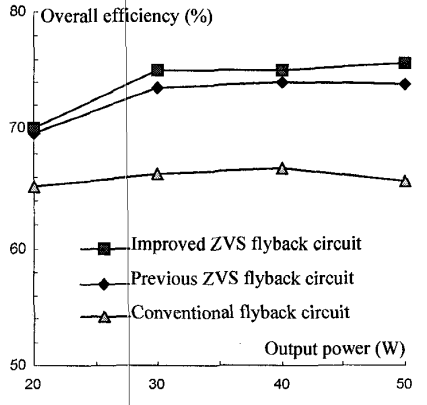


Fig. 13. The overall efficiency as a function of output load. Operating conditions: V_{in} =125 V, f_s = 220 kHz.

VI. CONCLUSIONS

In this paper, an improved ZVS flyback converter topology that employs an auxiliary circuit has been presented. The proposed circuit achieves zero voltage switching of both the main and auxiliary switches. The proposed circuit has about 2% higher efficiency than the previously published ZVS flyback converter topology. This permits the operation of the converter at much higher switching frequencies.

ACKNOWLEDGMENT

The work reported in this paper was performed through a Nortel NSERC Collaborative R&D Program. The authors would like to thank Mr. G. Spak at Nortel (Ottawa) for optimizing the auxiliary magnetics and Mr. H. Pinheiro at Concordia University Power Electronics Laboratory for valuable discussions.

REFERENCES

[1] Carsten, B., "Design techniques for transformer active reset circuits at high frequencies and power levels," *High Frequency Power Conversion Proceedings*, 1990, pp. 235-246.

[2] Harada, K., Sakamoto, H., "Switched snubber for high frequency switching," *IEEE PESC '90 Record*, Vol.1, pp. 181-188.

[3] Jitaru, I., "Zero voltage PWM, double ended converter," *High Frequency Power Conversion Proceedings*, 1992, pp. 394-404.

[4] Tsai, F., Ng, W., " A low cost, low-loss active voltage-clamp circuit for interleaved single-ended Forward PWM converter," *IEEE APEC '93 Record*, pp. 729-733.

[5] Watson, R., Lee, F. C., Hua, G. C., "Utilization of an active-clamp circuit to achieve soft switching in flyback converters", *IEEE PESC ' 94 Record*, pp. 909-916.

[6] Xi, Y., Jain, P. K., Joos, G., "A zero voltage switching flyback converter topology", *IEEE PESC '97 Record*, pp. 951-957.