A Zero Voltage Switching and Self-Reset Forward Converter Topology [1]

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Abstract–**A zero voltage switching (ZVS) forward converter topology is presented in this paper. In this topology, an auxiliary circuit is employed. ZVS is achieved on both the main and auxiliary switches. The power transformer in the proposed topology is self-reset without the use of conventional tertiary reset winding. Analysis and design of the circuit are presented. Experiments on a 5 V, 100 W prototype converter switched at a frequency of 200 kHz verify the design and show an overall efficiency of about 90 %.**

I. INTRODUCTION

The forward converter topology is one of the most popular topologies used for the distributed power supplies in advanced telecommunication and computer systems. These systems require the supplies to have high power density and efficiency. To achieve high power density, the power supply is switched at an increasingly higher frequency. This leads to employing decreasingly smaller sized magnetics and capacitors.

However, the conventional forward converter is operated in the hard switching mode. In such a converter, as the switching frequency increases, the switching losses associated with the turn-on and -off of the power devices increase. Thus, the efficiency decreases, and the cooling requirement increases. This problem has become a major obstacle to the application of the conventional hard switching converters in the advanced systems.

To solve the problem, soft switching techniques are now commonly used to eliminate, or greatly reduce, the switching losses. Several zero voltage switching (ZVS) forward converter topologies have been reported in the literature [1-7], among which are typically the active clamp/reset forward converter topologies. These ZVS topologies have certain merits, but they suffer from at least one of the following drawbacks:

(i) ZVS is achieved at the cost of increased conduction losses.
(ii) ZVS is lost under light load or no load conditions.
(iii) The design of the gate drive and control circuit becomes complicated.
(iv) Some patent legal issues limit their applications.

1. U.S. and other international patents are pending.

In order to overcome these drawbacks, a ZVS forward converter topology has been proposed recently [8]. It employs an auxiliary circuit to achieve ZVS of the main switch. However, in this circuit, the energy associated with the leakage inductance of the auxiliary transformer was not recovered, and the auxiliary switch had hard switching at turnoff. These problems limit the operation of the converter at very high frequencies.

In this paper, a modified auxiliary circuit is employed, and hence both the main and auxiliary switches can achieve ZVS. In addition to this improvement, the power transformer self resets without the use of conventional tertiary reset winding. This leads to a simplified transformer structure. Steady state analysis of the circuit is presented in this paper. A design procedure is provided. A 5 V, 100 W, 200 kHz prototype circuit is built to verify the analysis and design. The experimental results show an overall efficiency of about 90% at full load over entire range of the input voltage.

II. CIRCUIT DESCRIPTION

Fig. 1 shows the proposed ZVS forward converter topology. It has two functional sub-circuits. One is the auxiliary circuit that is drawn inside the dashed line block. The other, outside the block, is the conventional forward converter, which is referred to as the "power circuit" hereafter.

The power circuit is comprised of (i) T_r, the power transformer with a magnetizing inductance L_m and a turns ratio of k, (ii) Q_1, the main switch, (iii) D_{o1} and D_{o2}, the output rectifiers, (iv) L_o and C_o, the output filter, (v) R_L, the load, and (vi) C_{in}, the input filter capacitor.

The auxiliary circuit consists of (i) Q_2, the auxiliary switch,

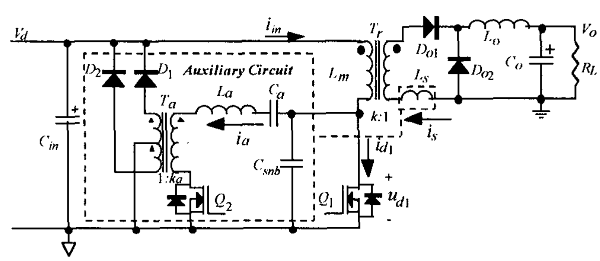


Fig.1 The proposed ZVS forward converter topology.

(ii) C_{snb}, a snubber capacitor for the main switch, (iii) L_s, a current limit inductor, which is inserted into the secondary side of T_r, (iv) L_a and C_a, a resonant bank, (v) T_a, a center-tapped auxiliary transformer with a turns ratio of k_a, and (vi) D_1 and D_2, two auxiliary rectifiers.

The auxiliary circuit has a threefold function: (i) it provides ZVS of the main switch Q_1 both at turn-on and turn-off, thereby eliminating the switching losses of Q_1, (ii) it provides zero current switching (ZCS) of the auxiliary switch Q_2 at turn-on and ZVS at turn-off, thereby eliminating the switching losses of Q_2, and (iii) it resets the core of the transformer T_r.

III. Operating Principle

Fig.2 shows key waveforms that highlight the operating principle of the proposed converter topology in Fig. 1. The steady state operation of the circuit can be divided into six intervals in each switching cycle. Before each interval is described, the following assumptions are made:

(i) the circuit has already reached the steady state operation and it outputs the rated power P_o at the nominal output voltage V_o and constant input voltage V_d,

(ii) k_a<<1, and L_m>>L_a,

(iii) the values of L_o and C_o are fairly large and can be considered infinite,

(iv) ON resistance of each switch is zero,

(v) the capacitors, inductors and transformers are lossless, and

(vi) all diodes are ideal devices.

A. *Interval* 1

At the beginning of this interval, t = 0 and Q_2 is turned on. A zero current switching (ZCS) is achieved in Q_2 as it is in series with L_a. A resonant network is formed with C_{snb}, C_a, L_a, T_r and L_s.

Fig. 3.a shows the equivalent circuit of this network. A resonant current builds up in the auxiliary circuit. By this current, C_{snb} is discharged through C_a, L_a, T_a and Q_2. This discharging current feeds energy back into the input dc line via T_a and D_1.

The drain to source voltage u_{d1} of Q_1 satisfies the following equation

$$\alpha\frac{d^4u_{d1}(t)}{dt^4}+\beta\frac{d^2u_{d1}(t)}{dt^2}+u_{d1}(t)=V_d \tag{1}$$

where

$$\alpha=L_aC_aL_eC_{snb} \tag{2}$$

$$\beta=L_e(C_{snb}+C_a)+L_aC_a \tag{3}$$

and L_e is the equivalent value of the paralleled L_m and L_s seeing from the primary side of T_r, and it is defined as

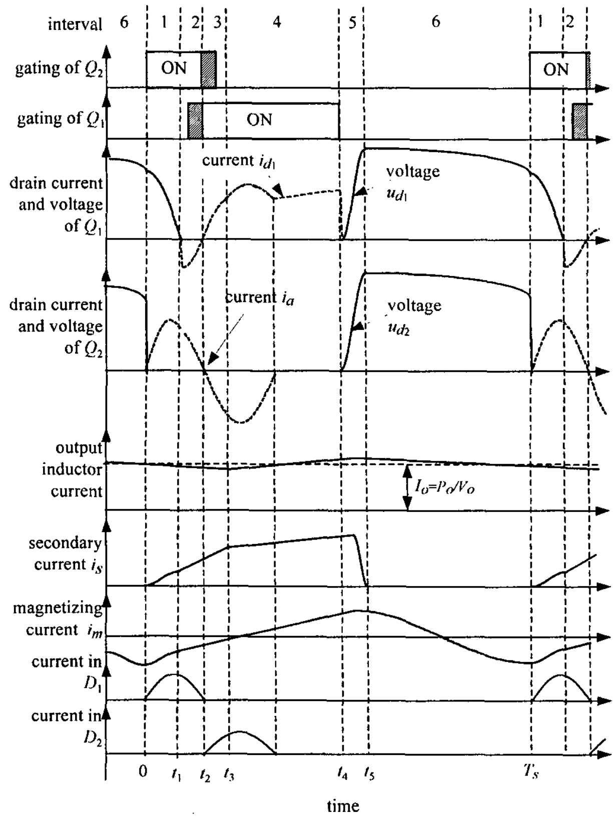


Fig. 2 Key waveforms (not to scale in magnitude).

$$L_e=\frac{k^2L_sL_m}{k^2L_s+L_m}\approx k^2L_s \tag{4}$$

The solution of (1) is found to be

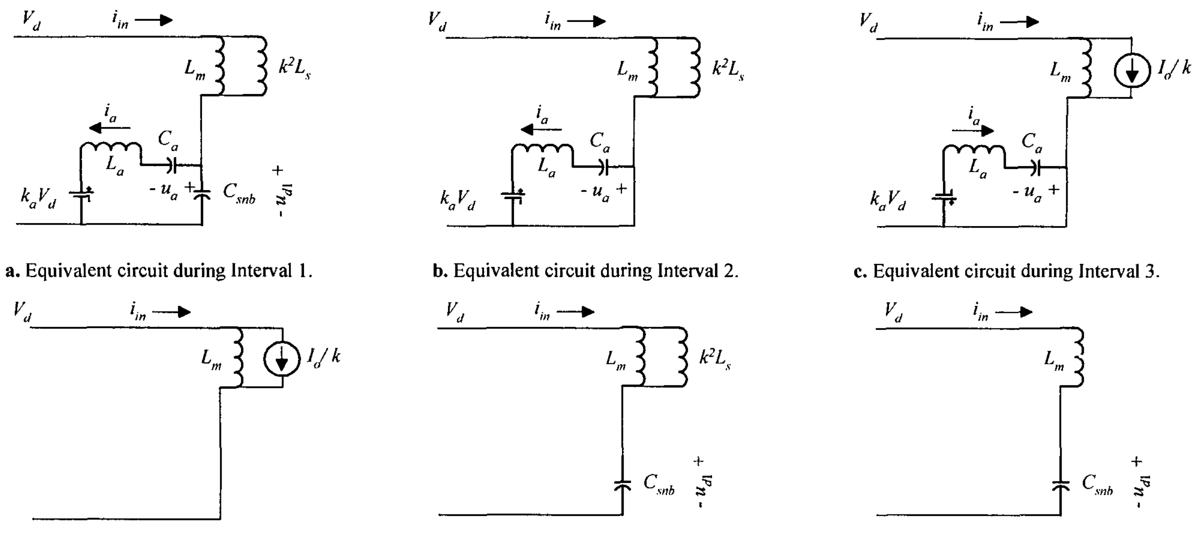
$$u_{d1}(t)=V_d+a_1\cos\omega_1t+a_2\sin\omega_1t+a_3\cos\omega_2t+a_4\sin\omega_2t \tag{5}$$

where

$$\omega_1=\frac{1}{2}\sqrt{\frac{2\beta+2\sqrt{\beta^2-4\alpha}}{\alpha}}\approx\sqrt{\frac{\beta}{\alpha}} \tag{6}$$

$$\omega_2=\frac{1}{2}\sqrt{\frac{2\beta-2\sqrt{\beta^2-4\alpha}}{\alpha}}\approx\frac{1}{\sqrt[4]{\alpha}} \tag{7}$$

$$\begin{bmatrix}a_1\\a_2\\a_3\\a_4\end{bmatrix}=\begin{bmatrix}1&0&1&0\\0&\omega_1&0&\omega_2\\-\omega_1^2&0&-\omega_2^2&0\\0&-\omega_1^3&0&-\omega_2^3\end{bmatrix}^{-1}\begin{bmatrix}u_{d1}(0)-V_d\\\dot{u}_{d1}(0)\\\ddot{u}_{d1}(0)\\\dddot{u}_{d1}(0)\end{bmatrix} \tag{8}$$



a. Equivalent circuit during Interval 1. **b.** Equivalent circuit during Interval 2. **c.** Equivalent circuit during Interval 3.

d. Equivalent circuit during Interval 4. **e.** Equivalent circuit during Interval 5. **f.** Equivalent circuit during Interval 6.

Fig. 3 Equivalent circuits seen from the primary side of the power transformer in each interval.

By proper design, u_{d1} will decrease. When u_{d1} is lower than V_d, L_m starts to see a positive voltage that is V_d-u_{d1}, and the magnetizing current starts to rise. Its change is governed by

$$L_m \frac{di_m(t)}{dt} = V_d - u_{d1}(t) \qquad (9)$$

The secondary current rises in the similar fashion as (9).

The positive primary winding voltage increases as C_{snb} continues discharging, and it is coupled to the secondary side of T_r. Therefore, D_{o1} becomes forward biased. Owing to L_s, the current flowing through D_{o1} can only rise slowly. This secondary current is reflected back into the primary side. The value of L_s can be so selected that this reflected current can be limited and thus C_{snb} can be discharged completely by the end of this interval.

Similarly, u_a, the voltage of C_a, is governed by

$$\alpha \frac{d^4 u_a(t)}{dt^4} + \beta \frac{d^2 u_a(t)}{dt^2} + u_a(t) = (1-k_a)V_d \qquad (10)$$

and its solution has a similar form as of (5).

The current in the auxiliary circuit is determined by

$$i_a(t) = C_a \frac{du_a(t)}{dt} \qquad (11)$$

A current equal to $k_a i_a(t)$ flows through the secondary winding of T_a and D_1, feeding back the energy into the input dc line.

During this interval, D_{o2} is in freewheeling of the inductor current in L_o. At the end of this interval, $t = t_1$, and $u_{d1}(t_1) = 0$, $u_a = u_a(t_1)$ and $i_a = i_a(t_1)$.

B. Interval 2

At the beginning of this interval, $t = t_1$, C_{snb} is totally discharged. Forced by L_a, the resonant current i_a must continue in the same direction. Fig. 3.b shows the equivalent circuit of this interval.

It is found that

$$u_a(t) = [u_a(t_1) + k_aV_d]\cos\omega_3(t-t_1) + i_a(t_1)\sqrt{\frac{L_a}{C_a}}\sin\omega_3(t-t_1) - k_aV_a \qquad (12)$$

$$i_a(t) = -[u_a(t_1) + k_aV_d]\sqrt{\frac{C_a}{L_a}}\sin\omega_3(t-t_1) + i_a(t_1)\cos\omega_3(t-t_1) \qquad (13)$$

where

$$\omega_3 = 1/\sqrt{L_aC_a} \qquad (14)$$

A current equal to $k_a i_a(t)$ flows through the secondary winding of T_a and D_1, feeding back the energy into the input dc line.

As i_a flows, the body diode of Q_1 starts to conduct, clamping the drain voltage of Q_1 at zero volts. Hence, Q_1 can be turned on under ZVS at any instant between t_1 and t_2.

Now, L_m sees a constant voltage V_d, and the magnetizing current rises linearly, as determined by (9). So does the secondary current i_s that is also the current in L_s.

During this interval, D_{o2} is in freewheeling of part of the inductor current in L_o. At the end of this interval, $t = t_2$, and $i_a(t_2) = 0$, and u_a rises to $u_a(t_2)$.

C. Interval 3

At the beginning of this interval, $t = t_2$, the resonant current i_a in the auxiliary circuit crosses zero and it reverses its flowing direction. Fig. 3.c shows the equivalent circuit of this interval.

It is found that

$$u_a(t) = [u_a(t_2) - k_a V_d]\cos\omega_3(t - t_2) + k_a V_a \quad (15)$$

$$i_a(t) = -[u_a(t_2) - k_a V_d]\sqrt{\frac{C_a}{L_a}}\sin\omega_3(t - t_2) \quad (16)$$

A current equal to $k_a i_a(t)$ flows through T_a and D_2. The energy stored in C_a and L_a during the first two intervals is now fed back into the input dc line. Q_2 sees a negative drain current. Then, Q_2 can be turned off under ZVS at or shortly a after $t = t_3$, as its body diode conducts and clamps its drain voltage at zero.

L_m continues to see a constant voltage. The magnetic current is increasing linearly as governed by (9). So is the secondary current i_s.

During this interval, the reversed i_a continues. D_{o2} is in freewheeling of part of the inductor current in L_o. At the end of this interval, $t = t_3$, and $i_s(t_3) = P_o/V_o$.

D. Interval 4

At the beginning of this interval, $t = t_3$, the secondary current i_s reaches the value of the inductor current in L_o. D_{o2} becomes reverse biased. D_{o1} conducts the total inductor current in L_o. From now onwards, the power circuit transfers the power from the input line to the load in the same way as in a conventional forward converter. Fig. 3.d shows the equivalent circuit of this interval.

During this interval, the reversed resonant current i_a in the auxiliary circuit reaches zero Amperes again. As Q_2 is off, this current cannot cross zero and it is stopped.

At the end of this interval, $t = t_4$, and the duty ratio of the main switch is completed to regulate the output voltage.

E. Interval 5

At the beginning of this interval, $t = t_4$ Q_1 is turned off. C_{snb} slows down the rate of rise of the drain voltage u_{d1}. This helps in achieving a near ZVS turn-off of Q_1. Fig. 3.e shows the equivalent circuit of this interval.

When u_{d1} rises above the value of V_d. L_m starts to see a negative voltage. Thus, the magnetizing current starts to decrease.

The negative voltage is coupled to the secondary side of T_r. The current in L_s, i_s, starts to decrease. As the current in L_o is almost constant, D_{o2} is forced to conduct. Both D_{o1} and D_{o2} now conduct simultaneously until current through L_s becomes zero. The simultaneous conduction of D_{o1} and D_{o2} places the L_s across the secondary of T_r. L_s and C_{snb} undergo a resonance through the coupling of T_r. As long as i_s flows, it continues to charge C_{snb} through T_r, and u_{d1} continues rising.

It is found that

$$u_{d1}(t) = V_d - V_d\cos\omega_4(t - t_4) + \frac{P_o}{kV_o}\sqrt{\frac{L_e}{C_{snb}}}\sin\omega_4(t - t_4) \quad (17)$$

$$i_s(t) = -V_d\sqrt{\frac{C_{snb}}{L_s}}\sin\omega_4(t - t_4) + \frac{P_o}{V_o}\cos\omega_4(t - t_4) \quad (18)$$

where

$$\omega_4 = 1/\sqrt{L_e C_{snb}} \quad (19)$$

The magnetizing current is governed by (9).

F. Interval 6

At the beginning of this interval, $t = t_5$, i_s reaches zero and u_{d1} reaches the peak, $u_{d1}(t_5)$. Blocked by D_{o1}, i_s cannot cross zero and continue in resonance. Thus, only L_m and C_{snb} undergo a resonance. As L_m still sees a negative voltage, the magnetizing current continues to decrease, as governed by (9). Fig. 3.f shows the equivalent circuit of this interval.

It is found that,

$$u_{d1}(t) = V_d - [u_{d1}(t_5) - V_d]\cos\omega_5(t - t_5) + i_m(t_5)\sqrt{\frac{L_m}{C_{snb}}}\sin\omega_5(t - t_5) \quad (20)$$

where

$$\omega_5 = 1/\sqrt{L_m C_{snb}} \quad (21)$$

During this interval, D_{o2} is in freewheeling of the total inductor current in L_o. At the end of this interval, $t = T_s$, this switching cycle is completed and another cycle starts. The magnetizing current returns to the same value as at the beginning of this cycle. Thus, the core is reset.

IV. Design Procedure

The design for the power circuit is not repeated in the paper, as it is extensively discussed in the literature.

The following parameters are assumed known: (i) $V_{d\,\min}$ and $V_{d\,\max}$, the minimal and maximal input voltage, (ii) $D_{\max}$ and $D_{\min}$, the maximum and minimum duty ratio of Q_1, (iii) f_s, the switching frequency, (iv) L_m, the magnetizing inductance of T_r, (v) k, the turns ratio of T_r, (vi) V_o, the nominal output voltage, and (vi) P_o, the rated output power.

A. Selection of L_s

As stated previously, L_s is introduced to limit the rate of rise of the secondary current in Intervals 1 and 2. However, it will reduce the effective duty ratio of Q_1 in Interval 3. To limit this duty ratio reduction, L_s should be limited by:

$$L_s \le \frac{V_{d\,\min} V_o}{k f_s P_o} \Delta_d \tag{22}$$

where Δ_d is the allowable reduction of the effective duty ratio. Usually this reduction should be limitted under 0.1.

On the other hand, the residual energy in L_s when Q_1 is turned off must be large enough to reset the core. Thus, L_s should also be limited by:

$$L_s \ge \frac{D_{\max}^2 V_{d\,\min}^2 V_o^2}{2 f_s^2 P_{o\,\min}^2 L_m} \tag{23}$$

where $P_{o\,\min}$ is the minimal output power above which self reset can be achieved in T_r.

If L_s is selected only on basis of (22), then (23) sets a limitation either for selecting L_m or for workable range of the output power level.

B. Selection of D_{aux}

The duty ratio D_{aux} of the auxiliary switch is fixed and it should be limited by

$$D_{aux} \le (1 - 2D_{\max}) \tag{24}$$

C. Selection of C_{snb}

From (17), it is seen that C_{snb} determines the rises time of the drain-to-source voltage of Q_1 at its turn-off. Limiting u_{d1} below V_d within the required rise time t_r, C_{snb} should be limited by:

$$C_{snb} \ge \frac{P_o t_r}{k V_o V_{d\,\min}} \tag{25}$$

However, the rise time should not exceed the gap left by $2D_{\max}$ and D_{aux} in one cycle. This limits C_{snb} by

$$C_{snb} \le \frac{P_o}{2 k V_o V_{d\,\min}} (1 - 2D_{\max} - D_{aux}) \tag{26}$$

D. Selection of L_a and C_a

The reversed i_a in the auxiliary circuit during Interval 3 should complete its negative half cycle resonance within that interval. Hence, the following equation should be satisfied:

$$C_a \le \frac{D_{\min}^2}{\pi^2 f_s^2 L_a} \tag{27}$$

On the other hand, (11) and (13) indicate that L_a should be selected a large value in order to reduce the magnitude of the resonant current and hence the conduction losses in Q_2.

In order to achieve ZVS in Q_1, u_{d1} must reach zero Volts in Interval 1. (5) and (8) indicate that L_a is dependent on C_{snb}, L_s, and D_{aux}. The value of L_a can be found by numerical method. Fig. 4 shows an example of the design curves to select L_a.

E. Selection of T_a

The turns ratio k_a of T_a should be small to limit the reflected voltage of V_d seen on the primary side of T_a. Otherwise, this voltage, which is against the discharging current i_a in Interval 1, would become significant, C_{snb} could not be completely discharged, and ZVS would be lost in Q_1.

F. Selection of Q_2

A switch with low on-resistance and low inherent capacitance should be selected for Q_2. The voltage rating of Q_2 should be the same as Q_1. The current rating is determined by (13).

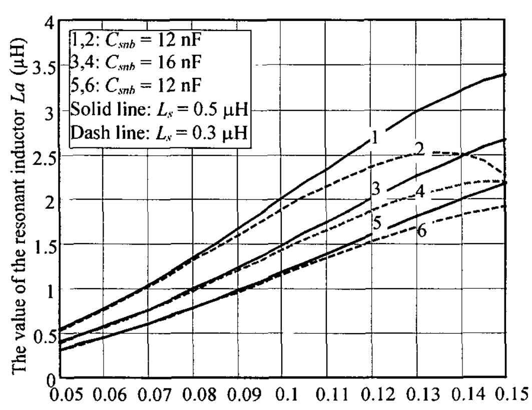


Fig. 4 An example of design curves for selecting L_a, as a function of C_{snb}, L_s and D_{aux}. In this example, $V_{d\,\max}$=60 V, f_s=200 kHz,, $D_{\min}$=0.2.

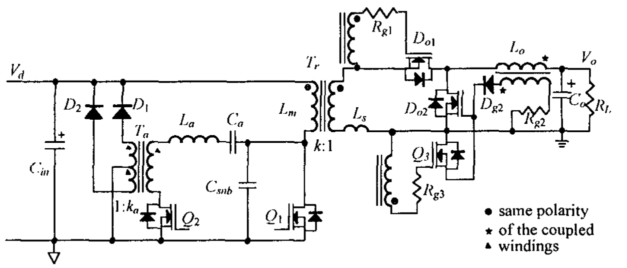


Fig. 5 The prototype converter. It employs self-driven synchronous rectifiers reported in [9]. The gate drives for synchronous rectifier D_{o1} is generated by a winding coupled to T_r, and for D_{o2} by a winding coupled to L_o. Q_3 helps to fast turn off D_{o2}. D_{g2} blocks the excessive negative gate voltage during D_{o2} is off and thus protects D_{o2}.

TABLE I
PRINCIPAL PARAMETERS OF THE EXAMPLE CIRCUIT

parameter		parameter	
$V_{d\,\min}$, V_{in_max}	35, 60V	C_{in}	100μF
P_o	100W (V_o=5V,I_o=20A)	L_o/C_o	12 μH / 400μF
$D_{\min}/D_{\max}$	0.2 / 0.40	Q_1	IRF640*
f_s	200kHz	D_{o1}/D_{o2}	MTP75N05*
L_m	160μH	Q_3	IRF510
k	3:1	Controller	UC3855AN
D_{aux}	0.1	k_a	1:7
C_{snb}	16nF	Q_2	IRF634
L_a/C_a	1.5μH/66nF	D_1, D_2	HFA08TB

* Two in parallel.

G. Selection of D_1 and D_2

D_1 and D_2 should be fast recovery diodes. Their voltage rating should be higher than $2V_{d\,\max}$, and their current rating should be higher than $f_s C_{snb} V_{d\,\max}$.

H. Design Example

A design example is given here. Fig. 5 shows the example circuit. Self-driven synchronous rectifiers that is reported in [9] are employed in the output stage of the circuit.

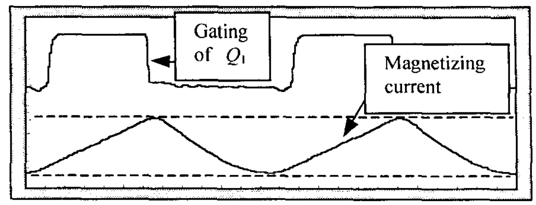
Table I shows the principal specifications and parameters of the power circuit and the auxiliary circuit of the prototype forward converter.

V. EXPERIMENTAL AND SIMULATION RESULTS

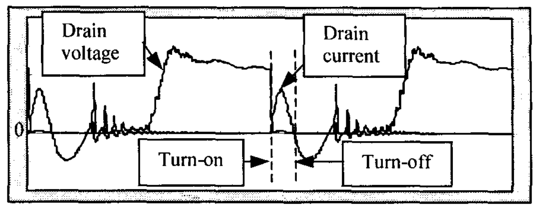
A prototype of 5 V, 100 W circuit operated at 200 kHz has been built. The circuit is shown in Fig. 5 and the circuit parameters are shown in Table I.

Fig. 6 shows typical simulation results. In 6.a, it is seen that the magnetizing current returns to the same point after each cycle, i.e., T_r achieves self reset. In 6.b and c, it is seen that ZVS is achieved in both the main and auxiliary switches.

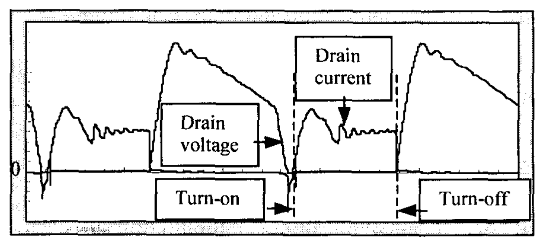
Fig. 7 shows the experimental waveforms of the main switch Q_1 under different operating conditions. It is seen clearly that ZVS is always achieved in Q_1.



a. Magnetizing current of the power transformer (Scale:10V/div., 0.5A/div.).

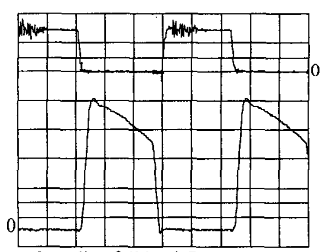


b. Key waveforms of auxiliary switch (Scale: 40 V/div., 5 A/div.).

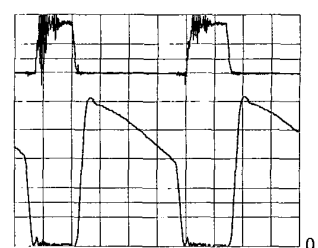


c. Key waveforms of main switch (Scale: 40 V/div., 5 A/div.).

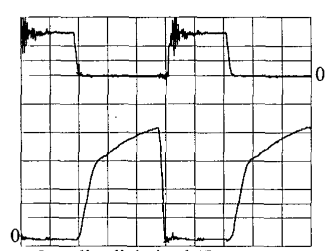
Fig. 6 Simulation results: key waveforms. Simulation conditions are: V_d = 50 V, f_s=200 kHz, P_o=90W.



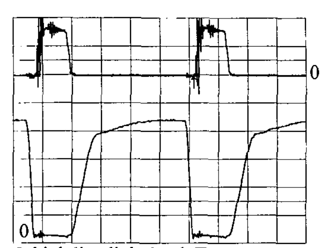
a. Low line full load. Top trace: gating. Bottom: drain voltage.



b. High line full load. Top trace: gating. Bottom: drain voltage.

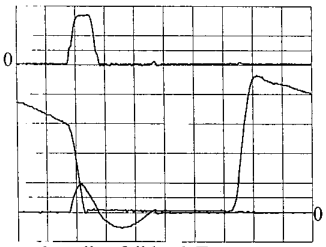


c. Low line light load. Top trace: gating. Bottom: drain voltage.

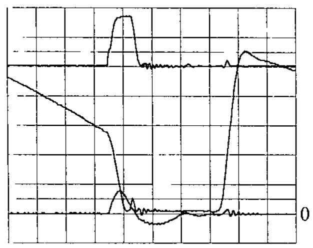


d. high line light load. Top trace: gating. Bottom: drain voltage.

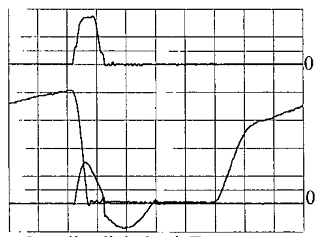
Fig. 7 Experimental waveforms of the main switch. f_s=200 kHz, high line V_d = 55 V, low line V_d = 35 V, full load P_o=90W, and light load P_o=30W. Scales: vertical-5 V/div. for gating signal, 20 V/div. for drain voltage; horizontal: 1 μs/div.



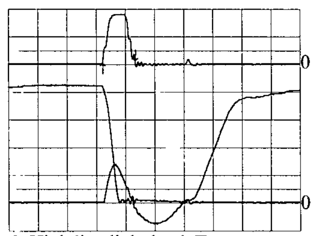
a. Low line full load. Top trace: gating. Middle: drain voltage. Bottom: drain current.



b. High line full load. Top trace: gating. Middle: drain voltage. Bottom: drain current.

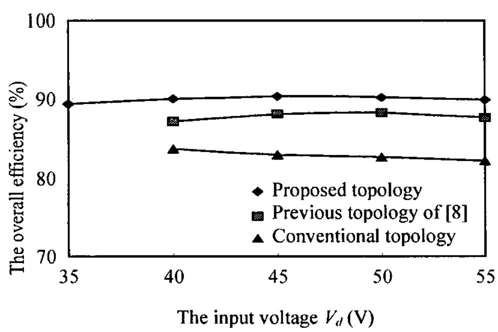


c. Low line light load. Top trace: gating. Middle: drain voltage. Bottom: drain current.

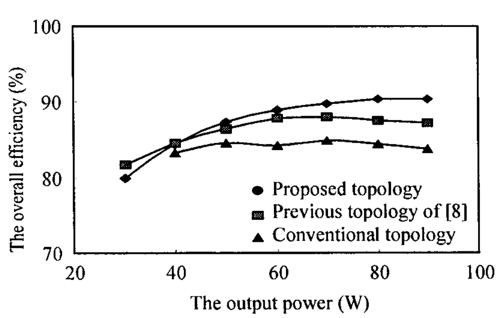


d. High line light load. Top trace: gating. Middle: drain voltage. Bottom: drain current.

Fig. 8 Key waveforms of the auxiliary switch of the experimental results. f_s=200 kHz, high line V_d = 55 V, low line V_d = 35 V , full load P_o=90W, and light load P_o=30W. Scales: vertical-5 V/div. for gating signal, 20 V/div. for drain voltage, 5 A/div. for drain current; horizontal: 0.5 μs/div.



a. The efficiency vs. input voltage at full load (90 W).



b. The efficiency vs. output power under fixed input voltage (45 V).

Fig. 9 The overall efficiency of the proposed ZVS converter topology.

Fig. 8 shows the experimental waveforms of the auxiliary switch Q_2 under different operating conditions. It is seen clearly that ZVS is always achieved in Q_2.

Fig. 9 shows the experimental results of the overall efficiency under different operating conditions. It is seen that the proposed topology has about 90% efficiency and it is almost constant over the entire range of input voltage. Also the proposed topology has about 2-3% better efficiency than the previously published ZVS forward topology [8].

VI. Conclusions

The proposed forward converter topology achieves ZVS in both the main and auxiliary switches, and the power transformer self resets without the use of conventional tertiary reset winding. The converter has about 90% overall efficiency over entire range of input voltage.

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