A Precisely Regulated Multiple Output Forward Converter Topology

Youhao Xi Praveen K. Jain

P. D. Ziogas Power Electronics Laboratory
Dept. of Electrical and Computer Engineering
Concordia University
Montreal, Quebec, CANADA H3G 1M8

Yan-Fei Liu

Dept. of Electrical and Computer Engineering
Queen's University
Kingston, Ontario
CANADA

***Abstract*-A precisely regulated multiple output forward converter topology is presented in this paper. In this topology, each output voltage is directly and independently regulated by its own feedback control circuit that controls the appropriate synchronous rectifiers in the pertinent output stage, while the main switch is feedforward controlled. Thus, there is no cross regulation between the outputs, and design of each output becomes straightforward. Steady state analysis is performed to understand the topology and to provide design guidance. A prototype circuit with two outputs is built, and experiment are carried out on this prototype and the results verify the concepts and design.**

I. Introduction

The forward converter topology has long been used in designing the distributed power supplies in tele-communication and computer systems, because of its capability to provide low ripple output voltage and high output current. However, in these systems, many electronic loads now require more than one supply voltage to power different devices on the same board, and the required supply voltages are becoming lower and lower. As the noise margin of the logic level under low supply voltage becomes smaller, tight regulation in each supply voltage must be guaranteed. The conventional forward topology is no longer suitable to fulfill the task in these applications.

The major problems here with the conventional multiple output forward topology are the poor regulation against load in the slave outputs, and the cross regulation between different outputs. To avoid such problems, a general practice is to use several single output converters, each providing a specific, well regulated supply voltage. Nevertheless it is bulky and costly, and this forces some designers to turn to the flyback topology. But the flyback is less preferable due to high ripples in the output voltage, large current stress on the switches, and also due to the difficulties in employing self-driven synchronous rectifiers.

To improve the multiple output regulation, the magnetic amplifier is usually used in each slave output stage to obtain post regulation [1]. Unfortunately, the magnetic amplifier can not be employed together with the synchronous rectifier, thus, it is not a solution to advanced applications where the required supply voltage can be as low as about 1.0 V and hence the synchronous rectifiers in the output stages are essentially needed.

In recent years, other post regulation techniques are developed for multiple output forward converter topologies [2-5]. But they are rather complicated in analysis, and difficult to design, owing to the complexity arising from cross regulation. Furthermore, precise regulation in each slave output is hardly obtainable owing to exacting matching and coupling of the magnetics. In some multiple output converters, the precise regulation is achieved by using a second stage buck converter in each output [6-7]. This sacrifices the overall efficiency, erases the natural simplicity of the forward topology, and increases the cost. The feedback loop from the output to input brings other problems, such as less reliable isolation between the input and output, narrowing the closed loop bandwidth due to the use of opto-coupler, and so on.

This paper presents a precisely regulated multiple output forward converter topology. The major features of the proposed topology include:

(i) feedforward control of the main switch, thereby enabling instant response in regulation of the output voltages against the input voltage variations,
(ii) independent feedback control of each output voltage, hence realizing precise regulation of each output voltage,
(iii) voltage decoupling among the outputs, therefore eliminating cross regulation;
(iv) no need of the feedback loop crossing the isolation boundary between the input and output, thereby permitting complete and reliable isolation.

Steady state analysis is performed to understand the topology. Based on the analysis, a design procedure is generated. A prototype circuit is built having two outputs, 5.0V 30Wand 2.0V 40W. The input voltage varies between 35V and 75V dc, and the switching frequency is at 200 kHz. Experiments are carried out on this prototype and the results verify the concepts and design.

II. Circuit Description

Fig. 1 shows the proposed multiple output forward converter topology. The topology consists of the following functional blocks: (i) a power transformer, (ii) a main switch MOSFET, (iii) a feedforward control circuit controlling the

0-7803-5864-3/00/$10.00 © 2000 IEEE

main switch S_{main}, and (iv) multiple output sub-circuits on the secondary side of the power transformer.

All the output sub-circuits have identical structures. For the k^{th} output, where k is any of the outputs, it consists of the following functional blocks: (i) a secondary order output filter comprised of L_{ok} and C_{ok}, (ii) two synchronous rectifier (SR) MOSFET switches, SR_{k1} and SR_{k2}, (iii) a small voltage decoupling inductor L_{sk}, and (iv) a feedback control circuit producing PWM for the bottom SR, namely SR_{k2}.

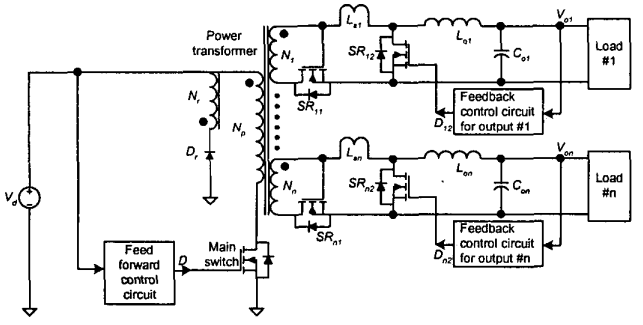


Fig. 1 The proposed precisely regulated multiple output forward converter topology.

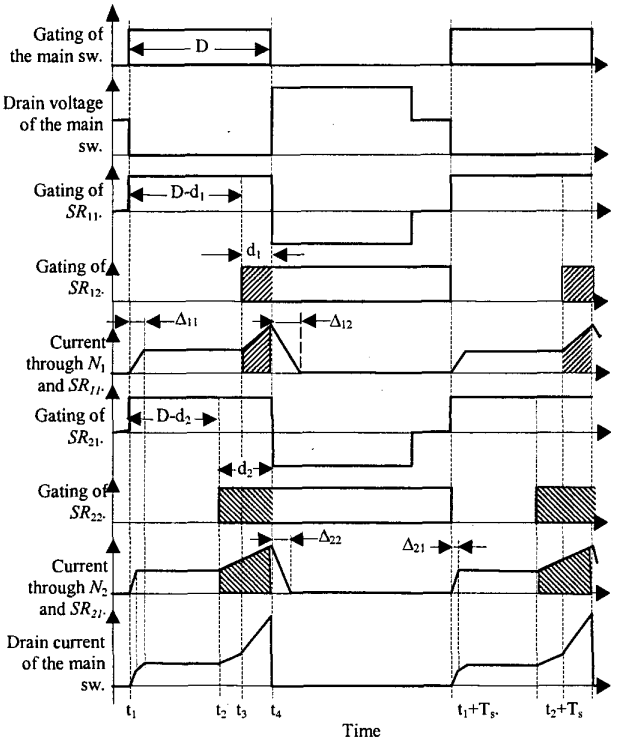


Fig. 2 Key waveforms of a two output converter of the proposed topology.

III. Operating Principle and Steady State Analysis

Fig. 2 shows key waveforms of the steady state operation of a two output converter of the proposed topology in Fig. 1. It can easily be extended to more outputs operation.

The main switch is feedforward controlled, and its gating signal is exclusively determined by the input voltage. During operation, the main switch has only two states, ON and OFF. However, every output circuit goes through five basic intervals in each switching frequency. The first three intervals happen during S_{main} is ON, and the rest two during S_{main} is OFF.

The following assumptions are made to perform the steady state analysis for the k^{th} output:

(i) The input and output dc voltage is at constant values, V_d and V_{ok}, respectively,
(ii) The load draws constant output current, I_{ok},
(iii) The switching frequency is f_s.
(iv) The output inductors are in continuing conduction mode,
(v) The components have linear properties,
(vi) The leakage inductance of T_r is ignored,
(vii) Each pair L_{ok} and C_{ok} make an ideal output filter.

The analysis will be made on the k^{th} output circuit.

A. Main Switch ON

As soon as S_{main} is ON, the top SR MOSFET in each output circuit is also turned on, as it is driven by the corresponding transformer winding. Thus, the duty ratio of the top SR in each output is D. While S_{main} is ON, each output circuit undergoes the following three intervals.

1) Interval 1

At the beginning of this interval, SR_{k1} is turned on, and SR_{k2} is OFF. Due to the series voltage decoupling inductor L_{sk}, the current i_{sk} that flows through SR_{k1} can only rise gradually from zero.

As the current through the output inductor is nearly constant, the body diode of SR_{k2} is forced to conduct when i_{sk} is rising. Then, L_{sk} will see a constant voltage that is the induced secondary voltage on the related winding. Therefore, i_{sk} is governed by

$$i_{sk}(t) = \frac{N_{sk} V_d}{N_p L_{sk}} (t - t_1) \tag{1}$$

This interval completes when i_{sk} reaches the value of the current flowing through L_{ok}, which is approximately the k^{th} output current I_{ok}. Thus, the duration of this interval as a fraction of a switching period is determined by

$$\Delta_{1k} = \frac{N_p f_s L_{sk}}{N_{sk} V_d} I_{ok} \tag{2}$$

2) Interval 2

At the beginning of this interval, i_{sk} reaches I_{ok}, the body diode SR_{k2} becomes reverse biased, the total output inductor current now flows through SR_{k1}, and the power is transferred from the input to the load as in a conventional forward converter.

This interval terminates when SR_{k2} is turned on at some time near the end of the ON period of the feedforward controlled SR_{k1}, in order to regulate the output voltage.

The duration of this interval is determined by (D-Δ_{1k}-d_k), where d_k is the duration of the next interval, the mutual conduction period of both SRs.

3) Interval 3 (t_3 to t_4)

Commanded by the feedback control circuit to regulate the output voltage, SR_{k2} will turn on at some time near the end of the ON period of SR_{k1}, say at a time ahead of the end of D by d_k. The mutual conduction of both SRs makes a short circuit, and this reduces the effective duty ratio of the top SR. Particularly, for Output #1, the effective duty ratio reduction is d_1, and for Output #2 it is d_2. Thus, the effective duty ratio for the k^{th} output is:

$$D_{eff\_k} = D - d_k \tag{3}$$

where D is the duty ratio of the main switch commanded by the feedforward control circuit.

In spite of this short circuit, the voltage cross the winding of the power transformer T_r does not collapse thanks to the decoupling inductor L_{sk}—it simply decouples this short circuit state from the pertinent winding, eliminating the cross regulation between different outputs. Because L_{sk} now sees the total voltage of the pertinent secondary voltage, the current through the inductor as well as the pertinent winding will rise linearly, as given by

$$i_{sk}(t) = \frac{N_{sk}}{N_p}\frac{V_d}{L_{sk}}(t - \frac{D-d_k}{f_s}) + I_{ok} \tag{4}$$

where I_{ok} is the load power of the k^{th} output.

At the end of this interval, i_{sk} reaches a peak value given by

$$I_{peak} = I_{ok} + \frac{N_{sk}}{N_p}\frac{V_d}{L_{sk}}\frac{d_k}{f_s} \tag{5}$$

B. Main Switch OFF

1) Interval 4

When S_{main} is turned off by the feedforward control circuit, the voltage polarity of each windings of the power transformer reverses. Thus, the top SR in each output circuit is also turned off.

However, the current in L_{sk} can not stop flowing instantaneously, and the body diode of the top SR (SR_{k1}) is forced to conduct the residual current in L_{sk}. This causes L_{sk} sees a negative voltage induced on its pertinent winding, and the current through L_{sk} start to decrease linearly.

Assume the resetting winding of Tr has the same number of turns as does the primary winding, then the current through L_{sk} is governed by

$$i_{sk}(t) = I_{peak} - \frac{N_{sk}}{N_p}\frac{V_d}{L_{sk}}(t - \frac{D}{f_s}) \tag{6}$$

This interval finishes when the residual current drops to zero, and the duration of this interval can be easily found to be $\Delta_{1k} = (\Delta_{2k} + d_k)$.

2) Interval 5

This is the last interval of one switching cycle. During this interval, the bottom SR is in freewheeling of the output inductor current, the same as in a conventional forward converter. Obviously, the duration of this interval is (1-D-Δ_1+d_k)

C. Characteristics of the Steady States Operation

Each output circuit can be represented by the Thevenin equivalent circuit. Thus, the output voltage is determined by

$$V_{ok} = V_k - R_{sk} I_{ok} \tag{7}$$

where V_k and R_{sk} are the Thevenin equivalent source voltage and resistance, respectively, of the the k^{th} output circuit, and

$$V_k = \frac{N_k}{N_p} V_d (D - d_k - \Delta_{1k}) \tag{8}$$

where $k = 1, 2, \ldots n$.

From (7) and (8), it is seen that, if the feedforward control circuit is programmed properly to generate required D, the output voltage can be regulated at reduced load by modulating d_k, or the overlap interval of the pair of SRs.

Solving from (2), (7) and (8), it is found that,

$$d_k = D - \frac{N_p V_o}{N_{sk} V_d} - \frac{N_p (f_s L_s + R_{sk})}{N_{sk} V_d} I_{ok} \tag{9}$$

As seen from (5), the peak current in the circuit increases with d_k, or the short circuit interval, and so do the conduction losses. In order to limit the conduction losses, it is expected that d_k shall be as small as possible.

As seen from (9), for a given input voltage or D, the maximum d_k results from no load conditions, while the minimum d_k takes place at full load conditions. as the load current I_{ok} decreases. Thus, to minimize the conduction losses, the optimal design is to set d_k to be zero at full load.

Equation (9) also shows that, at reduced load, the short circuit interval d_k increases with the equivalent source resistance. Thus, to limit this short circuit interval, use low $R_{DS(on)}$ switches for S_{main} and SRs, optimize the magnetics and the circuit layout.

Fig. 3 shows the effective duty ratio reduction by the short circuit interval as functions of different parameters in the 5V 30W output circuit of the prototype converter.

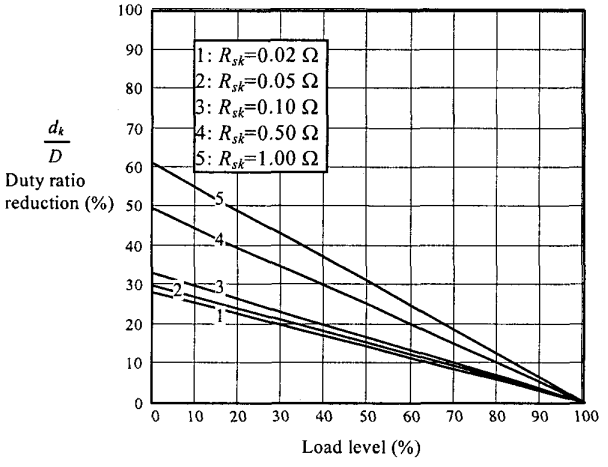
On the other hand, the rms current through a component is determined by

$$I_{rms} = \sqrt{f_s \int_0^{1/f_s} i^2 dt} \qquad (10)$$

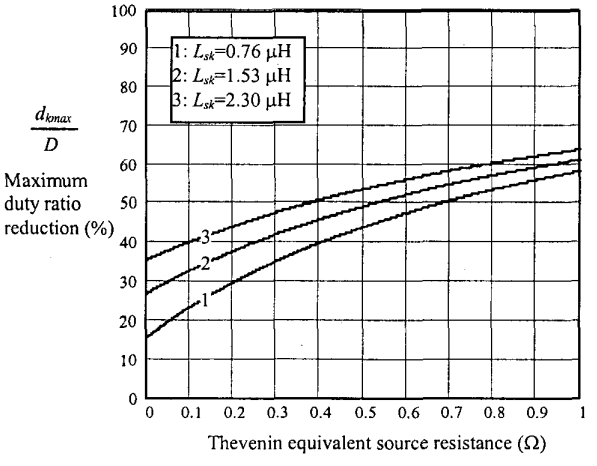
where i is the instant current through the component.

By investigating the current in each interval, the rms current can be obtained. Fig summarizes the properties of the rms current in both top and bottom SRs as functions of the load current I_{ok}, equivalent source resistance R_{sk}, and the decoupling inductor L_{sk}, in the 2V 40W output circuit of the prototype converter.

All these curves show that, when the circuit is designed properly, the short circuit interval can be limited, and independent regulation can be achieved, and excessive rms current or conduction losses cane be prevented from occurring.

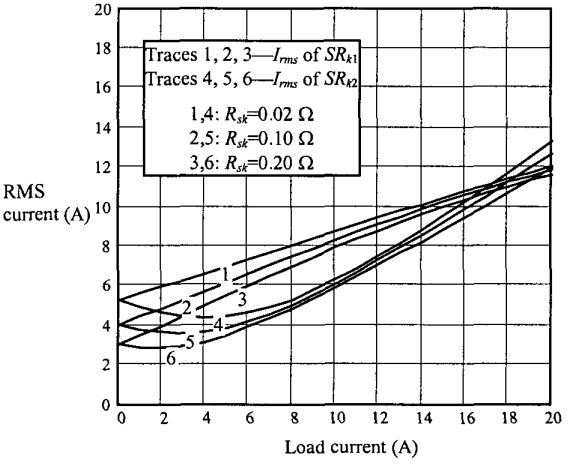


a. Reduction of the effective duty ratio vs. load level.

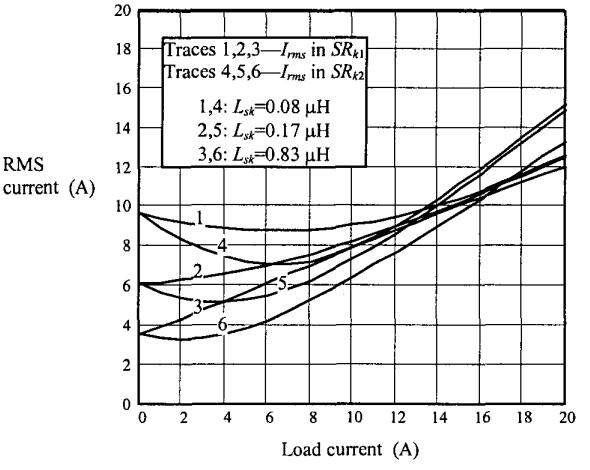


b. The maximum duty ratio reduction vs. equivalent resistance R_{sk}.

Fig. 3 The effective duty ratio reduction by mutual conduction of the pair SRs vs. the load condition, decoupling inductor, and Thevenin equivalent source resistance in the 5V output of the prototype circuit. P_o=0 to 30 W, f_s=200kHz.

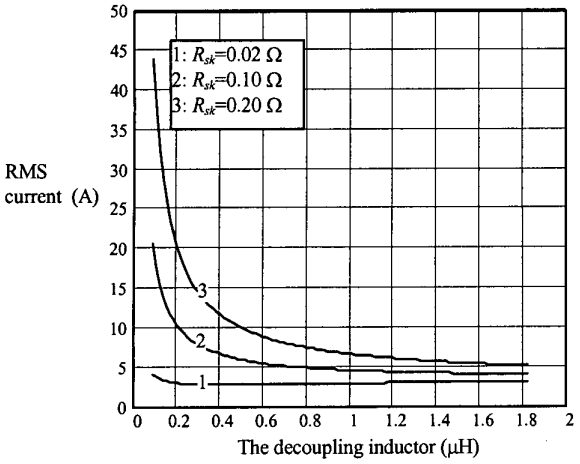


a. RMS currents both SRs vs. load current and the equivalent resistance R_{sk} in the 2V 40W output circuit. L_{sk}=1.65 μH, V_d=50V, f_s=200kHz.

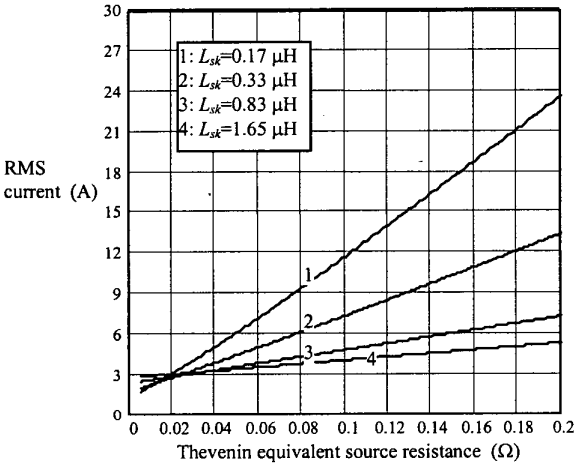


b. RMS currents both SRs vs. load current and the decoupling inductor L_{sk} in the 2V 40W output circuit. R_{sk}=0.05 Ω, V_d=50V, f_s=200kHz.

Fig. 4 (to be continued) The rms current through the 2V output circuit of the prototype circuit as functions of the load condition, decoupling inductor, and Thevenin equivalent source resistance.



c. RMS currents both SRs vs. the decoupling inductor L_{sk} in the 2V 40W output circuit under open circuit conditions. I_{ok}=0A, V_d=50V, f_s=200kHz.



d. RMS currents both SRs vs. the equivalent resistance R_{sk} in the 2V 40W output circuit under open circuit conditions. I_{ok}=0A, V_d=50V, f_s=200kHz.

Fig. 4 The rms current through the 2V output circuit of the prototype circuit as functions of the load condition, decoupling inductor, and Thevenin equivalent source resistance.

IV. Design Procedure

Based on the analysis, the design procedure can be readily generated. Following are the selection criteria of each key component. The curves in Fig. 3 and Fig. 4 should be consulted to refine the selection of each component.

A. D

The maximum D at the lowest input voltage should be limited below 0.5, if the reset winding has the same turns as does the primary winding, so as to guarantee successful reset of the power transformer in each switching cycle. However, the maximum D shall not be too small, or higher output filter may be required to meet the application specifications on ripples. 0.4 to 0.45 are good values for the maximum D at the lowest input voltage.

B. S_{main}, SR_{k1} and SR_{k2}

All these switches should have the least $R_{DS(on)}$, as seen in Fig. 4. They must also meet the rating requirement.

The rms current at full load condition is almost the same as in the conventional forward circuit, but at reduced load, short circuit by the SRs seems increasing the peak current. However, by consulting Fig. 4, the rms current at reduced load can be kept lower than the rms current at full load, if the circuit is designed properly.

In short, selection of the main and SR switches can follow the conventional design procedure.

C. N_p/N_{sk}

Selection of the magnetizing inductance of the power transformer can follow the conventional design procedure, as the operating of the proposed converter topology does not change the way the forward transformer operates.

In selecting the turns ratio, it is determined by

$$\frac{N_p}{N_{sk}} = \frac{D_{\max} V_{d\min}}{V_{ok} + (R_{sk} + f_s L_{sk}) I_{ok}} \tag{11}$$

D. L_{sk}

It is noticed from (2) that, even if d_k is zero under full load, a reduction of effective duty ratio by L_{sk} still exists, i.e. Δ_{k1}, and this reduction increases with L_{sk}. A higher duty ratio reduction should be avoided, otherwise a larger output inductor must be employed to limit the ripples in the output.

On the other hand, as seen from Fig. 4, L_{sk} should not be too small, or excessive rms current and hence excessive conduction losses would be resulted.

Therefore, tradeoff must be made in selecting L_{sk}. In the prototype converter, Δ_{k1} is set to 0.05 to 0.1. Thus,

$$L_{sk} = \frac{N_{sk} V_d}{N_p f_s I_{ok}} \Delta_{1k} \tag{12}$$

It is important to point out that, L_{sk} must be prevented from saturation under the worst case conditions, otherwise, it loses the voltage decoupling function, and then failure of whole circuit happens.

The output filter can also follow the conventional design. Techniques in [8-10] can be used to achieve soft switching of the main switch and self reset of the power transformer, to further improve the converter's performance.

E. *An design example*

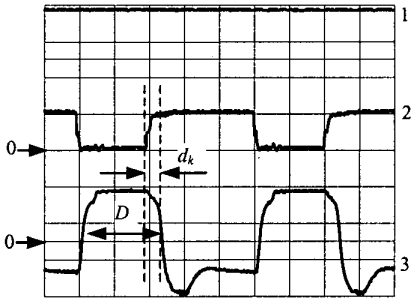
The principal parameters of the prototype converter are shown in Table I.

Table I Principal parameters of the prototype converter

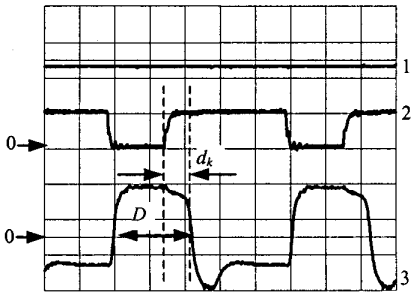
Parameter	Specifications	Components	Selections
V_d	35-75 V dc	N_p/N_{s1}	3
f_s	200 kHz	N_p/N_{s2}	1.2
V_{o1}	5.0 V	L_{s1}/L_{s2}	1.2 μH/0.36μH
I_{o1}	6.0 A	SRs	MTP75N05
V_{o2}	2.0 V	S_{main}	IRF640
I_{o2}	20 A	L_{o1}/C_{o1}	32μH/120μF
D_{max}	0.45	L_{o2}/C_{o2}	4.2μH/120μF

V. Experimental Results

Experiments are carried out on the prototype circuit to verify the concepts of the proposed converter. During the test the circuit can only output 12 A at the 2V output and 3A at the 5V output. Full load current is not obtainable in this breadboard prototype due the higher voltage drops along the current path, and also due to the improperly designed power transformer turns ratio, otherwise the regulation is lost. This problem can be overcome by using a higher turns ratio in the power transformer in the future work.

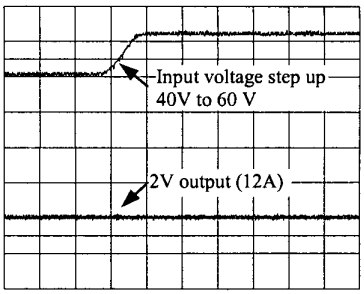


a. The gating of the SRs at full load for the 2 V output. I_o=12 A.

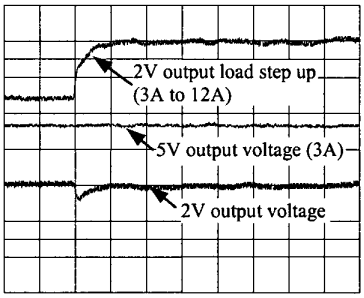


a. The gating of the SRs at no load for the 2 V output. I_o=0 A.

Fig. 5 The gating of the SRs under different load conditions for the 2V output. V_d=55V, f_s=200kHz. Scales: timimg-1us/div.; voltage-10V/div.; current-10A/div. Traces:1-load current; 2-gating of the bottom SR; 3-gating of the top SR

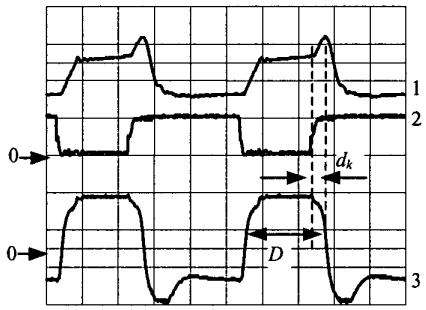


a. The output voltage vs. input voltage step up. Timing-10ms/div.

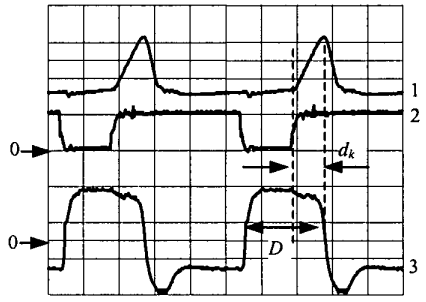


b. The output voltage vs. load step up. Timing-0.1ms/div. V_d=55V.

Fig. 6 The precise and independent regulation of each output voltage against input and load variation.



a. The current through the top SR of the 2V output at full load (12A)



b. The current through the top SR of the 2V output at no load (0A)

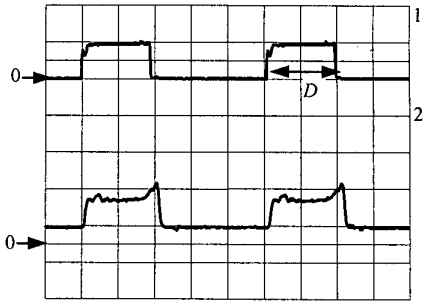
Fig. 7 The current flowing through the top SR current at different load conditions for the 2 V output. V_d=55V, f_s=200kHz.. Scales: timimg-1μs/div.; voltge-10V/div; current-10A/div. Traces:1-top SR current; 2-gating of the bottom SR; 3-gating of the top SR .

Fig. 5 shows gating patterns for the SRs in the 2V output vs. the load conditions under given input voltage. It is seen that the mutual conduction interval increases as the load decreases from full load to open circuit (no load). This confirms with the analysis in the last section and proves the design.

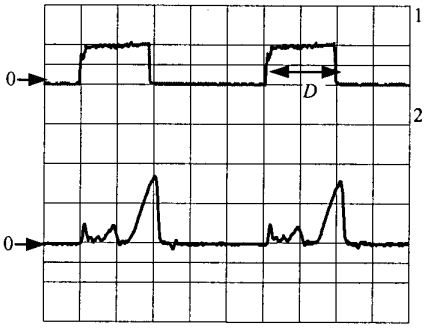
Fig. 6 shows the independent and precise regulation in the two outputs against variations in the input and loads, experimentally verifying the concepts of the proposed converter topology. It is seen in Fig. 6a that, due to the instant response of feedforward control circuit, the output is immunized of disturbance under input voltage variations. In Fig. 6b, it is clear seen that, a large step change in one output does not affect the other output voltage. The details of the dynamic properties of the topology are given in [11].

Fig. 7 shows the current through the top SR in the 2V output circuit vs. load conditions under given input voltage. It is seen that, although the mutual conduction interval is increased at no load, the peak current does not go excessive. Moreover, the rms current is seemingly lower at no load than that at full load conditions. It is also seen that even at open circuit, although the mutual conduction interval of both SRs is at the maximum.

Fig. 8 shows the drain current of the main switch under different load conditions. It is seen that, at no load at all, although the mutual conduction interval of all pair SRs is at the maximum, the main switch does not suffer from excessive rms current. This attributes to the decoupling inductors that simply limit the short circuit current caused by the mutual conduction of the SRs through each output circuit.



a. Current through the main switch under full load



b. Current through the main switch under no load conditions (both outputs open circuit).

Fig. 8 Main switch current under different load conditions. Traces: 1-gating of S_{main}; 2-drain current of S_{main}. V_d=55V Scale: timing-1μs/div; current-2A/div.;voltage-10V./div.

VI. Conclusions

The proposed topology enables precise and independent regulation of multiple outputs. The feedforward control of the main switch allows instance response in regulation against input voltage variations. Each output circuit has an independent feedback control circuit that regulates the output voltage by controlling the synchronous rectifiers. The decoupling inductor between the power transformer and each output circuit eliminates cross regulation between the outputs. Analysis of the proposed topology reveals its characteristics and properties, and a design procedure is generated. By proper design, the circuit will not suffer from excessive rms current and hence conduction losses. The concepts and design are verified experimentally.

Acknowledgment

The work reported in this paper is performed as a NSERC Collaborative R&D Program between Nortel Networks and Concordia University. The authors would like to thank Analog Devices, Inc. for providing samples of mutipler/ divider.

Reference

[1] A. I. Pressman, *Switching Power Supply Design*, McGraw-Hill, 1991, pp.381-412

[2] H. Matsuo, "Comparison of multiple output dc/dc converter using cross regulation," *IEEE PESC'79 Record*, pp.169-185.

[3] R. Erickson and D. Maksimovic, "Cross regulation mechanisms in multiple output forward and flyback converters," *IEEE APEC'99 Seminar 8.*

[4] Y. Lin, K. Liu, "A new synchronous switch post regulator for multi-output forward," *IEEE APEC'90 Record*, pp. 693-696.

[5] J. A. Carasco, J. B. Ejea, A. Ferreres, E. J. Dede, "A multiple output regulator using the variable transformer turns ratio regulator technique," *IEEE PESC'95 Record*, pp.1098-1103.

[6] K. Harada, T. Ninomiya and T. Nabeshima, "On the precise regulation of multiple outputs in a dc-dc converter with an energy storage reactor," *IEEE PESC'79 Records*, pp.

[7] H. Matsuo and F. Kurokawa, "Precise Regulation of multiple output voltages in a dc-dc converter", *IEEE.PESC'80 Records*, pp. 275-283.

[8] Y. Xi, P. Jian, G. Joos and H, Jin, "A zero voltage switching forward converter topology", *IEEE INTELEC'97 Record*, pp. 116-123.

[9] Y. Xi, P. Jain, Y. Liu and R. Orr, "A modified zero voltage switching forward converter topology with self core reset", *IEEE PESC'99 Record*, pp. 281-286

[10] Y. Xi, P. Jain, Y. Liu and R. Orr, "A zero voltage switching and self reset forward converter topology", *IEEE APEC'99 Record*, pp. 827-833.

[11] Y. Xi and P. Jain, "Small signal model and control of an independently regulated multiple output forward converter topology", to be presented in IEEE APEC'2000.