A New Power Factor Correction (PFC) Control Method Suitable for Low Cost DSP

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Abstract:
One main barrier to implement digital control for power factor correction (PFC) is the limited switching frequency due to the limited processor speed. A new digital PFC control method is proposed to solve this problem. For conventional digital methods, the duty cycle is calculated every switching period. The new digital PFC control method uses an optimization algorithm to generate all of the required duty cycles for one half line period at one time in advance, which is based on the input current and duty cycles in the previous half line periods. Total Harmonic Distortion (THD), which is directly related to the power factor, is determined as the objective function. Gradient descent is used as the optimization algorithm to minimize the THD and improve the power factor. The proposed new digital PFC control strategy overcomes the problem of limited switching frequency due to limited DSP speed. Simulation results show that unity power factor is achieved using the proposed method.

1. *Introduction*

Analog control is the traditional method of power factor correction (PFC) in AC-to-DC converter. Because of the advantages of the digital control over the analog control, it is necessary and possible to use DSP in PFC circuit to achieve unity power factor. Digital control has many advantages over analog control, including programmability, adaptability, less part count, less susceptibility to environmental variations, and more immunity to the input voltage distortion, etc.. Some work has been done to make the digital control a competitive option in PFC implementation as compared with analog control. Unfortunately, all of the existing control technique can not take full advantages of the DSP. In addition, the switching frequency of the converter is limited by the speed of the DSP.

A new digital PFC control method is proposed in this paper. An optimization algorithm is used to find the required duty cycles to achieve unity power factor in the proposed PFC control method. One significant characteristic of the new digital PFC control strategy is that the switching frequency is not directly dependent on the speed of the DSP. Therefore, a low speed/low cost DSP or microprocessor could be fast enough to generate the duty cycles for the switch operating at high switching frequency (e.g., 400kHz).

In this paper, the existing digital control methods for PFC are reviewed and their problems are highlighted in section 2. The principle of the new digital PFC control strategy is presented in section 3. Determination of objective function and the optimization algorithm are introduced in section 4. In section 5, the required CPU time to implement the proposed PFC control algorithm is estimated. The simulation results are given in section 6. In section 7, conclusion is presented.

2. Problems of the Conventional Digital PFC Control

Almost all of the existing digital PFC control methods are based on the conventional analog control laws. In other words, the existing digital PFC control methods implement the analog control law in the digital form. Because of the sampling delay and necessary processing time, the switching frequency is limited even when the latest and fastest DSPs are used. Average current control, which is one of the main conventional analog control strategies, as shown in Fig.1, is used in digital controlled PFC [1-4]. The average inductor current i_L is forced to follow the reference current i_{ref}, which is proportional to the rectified voltage, so that unity power factor is achieved. In the average current control, the duty cycle is determined in every switching period T_s based on the feedback current and the reference current. In order to achieve PFC, DSP or microprocessor is used to calculate the duty cycle for the switch S in every switching period T_s. If single sampling in single period method (SSSP) [5] is adopted, the maximum switching frequency is only about 50kHz when a DSP with high performance and high clock frequency (TMS320LF2407, 30MHz) is used. The problem of limited switching frequency is one of the main barriers of digital implementation for PFC.

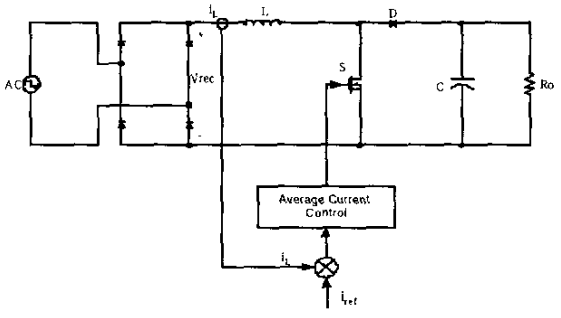

Fig.1 Average current control of the Boost PFC

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Reference [6-7] presented a digital control strategy that updates the duty cycle only once in m switching periods using predictive dead-beat (PDB) control for the purpose of increasing the switching frequency. However, this implementation works well only under the ideal situation because that the reference current and input voltage are determined by the look-up table. Another disadvantage is that the current waveform will be dependent on the accuracy of the inductance value when the proposed predictive control method is implemented by the hardware. In addition, the THD is increased with the increscent m.

Based on above analysis, the first problem of the existing digital control is that the high performance digital controller is almost exclusively used to control the PFC stage that operates at the relatively low switching frequency. This is because that the DSP can not complete all the calculation and control tasks in one switching cycle if the switching frequency is too high. In the digital controlled PFC system, if the switching frequency is 400kHz, one switching cycle is only 2.5 μs. This imposes very high requirement for the speed of the DSP. The higher the switching frequency, the faster the DSP required. Second, the implementation of the digital control method in the PFC application is limited due to the high cost. Third, even when the fastest DSP is used in the digital controlled PFC system, the switching frequency can not reach the same level as that in the analog controlled PFC system.

All the above problems can be solved by the new digital control PFC strategy proposed in the following section.

3. New Digital PFC Control Method

In this section, a new digital control method for AC-to-DC converter is proposed.

3.1 Unique Duty Cycle Set to Achieve PFC

It is noted that in AC-to-DC converter, there is a duty cycle set D in every half line period by which the unity power factor can be achieved. For example, if a Boost PFC circuit works at switching frequency of $f_s = 100KHz$ and line frequency of $f_{line} = 50Hz$, the number of the duty cycles in half line period is 1000 $(= 100{,}000 / 2 \times 50)$. That means, in every half line period, there are 1000 specific duty cycles $d_1, d_2, ..., d_{1000}$ to achieve unity power factor. The duty cycle set D, which consists of these specific duty cycles, can also achieve unity power factor. The problem is how can these specific duty cycles be generated or found?

In the analog controlled PFC circuit based on average current mode control, the unity power factor is obtained by forcing the average inductor current i_L to follow the reference current signal i_{ref}. In that method, the duty cycles d_i $(i = 1, 2, ..., 1000)$ of the duty cycle set D are determined in every switching cycle according to instantaneous time sequence based on the feedback current i_L and the reference current i_{ref}. It is easy to implement this control method using analog device because analog circuit is fast.

But in the digital controlled PFC circuit using the same average current mode control algorithm, the switching frequency is limited due to the required sampling and processing time. If the duty cycles are calculated one by one within every switching cycle, the switching frequency can not reach the same value as that in the analog circuit even when the latest DSP is implemented. For example, if the switching frequency is 400kHz, the duty cycle should be calculated and provided in every 2.5 μs. It is not long enough to accomplish all of the work in one switching period, including sampling the average current, achieving the voltage and current regulator, calculating the duty cycle and so on. Therefore, the higher the switching frequency, the faster the CPU required.

3.2 Principle of the New Digital PFC Control Method

A new digital PFC control method is proposed to solve this problem. One key point of the proposed control method is that all the required duty cycles for one half line period are generated at one time in advance. Another key point is that an optimization algorithm is used to find the required duty cycles to achieve unity power factor. Fig.2 illustrates the basic principle of the proposed new digital control PFC strategy.

In Fig.2, the optimization algorithm is implemented by a DSP. The inputs of the optimization algorithm are previous inductor current $i_L|_{p,p-1,...,p-n}$ and previous duty cycles $D|_{p,p-1,...,p-n}$. The output of the optimization algorithm is the required duty cycles for next half line period. The required duty cycles are determined by the optimization algorithm.

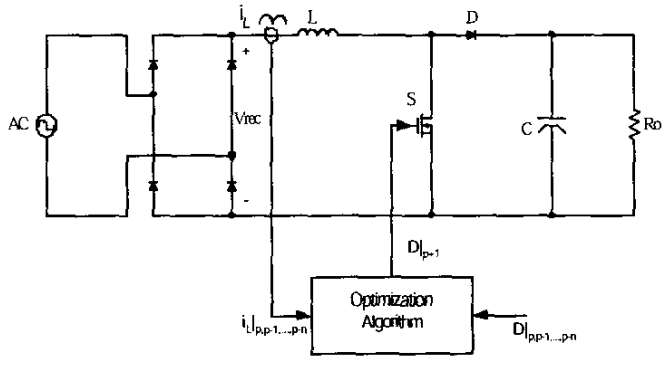


Fig.2 Proposed new digital control PFC scheme

Total Harmonic Distortion (THD) is used as the objective function for the optimization algorithm because the power factor is increased when THD is decreased. Gradient descent

is used to minimize THD and achieve PFC in optimization algorithm.

The duty cycle set for next half line period, $D|_{p+1}$, is determined by the optimization algorithm based on the previous inductor current $i_L|_{p,p-1,\ldots,p-n}$ and previous duty cycle set: $D|_{p,p-1,\ldots,p-n}$. The optimization algorithm calculates the new duty cycle set $D|_{p+1}$ for the next half line period so as to achieve a higher power factor. The power factor will be over 0.99 after a number of iterations of the optimization. Once the unity power factor is achieved, the duty cycle set is just "copied" from the previous one if the steady state is remained.

It is noted from the above analysis that by using the proposed method, the switching frequency is not directly dependent on the speed of the DSP. A relatively low speed DSP will be fast enough to generate the duty cycles for high switching frequency (e.g., 400kHz). The proposed new PFC control method essentially overcomes the switching frequency limitation in the digital implementation.

3.3 Output Voltage Control

Digital controlled PFC system should not only achieve unity power factor, but also regulate the output DC voltage. The diagram shown in Fig.3 is proposed to egulate the output voltage.

First, the output voltage is processed via a low-frequency filter to eliminate the line frequency ripple. Then the feedback signal is compared with the reference voltage and the error serves as the input of the voltage loop PI controller. The output of the PI controller, K_{pi}, is the scaling factor for the duty cycles determined by the optimization algorithm. The product of the multiplier is the duty cycle to control the switch S.

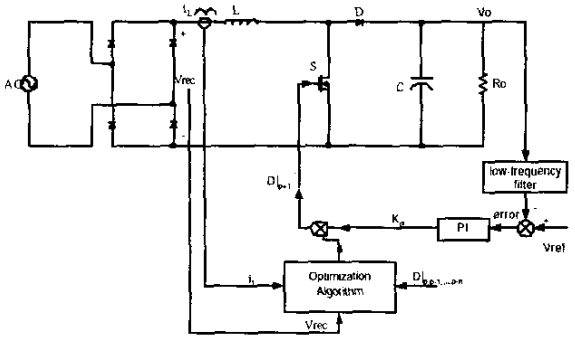


Fig.3 Output voltage control scheme

Similar to the analog control, the bandwidth of the voltage loop should be much lower than the double line frequency. If the bandwidth is closed or higher than the double line frequency, the inductor current waveform will be distorted and the harmonic current will be increased.

4. Optimization Algorithm

The optimization algorithm is used to find the duty cycle set for every half line period so as to achieve the unity power factor.

4.1 Determination of the Objective Function

An important subject of the new digital control PFC method is how to determine the objective function when the optimization algorithm is implemented. In this paper, Total Harmonic Distortion (THD) of the input current is chosen as the objective function.

The objective of the digital control PFC algorithm is to achieve a high power factor. The ideal situation is unity power factor. The power factor (PF) is defined as

$$PF = \frac{(average\ \ power)}{(rms\ \ valtage)*(rms\ \ current)} = (distortion\ \ factor)*(displacement\ \ factor) \quad (1)$$

In the rectifier cascaded by a PFC circuit, the displacement factor is one. So if the distortion factor approaches one, unity power factor is realized. The relation between distortion factor and THD is expressed by

$$(distortion\ \ factor) = \frac{1}{\sqrt{1+(THD)^2}} \quad (2)$$

If THD of the line current is minimum, the distortion factor is maximum and the power factor becomes maximum too. Zero THD means unity power factor. Therefore, the THD of input current can be used as the objective function in the new digital PFC control algorithm.

The relation between the THD and the duty cycles in one half line period is a very complicated nonlinear function. It can only be expressed as

$$(THD)|_p = f(D|_p, v_{in}, i_L(0), V_o, R_o) \quad (3)$$

Where $(THD)|_p$ is the Total Harmonic Distortion with the duty cycle set $D|_p$ in the p^{th} half line period, and $D|_p = [d_1, d_2, \ldots, d_i, \ldots, d_n]^T$. V_{in} is the input line voltage and $v_{in}(t) = V_{pk} \cdot \sin(2\pi ft)$. V_{pk} is the peak value of the line voltage and f is the line frequency. In the steady state, V_{pk} does not change. V_o is the output voltage and, in the steady state, V_o does not change either, $V_o = V_{dc}^*$. $i_L(0)$ is the initial inductor current in p^{th} half line period, $i_L(0) = 0$. Assuming that R_o does not change in a period which is longer enough to complete the optimization routine, (3) can be simplified as

$$(THD)|_p = f(D|_p) \quad (4)$$

The above equation shows that the THD depends on the duty cycle set in that half line period.

It is necessary to calculate the gradient vector components of the objective function (4) in order to implement the optimization algorithm. Unfortunately, it is too complicated

to perform the differentiation $\frac{\partial f}{\partial d_i}$ calculation analytically.

According to the secant approximation, the gradient vector component of the function (4) can be calculated as

$$\frac{\partial f}{\partial d_i} \approx \frac{f(d_1, d_2, ..., d_i + \Delta d_i, ..., d_n) - f(d_1, d_2, ..., d_i, ..., d_n)}{\Delta d_i} \qquad i = 1, 2, ..., n \qquad (5)$$

(5) can be achieved in the digital controller of the PFC system.

After the gradient vector components are calculated from (5), the THD of the line current can be reduced by the gradient descent optimization algorithm. So the unity power factor is achieved.

4.2 Optimization Algorithm-Gradient Descent

The proposed optimization algorithm in the digital controlled PFC circuit is based on gradient decent. The gradient of a differentiable function, $f(D|_p)$, with n variables, is the n-dimensional vector

$$\nabla f(D|_p) = \left[\frac{\partial f}{\partial d_1}(D|_p), \frac{\partial f}{\partial d_2}(D|_p), ..., \frac{\partial f}{\partial d_n}(D|_p)\right]^T \qquad (6)$$

where $f(D|_p)$ is the objective function. This vector defines the direction called gradient direction, which is the basis of all gradient algorithms. It is the direction of the steepest descent for minimization problems or the steepest ascent for maximization problems[8,9].

The gradient vector components can be calculated from (5), which can be implemented easily by a DSP or a microprocessor. Once the gradient direction is known, the gradient algorithm, which takes a point $D|_p \in S \subset E^n$ (or points $D|_p, D|_{p-1}, ...$) and defines a new point $D|_{p+1} \in S \subset E^n$, can be written in discrete form

$$D|_{p+1} = D|_p + k\nabla f(D|_p) \qquad (7)$$

where k is an arbitrary step size. In this paper, the condition k<0 is required to minimize the objective function THD.

4.3 An Implementation Example

The implementation of the proposed digital control algorithm can be understood better using the following example.

Assume the Boost PFC system operates at 100kHz switching frequency and the line frequency is 50Hz. There are 1000 duty cycles in one duty cycle set D (in every half line period). The objective is to find the value of the 1000 duty cycles to achieve the unity power factor.

Theoretically, the gradient of the function $f(D)$ is a 1000-dimentional vector. However, it is not only unnecessary but also impossible to implement the optimization using a 1000-dimentional gradient in the real time control system. In order to reduce the amount of calculation and the time for digital controller to achieve the optimization algorithm, these 1000 duty cycles are divided into 20 subsets. Therefore, there are 50 duty cycles in every subset. Each subset is processed as one component of the gradient vector. So the gradient can be expressed as a 20-dimentional vector

$$\nabla f(D) = [\frac{\partial f}{\partial D_1}(D), \frac{\partial f}{\partial D_2}(D), ..., \frac{\partial f}{\partial D_{20}}(D)]^T \qquad (8)$$

where, $D = [D_1, D_2, ..., D_{19}, D_{20}]$ is the duty cycle set. $D_1, D_2, ..., D_{19}, D_{20}$ are the subsets of the duty cycle set D, $D_1 = [d_1, d_2, ..., d_{50}]^T$, ..., $D_{20} = [d_{951}, d_{952}, ..., d_{1000}]^T$.

In digital implementation, the gradient algorithm is implemented according to the following steps and time sequences, as shown in Fig.4. The optimization starts at the #1 half line cycle. There are 22 half line periods in one optimization iteration. The duty cycle set $D|_p$ is the result of the previous optimization iteration and the optimized result of the current iteration is $D|_{p+1}$. The following steps provide the details of the implementation.

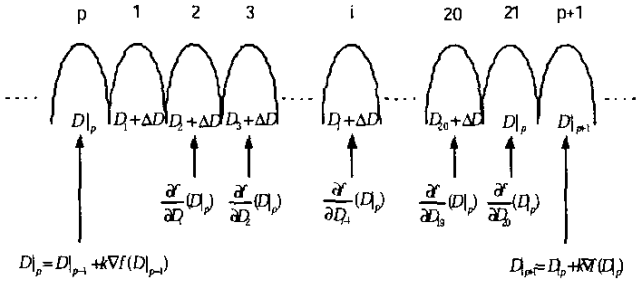


Fig.4 Step and time sequence of the optimization routine ($1 \le i \le 20$)

(I). Initial Condition

In p^{th} half line period, Boost PFC is assumed operating at the steady state. The duty cycle set is $D|_p$ and its duty cycle subsets are: $D_1 = [d_1, d_2, ..., d_{50}]^T$, $D_2 = [d_{51}, d_{52}, ..., d_{100}]^T$, ..., $D_{20} = [d_{951}, d_{952}, ..., d_{1000}]^T$.

(II). Calculation of Gradient Vector

$\frac{\partial f}{\partial D_1}(D|_p), ..., \frac{\partial f}{\partial D_i}(D|_p), ..., \frac{\partial f}{\partial D_{20}}(D|_p)$ are calculated in the next twenty one half line periods after p^{th} half line period. It is noted that the i^{th} component of the gradient vector can only be calculated in $(i+1)^{th}$ half line period because the current sampling data in the whole half line period is needed for the THD calculation.

In #1 half line period, the diagnostic disturbance Δd is added to every duty cycle in subset D_1. That is

$$D_1' = D_1 + \Delta D = [d_1 + \Delta d, d_2 + \Delta d, ..., d_{50} + \Delta d]^T \qquad (9)$$

where $\Delta D=[\Delta d,\Delta d,....,\Delta d]^T$. At the same time, $D_2,....,D_{19},D_{20}$ remain the same values as that in p^{th} half line period.

In #2 half line period, the first gradient vector component $\frac{\partial f}{\partial D_1}(D|_p)$ is calculated. Also in #2 half line period, the diagnostic disturbance Δd is added to every duty cycle in subset D_2. That is

$$D_2^{'}=D_2+\Delta D=[d_{51}+\Delta d,d_{52}+\Delta d,....,d_{100}+\Delta d]^T \quad (10)$$

At the same time, $D_1,D_3...,D_{19},D_{20}$ remain the same values as that in p^{th} half line period. The second gradient vector component $\frac{\partial f}{\partial D_2}(D|_p)$ is calculated in #3 half line period.

The above steps continue until the #21 half line period, during which 20^{th} gradient vector component $\frac{\partial f}{\partial D_{20}}(D|_p)$ is calculated.

(III). Calculation of the New Duty Cycles

New duty cycle set $D|_{p+1}$ can now be calculated by using equation (7) in $(p+1)^{th}$ half line period.

It should be noted that: First, the total time for an iteration of optimization is $220mS$ ($=10mS\times 22$, 22 half line periods). The Boost PFC circuit should operate in the steady state during this period so as to achieve the optimization algorithm. If the input line voltage or the load is changed during this period, the optimization will be terminated and re-setup until the next steady state. Second, the diagnostic disturbance Δd should be small enough to keep the circuit operating in the steady state and satisfy the approximation condition of (5).

5. CPU Requirement Estimation

The proposed PFC control strategy can significantly reduce the CPU calculation requirement so that the switching frequency is no longer limited by the speed of the DSP. In this section, the required CPU time to implement the proposed control method is estimated.

There are mainly three parts in the time consumption with the new PFC control strategy: (1) data sampling, (2) gradient descent implementation and (3) Fast Fourier Transform (FFT) calculation.

In a typical DSP system, it takes one instruction to activate analog-to-digital conversion, another instruction to address the memory. Therefore, if 128 sample points are needed in one half line period, 256 instruction cycles are required for data sampling.

For the gradient descent algorithm, it is implemented only once in 22 half line periods (referring to section 4.3). Hence, very little CPU time is required for this part.

Based on the above analysis, it is noted that the CPU time for the first and second part is negligible compared with the third part. The FFT calculation takes up the most time in the process [10-11]. The CPU time for FFT is estimated as the following.

For example, the radix-2 FFT algorithm can be used to calculate THD in DSP. It is used to estimate the CPU time requirement in this paper. If we use 128 sample points in half line period, there are 256 points in one line period. Assuming the line frequency is 50Hz, the sample frequency should be 12.8kHz ($=256\times 50$). According to sampling theory, the sampling frequency of 12.8kHz can distinguish the signal at frequency of 6.4kHz ($=12.8kHz/2$). It is noted that 6.4kHz is 128^{th} ($=6.4kHz/50Hz$) harmonic frequency of 50Hz base frequency. Usually, the harmonics with the frequency lower than the 13^{th} contribute the most to THD. Therefore, 256 point radix-2 FFT is good enough to calculate THD in the proposed PFC control strategy.

For N point radix-2 FFT, the required complex multiplications, M_c, and complex additions, A_c, are determined as:

$$M_c=\frac{N}{2}\log_2 N \quad (11)$$

$$A_c=N\log_2 N \quad (12)$$

It is noted that each complex multiplication requires four real multiplications and two real additions, each complex addition requires two real additions. Therefore, for N point radix-2 FFT, the required real multiplications, M_r, and required real additions, A_r, are:

$$M_r=4\times M_c=2N\log_2 N \quad (13)$$

$$A_r=2\times M_c+2\times A_c=3N\log_2 N \quad (14)$$

For 128 sample points in half line period, the point N of radix-2 FFT is 256 ($=2\times 128$). Therefore, the required real multiplication, $M_{r,256}$, and real additions, $A_{r,256}$, are determined as:

$$M_{r,256}=2N\log_2 N|_{N=256}=4096$$

$$A_{r,256}=3N\log_2 N|_{N=256}=6144$$

For a DSP with the hardware multiplier, typically, each multiplication can be achieved by four instruction cycles: (1) two cycles for data addressing for operand of multiplication, (2) one cycle for arithmetic operation and (3) one cycle for the data addressing for the product. Similarly, four instructions are required for each addition. Therefore, the 256 point radix-2 FFT requires 40,960 (=4096*4+6144*4) instruction cycles. Considering data sampling, gradient descent implementation, data processing and other overhead, 20% instruction cycle margin is added. Therefore, the new PFC control strategy can be achieved by no more than 50,000 (40,960*1.2=49,152) instruction cycles. Table 1 shows the required instruction cycles for different sampling points in one half line period.

TABLE 1 Calculations and Instructions Required for Proposed Digital PFC Control Strategy with Radix-2 FFT Algorithm

Sampling Point in Half line Period	Point of Radix-2 FFT	Complex Multiplications	Complex Additions	Real Multiplications	Real Additions	Instruction Cycles Required
N_s	N	Mc	A_c	M_r	A_r	n_I
64	128	448	896	1,792	2,688	21,504
128	256	1,024	2,048	4,096	6,144	49,152
256	512	2,304	4,608	9,216	13,824	82,944
512	1,024	5,120	10,240	20,480	30,720	184,320

For a DSP with 30 MIPS (Million Instructions Per Second) performance, during half line period ($10\,mS$), 300,000 (=30,000,000/100) instructions can be completed. Because about 49,152 instruction cycles (referring Table 1) are required for the situation with 128 sample points in half line period, the speed of the DSP is far beyond enough. For the implementation of the proposed digital strategy, a DSP with 10 MIPS performance is good enough for the 256 point radix-2 FFT. So the cost of the digital controller will be reduced.

It is shown from the above analysis that, in the proposed PFC control strategy, the required CPU time is dependent on the sample frequency, not on the switching frequency. That means, a high switching frequency (e.g., 400KHz) can also be implemented by using a low cost DSP based on the new digital PFC control strategy. Therefore, one of the biggest barriers of digital implementation for PFC control is eliminated.

6. Computer Simulation

The proposed new digital PFC control method is simulated by using Matlab. The design parameters of the Boost circuit are: V_{in}=220V(RMS), V_O=400V, L=1mH, C=1100uF, $R_O=160\,\Omega$, $R_L=0.05\,\Omega$, $R_{on}=0.27\,\Omega$, $f_{sw}=100kHz$, $f_{line}=50Hz$. Here, R_L is the winding resistor of the inductor and R_{on} is the on resistance of the MOSFET. The output power is 1000 W. The switching frequency is 100kHz.

6.1 Simulation Algorithm

The simulation program flow chart is shown in Fig.5. The program includes five modules: parameter setting up module, initialization module, calculation module for gradient vector component, optimization module and evaluation module. The later three modules perform the optimization algorithm.

In the first module, the Boost circuit parameters and other parameters of the PFC control algorithm, such as Δd, number of the gradient vector dimension, etc., are set up. All of these parameters will not be changed in the simulation once they have been determined in this module. In the second module, the duty cycle set is initialized. In this algorithm, the initialized values of the duty cycles are determined by (15)

$$D=1-\frac{V_{rec}}{V_{DC}^*}=1-\frac{V_{pk}\,|\sin(2\pi ft)|}{V_{DC}^*} \qquad (15)$$

where V_{DC}^* is the reference output voltage, V_{rec} is the rectified input voltage. The Boost circuit keeps working with this duty cycle set until it reaches the steady state. In the third module, the gradient vector components are calculated. It implements the same process as that shown in Fig.4. In the fourth module, the gradient descent is calculated. The optimized duty cycle set $D|_{p+1}$ is calculated by (7). In the fifth module, the optimization will be evaluated. If the power factor is larger than the specification, the optimization is terminated and the duty cycle set is just "copied" from that in the previous half line period.

The output voltage is controlled by the closed loop. The proportional coefficient of PI regulator is 0.01 and integral coefficient is 0.3.

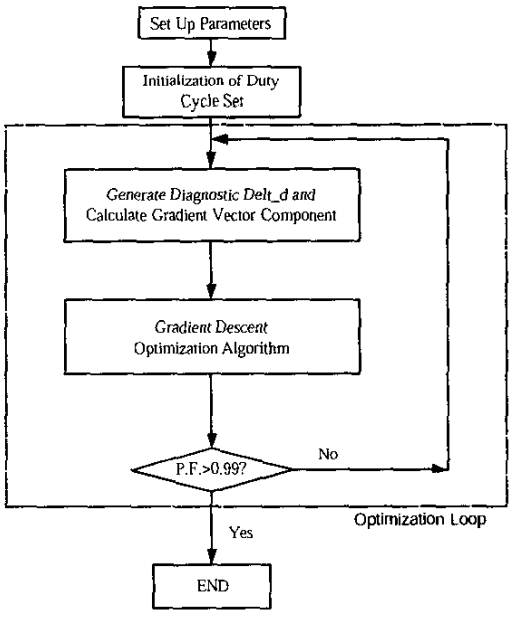


Fig.5 The simulation program flow chart

6.2 Simulation Results

The simulation results are shown in Fig.6-9. Fig.6 is the THD of the input current after every optimization. The THD before the optimization is 31.25%. After the first optimization iteration, the THD is reduced to 28.90%. The THD is reduced to 7.29% after the 13th optimization.

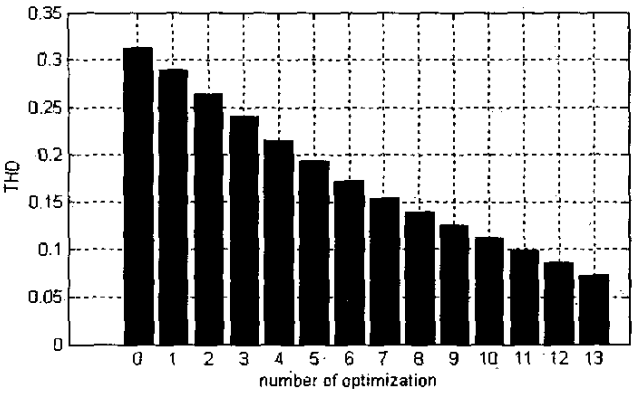


Fig.6 THD of the input current after every optimization

The power factor (PF) is 0.9545 before the optimization, as shown in Fig.7. It increases to 0.9607 after the first optimization. After the 13th optimization, PF becomes 0.9974. The PF is improved from 0.9545 to 0.9974.

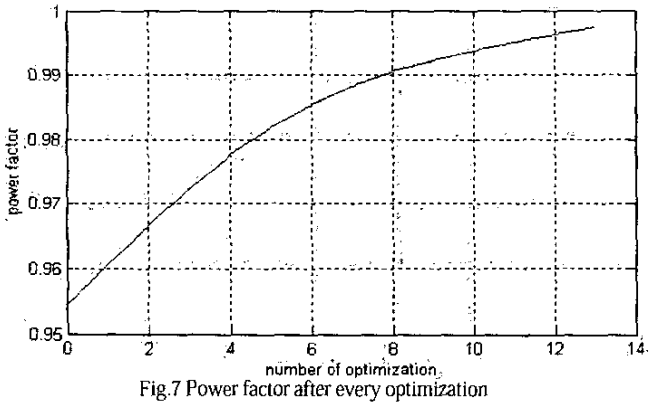
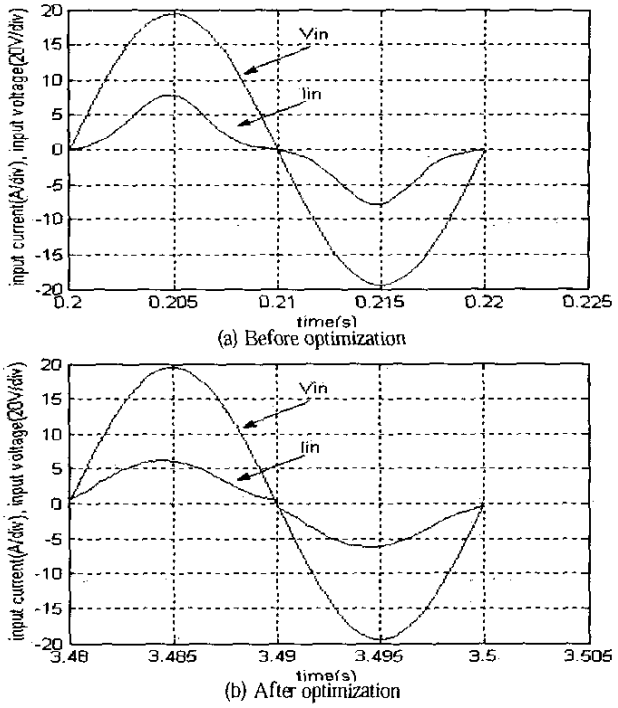


Fig.7 Power factor after every optimization

Fig.8(a) and (b) are the input current and voltage waveforms before and after the 13th optimization. The waveforms in Fig.8 (a) and (b) show that the input current waveform is improved significantly after the optimization.

Harmonic analysis is carried out to verify the proposed method. Fig.9 (a) and (b) are the harmonic components in the line current before and after the 13th optimization. The third harmonic is reduced from 1.83A to 0.38A by using the proposed PFC control method.

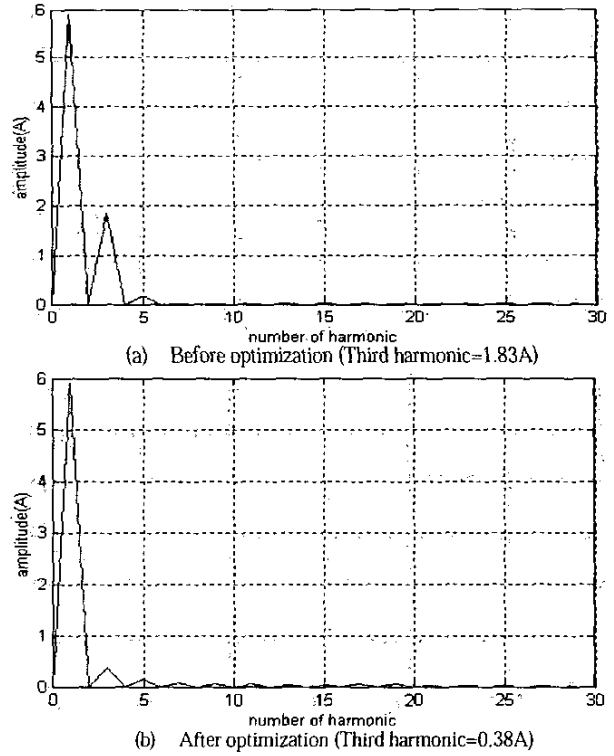
The simulation results show that the proposed optimization algorithm is valid in the digital PFC control strategy.



(a) Before optimization

(b) After optimization

Fig.8 Input current and voltage waveforms



(a) Before optimization (Third harmonic=1.83A)

(b) After optimization (Third harmonic=0.38A)

Fig.9 Harmonic components of the input current

7. Conclusion

In this paper, the conventional digital control methods for PFC are reviewed. One big problem of the conventional methods is that the switching frequency is limited by the speed of the DSP. A new digital PFC control strategy is proposed in this paper. The basic idea of the new digital PFC control strategy is that, based on the input current and duty cycles in the previous line periods, an optimization algorithm is used to generate all of the required duty cycles for one half line period at one time in advance. THD of the input current is determined to be the objective function and gradient descent is used to reduce THD and achieve unity power factor in the new digital PFC control strategy.

The implementation of the new digital PFC control strategy is discussed. The CPU requirement is estimated based on radix-2 FFT. One significant characteristic of the proposed method is that there is no direct relation between the switching frequency and the speed of the digital controller. Therefore, the switching frequency limitation of the digital controlled PFC system is essentially eliminated. That means a high switching frequency can be implemented by using a low cost/low speed DSP based on the new digital PFC control strategy. Computer simulation is performed to verify the feasibility of the proposed algorithm. Simulation results show that harmonic currents, particularly the third harmonic, are reduced significantly and unity power factor can be achieved. The basic principle of the proposed control strategy opens a new direction for the research of digital control of PFC.

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