A Zero Voltage Switching Asymmetrical Half-Bridge DC/DC Converter With Unbalanced Secondary Windings For Improved Bandwidth

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Abstract – **This paper presents a modified PWM half-bridge DC/DC converter that can achieve zero voltage switching (ZVS) and can operate under current or voltage mode control. The proposed topology operates with complementary-control (asymmetrical duty cycle) and utilizes unbalanced transformer secondary windings and a low output inductance value to achieve an improved bandwidth and load transient response compared to the active clamp forward converter. Self-driven synchronous rectifiers are used to increase efficiency. The operation of the converter is discussed, along with a comparison to the balanced secondary topology and the active clamp forward converter. A method is presented to eliminate synchronous rectifier gate drive voltage stress caused by asymmetrically unbalanced gate drive waveforms. In addition, an averaged switch large signal model is presented for the converter. Simulation results are presented for a converter operating at 400kHz, with a 48VDC nominal input and a 5VDC/5A output.**

I. Introduction

Many new electronic devices exhibit load characteristics with very fast transients. Consequently, the power supply industry has been forced to develop power modules that can exhibit these fast transient response characteristics at high efficiency.

The motivation for this paper came from this need to design and analyze a DC/DC converter with improved load transient response and efficiency. The objective of this paper is to present a high frequency, pulse-width-modulated (PWM) DC/DC converter that can achieve zero-voltage-switching (ZVS) along with high efficiency and improved load transient characteristics by using unbalanced secondary winding turns.

Complementary-driven topologies, including the active clamp forward (ACF) [1] and the asymmetrical half-bridge (AHB) topology, are two families of topologies that have been demonstrated as candidates to achieve these goals [2]-[8]. Self-driven synchronous rectifiers (SRs) can be used for either family to improve efficiency [3] and [4]. The AHB, also known as the half-bridge with complementary control, has many advantages over the ACF [5] and [8]:

1) A smaller output filter can be used due to the centre-tapped full-wave rectifier, allowing greater bandwidth to be achieved. In addition, the full-wave rectifier's secondary turns can be unbalanced to minimize the rectified voltage ripple.
2) ZVS can be attained easier because the reflected load current in the primary is bi-directional.
3) Switch voltage stress is clamped to the input voltage, allowing the use of MOSFETS with lower ratings to achieve higher efficiency.
4) The lower transformer primary voltage allows a smaller number of primary turns, resulting in lower leakage inductance, which reduces rectifier body diode commutation loss.
5) Utilizing peak current-programmed control does not require slope compensation due to the duty cycle (D) restriction of $0<D<0.5$.

The relative disadvantages are fewer and are of less significance. They include the following:

1) The transformer requires an additional secondary winding for the full-wave rectifier.
2) The duty cycle restriction of $0<D<0.5$, or $0.5<D<1$, limits the available duty cycle range.
3) Operation is required far from $D=0.5$ to compensate for input changes and load transients. This causes rectifier voltage stress and the SR gate drive waveforms to be more asymmetrically unbalanced.

In Section II, the operating principles of the AHB with self-driven SRs are outlined as in [3] and [4] and the key ideas are re-presented. The benefits of using the unbalanced secondary windings are explained in detail to demonstrate how the bandwidth can be improved. In addition, the principles of ZVS operation for the AHB have been documented [2],[4],[5] and [6] and the key ideas are re-presented.

A method is presented in Section III to eliminate the problems caused by the asymmetrically unbalanced self-driven SR gate drive waveforms.

Only the small signal, voltage mode control model [7],[8] has been developed for the AHB. There is not even a unified model that can predict both the steady-state and dynamic characteristics of the current mode controlled AHB. A unified large signal model [9] is derived in Section IV for the current mode controlled AHB. The model can be used to determine the large signal characteristics and it can be used to derive the steady-state and small signal models of the converter.

Section V includes simulation results. The bandwidth of the AHB is determined for a 48V/5V, 25W converter using the dynamic analysis tools from Cadence's Analog Workbench and Power Design Tool's Simplis. A comparison is presented between the balanced and unbalanced secondary rectified voltage and output filter current waveforms. In addition, the model of Section IV is simulated to demonstrate its accurate tracking of dynamics compared to the AHB using the current mode control circuit in [10] without slope compensation.

Section VI is the conclusion.

II. Operating Principles

The unbalanced AHB is shown in Fig. 1. It includes self-driven SRs to improve efficiency for low output voltage applications. It is proposed that this topology exhibits a significantly improved bandwidth by utilizing different secondary turns, N_{S1} and N_{S2} and can achieve high efficiency due to its inherent ZVS capability and self-driven SRs.

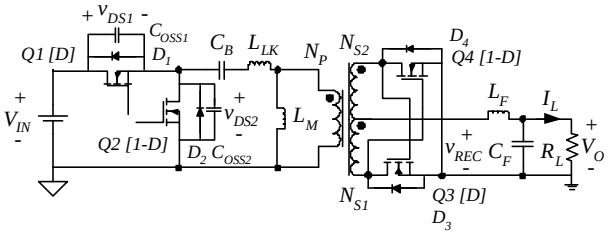

Fig. 1 AHB with self-driven SR and unbalanced secondary windings

The unbalanced secondary windings, N_{S1} and N_{S2} can significantly reduce the secondary side ripple of the rectified voltage, v_{REC} for nominal conditions including the nominal duty cycle, D, nominal input voltage, V_{IN} and nominal load current I_L. This reduces the output inductor current ripple and as a result, bandwidth can be improved because the output filter pole due to filter inductance, L_F increases in frequency by decreasing L_F.

A. Basic Operation

To illustrate the basic operation of the topology, the following assumptions have been made:

1) The MOSFETS are ideal with no conduction voltage drops, no switching loss and no switching time
2) The blocking capacitance, C_B is large enough so that the voltage across it is constant.
3) There is no dead-time between MOSFET on-off state transitions.

Using the above assumptions, there are two states of operation of the converter: 1) T_{on} *[D]*: Q1 and Q3 on, Q2 and Q4 off, and 2) T_{off} *[1-D]*: Q2 and Q4 on, Q1 and Q3 off. The corresponding waveforms are shown in Fig. 2.

B. Inductor Ripple Current Characteristics

Fig. 3 shows the v_{REC} waveform for the unbalanced AHB, and the waveforms for the balanced AHB and ACF. It is noted that v_{RECON} and v_{RECOFF} are always larger than zero and that by selecting N_{S1} and N_{S2} appropriately, the value of the difference between v_{RECON} and v_{RECOFF}, Δv_{REC}, can be made very small.

The unbalanced AHB has a significantly reduced $\Delta v_{REC.}$ During T_{on}, v_{REC} is given by v_{RECON} (1) and during T_{off}, v_{REC} is given by v_{RECOFF} (2).

$$v_{RECON} = \frac{N_{S1}}{N_P}(1-D)V_{IN} \tag{1}$$

$$v_{RECOFF} = \frac{N_{S2}}{N_P}DV_{IN} \tag{2}$$

For the balanced AHB, v_{RECON} and v_{RECOFF} are as given by (1) and (2), where N_{S1}=N_{S2}, however for the ACF, v_{RECON} is given by (3) and v_{RECOFF} is zero.

$$v_{RECON} = \frac{N_S}{N_P}V_{IN} \tag{3}$$

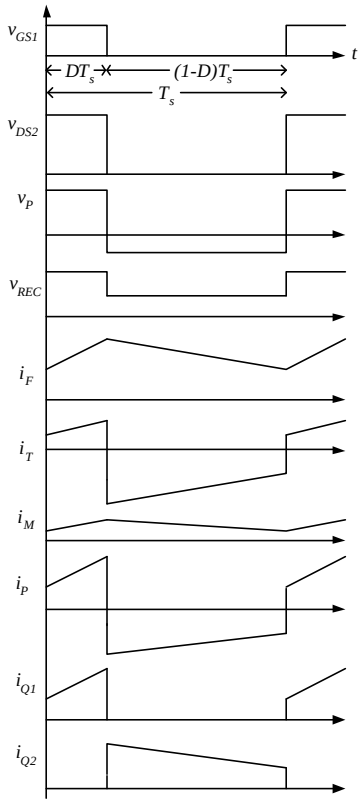

Fig. 2: AHB waveforms

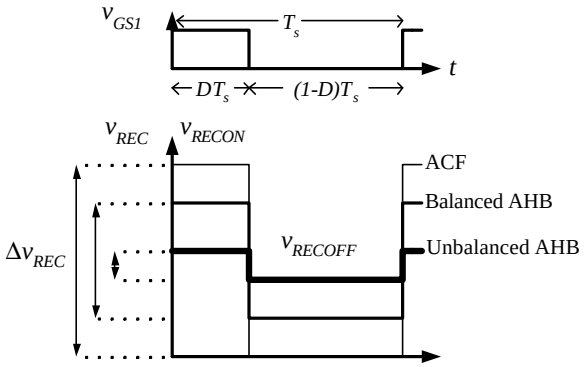

Fig. 3 Primary switch gate drive waveform, v_{GS1} and secondary side rectified voltage, v_{REC}

The small Δv_{REC} of the unbalanced AHB reduces the output filter inductor ripple current, Δi_F. The equations for inductor ripple current and output voltage as a function of input voltage are given below by (4)-(11) for the unbalanced AHB, balanced AHB and forward topologies.

Unbalanced AHB:

$$\Delta i_F = \left| \frac{T_s}{L} D(1-D)\left(\frac{N_{S1}}{N_P}(1-D) - \frac{N_{S2}}{N_P}D \right) V_{IN} \right| \tag{4}$$

$$D = \frac{1}{2} - \frac{1}{2}\sqrt{1 - 4\frac{V_O}{V_{IN}}\frac{N_P}{N_{S1}+N_{S2}}} \tag{5}$$

$$V_O = D(1-D)\left[\frac{N_{S1}}{N_P} + \frac{N_{S2}}{N_P}\right]V_{IN} \quad (6)$$

Balanced AHB:

$$\Delta i_F = \left|\frac{T_s}{L}D(1-D)(1-2D)\frac{N_S}{N_P}V_{IN}\right| \quad (7)$$

$$D = \frac{1}{2} - \frac{1}{2}\sqrt{1-2\frac{V_O}{V_{IN}}\frac{N_P}{N_S}} \quad (8)$$

$$V_O = 2D\frac{N_S}{N_P}(1-D)V_{IN} \quad (9)$$

ACF:

$$\Delta i_F = \left|\frac{T_s}{L}D(1-D)\frac{N_S}{N_P}V_{IN}\right| \quad (10)$$

$$V_O = D\frac{N_S}{N_P}V_{IN} \quad (11)$$

It can be observed from (3) that it is possible to achieve zero inductor ripple current for the Unbalanced AHB if (12) is satisfied.

$$\frac{N_{S1}}{N_P}(1-D) = \frac{N_{S2}}{N_P}D \quad (12)$$

However, we can only achieve zero inductor ripple current for the Balanced AHB if D=0.5 which is an impractical nominal operating point for reasons mentioned in Section I and the ACF cannot achieve zero inductor ripple current for any practical nominal duty cycle.

The benefits of using the unbalanced AHB topology are further illustrated in Fig. 4, which shows the relationship between filter inductor ripple current and input voltage for the three circuits. In all three cases, the output voltage, V_O, is 5V and the filter inductance, L_F, is 1µH. The transformer turns are as follows: 1) ACF: N_P=5, N_S=2, 2) Balanced AHB: N_P=5, N_S=2, and 3) Unbalanced AHB: N_P=6, N_{S1}=1 and N_{S2}=3.

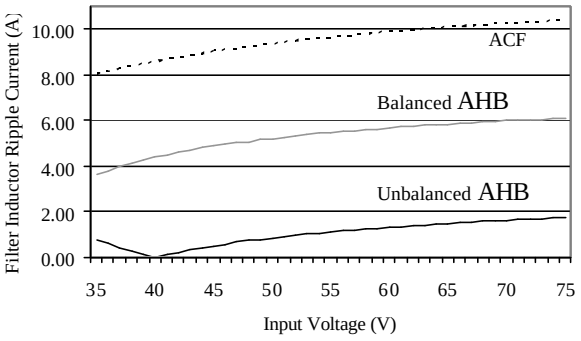

Fig. 4 Output inductor ripple current vs. input voltage for the unbalanced AHB, balanced AHB and ACF

It is noted that the ripple current is zero at an input voltage of 40V and the worst case inductor ripple current of the unbalanced AHB is 1.8A, which is 3 times less than that of the balanced AHB (6A) and almost 6 times less than that of the ACF (10.5A). This allows the use of a much smaller output filter inductor to improve the load transient response time for similar output ripple requirements, switching frequency and output filter capacitance.

C. Principles of ZVS Operation

In the above analysis, dead-time between *Q1* and *Q2* has not been included. In order to achieve ZVS dead-time is introduced during the switching transitions for both MOSFETs.

During the dead-time between the turn-off of *Q1* and turn-on of *Q2*, the transformer leakage inductance discharges the voltage v_{DS2} across C_{OSS2} and charges the voltage v_{DS1} across C_{OSS1}. During the dead-time between the turn-off of *Q2* and turn-on of *Q1*, the transformer leakage inductance discharges the voltage v_{DS1} across C_{OSS1} and charges the voltage v_{DS2} across C_{OSS2}. If the energy in the leakage inductance is greater than the energy in C_{OSS1} and C_{OSS2}, ZVS can be achieved at turn-on.

III. Self-Driven Synchronous Rectifier Gate Drive Implementation

The implementation of the proposed topology with unbalanced secondary windings and self-driven SRs utilizing auxiliary gate drive windings and an auxiliary turn-off circuit for *Q4* is provided in Fig. 5. The auxiliary circuit can be used for either SR, however it will be demonstrated that it is usually required for *Q4* and is not required for *Q3*.

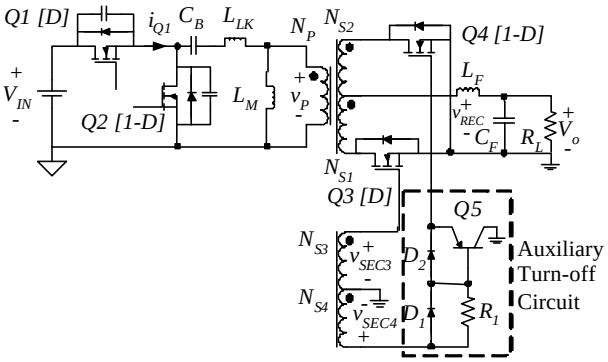

Fig. 5 Unbalanced AHB with SDSR and auxiliary secondary windings

Equations (13)-(16) give the SR gate drive voltages during T_{on} and T_{off}. The gate voltages, v_{Q3ON} and v_{Q4ON} must be sufficiently positive enough (typically>5V) to drive the SRs during T_{on}, but v_{Q3OFF} and v_{Q4OFF} cannot be too negative (typically>-20V) during T_{off}, or the MOSFETs will be damaged.

$$v_{Q3ON} = \frac{N_{S3}}{N_P}(1-D)V_{IN} \quad (13)$$

$$v_{Q3OFF} = -\frac{N_{S3}}{N_P}DV_{IN} \quad (14)$$

$$v_{Q4ON} = \frac{N_{S4}}{N_P}DV_{IN} \quad (15)$$

$$v_{Q3OFF} = -\frac{N_{S4}}{N_P}(1-D)V_{IN} \quad (16)$$

The gate drive waveforms are illustrated in Fig. 6a. If appropriate turns, N_{S3} is selected for *Q3* to be turned-on and if D<0.5, then there cannot be a negative gate voltage stress

problem for *Q3*. However, without the auxiliary circuit, the *Q4* gate voltage, v_{GSR2} is equal to v_{SEC4}, which is large negative during T_{on}. Using the auxiliary circuit, the *Q4* gate voltage waveform, v_{GSR2} is illustrated in Fig. 6b. The auxiliary turn-off circuit performs two functions: 1) it blocks the negative SR gate voltage, and 2) it provides a quick turn-off of *Q4* by providing a path for the *Q4* gate current to discharge.

The auxiliary turn-off circuit of Fig. 5 provides a simple method of eliminating one of the drawbacks of the AHB mentioned in the introduction.

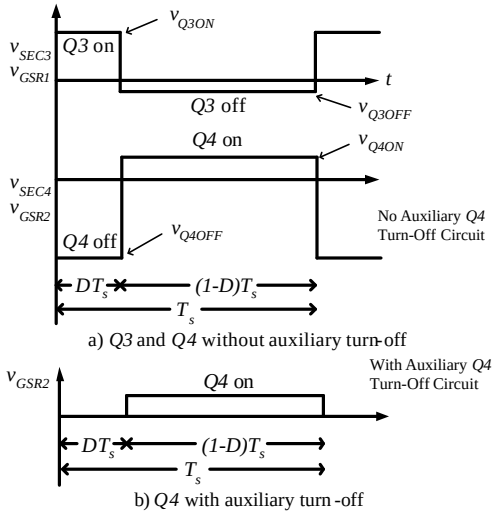

Fig. 6 SR gate drive waveforms

IV. Modeling the Asymmetrical Half-Bridge Under Current Mode Control

Current mode control (CMC) is widely used because of its advantages over voltage mode control, such as fast response, improved damping and over current protection. Unfortunately, because there are two feedback loops in current mode control, the analysis of the dynamic characteristics of current mode converters is difficult.

A large signal model for the current mode controlled AHB is presented using the averaged circuit model. This technique uses the state-space average technique and takes the form of the averaged circuit model that has the same topology as that of the switching converter. Once the large signal model is established, the large signal characteristics can be analyzed using the differential equations, or by using a circuit simulation software package, eg. SPICE. The large signal characteristics can be obtained by using the AC analysis tools in SPICE. In addition, the steady-state and small signal models can be easily derived from the large signal model.

It is proposed that all switches that conduct during T_{on} (*Q1* and *Q3*) are modeled by controlled current sources equal to the average current through the switch during one switching period and all switches that conduct during T_{off} (*Q2* and *Q4*) are modeled by controlled voltage sources equal to the average voltage across the switch during one switching period.

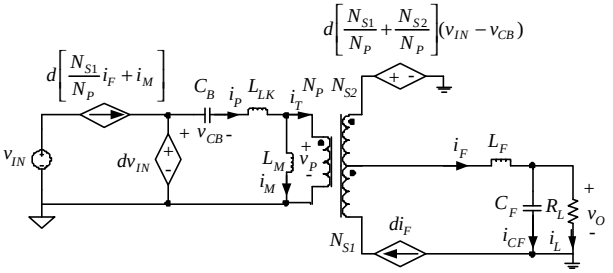

Fig. 7 Large signal current mode controlled model of the unbalanced AHB

Fig. 8 gives the detailed relationship between the control signal, i_C and the *Q1* switch current, $i_{Q1}(t)$, which is used to derive the duty ratio. In Fig. 8, $i_{Q1}(t)$ denotes the instantaneous switch current and i_{Q1} denotes the state-space averaged switch current during the interval dT_s. The state-spaced averaged switch current passes through the midpoint of the actual switch current, so i_{Q1} is derived from the geometry (17).

$$i_{Q1} = i_C - 0.5 m_1 dT_s \tag{17}$$

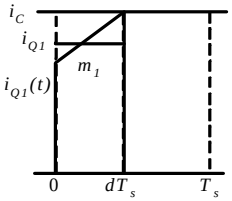

Fig. 8 Detailed waveforms between switch current, i_{Q1} and control signal, i_C for current mode control

Since the primary current, i_P is equal to i_{Q1} during T_{on}, we can replace i_{Q1} in (17) with i_P. In current mode control, the duty ratio, d is not the direct control variable, but it can be expressed as follows:

$$d = \frac{i_C - i_P}{0.5 m_1 T_s} \tag{18}$$

Equation (18) holds true for all switching converters. For the unbalanced AHB converter, it is expressed as:

$$d = \frac{i_C - \left(\frac{N_{S1}}{N_P} i_F - i_M\right)}{0.5 m_1 T_s} \tag{19}$$

where m_1 is the primary current slope. It can be expressed as:

$$m_1 = \frac{\Delta i_M}{dT_s} + \frac{N_{S1}}{N_P}\frac{\Delta i_F}{dT_s} \tag{20}$$

which reduces to:

$$m_1 = \frac{(v_{IN} - v_{CB})}{L_M} + \frac{N_{S1}}{N_P}\frac{\left[\frac{N_{S1}}{N_P}(v_{IN} - v_{CB}) - v_o\right]}{L_F} \tag{21}$$

It should be noted that the averaged sources are not independent, but are controlled by other circuit variables, such as i_C, i_F, v_{IN} and so forth. Furthermore, since all the circuit variables are the state-spaced averaged value and because no small signal assumption is imposed during the

derivation, the model given in Fig. 7 is a large signal model for the current mode controlled AHB. Simulation results have been included to demonstrate the accuracy of the model in the next section.

V. Simulation Results

A. Open-Loop Simulation Results

The topology of Fig. 5 was simulated using Simplis for the balanced and unbalanced configurations. Fig. 9 illustrates the transformer secondary side rectified voltage, v_{REC} and the output filter inductor current, i_F for the unbalanced AHB with N_P=6, N_{S1}=1, N_{S2}=3, L_F=1µH, V_{IN}=48 and V_O=5V. Fig. 10 illustrates the transformer secondary side rectified voltage, v_{REC} and the output filter inductor current, i_F for the balanced AHB with N_P=5, N_s=2 and L_F=1µH. The downward spikes towards zero for v_{REC} are due to the commutation of both body diodes of the secondary side SRs. If we disregard these spikes, we observe that the unbalanced AHB has a Δv_{REC} of about 600mV and the balanced AHB has a Δv_{REC} of about 12V. In addition, the unbalanced AHB has a Δi_F of 800mA and the balanced AHB has a Δi_F of 9A.

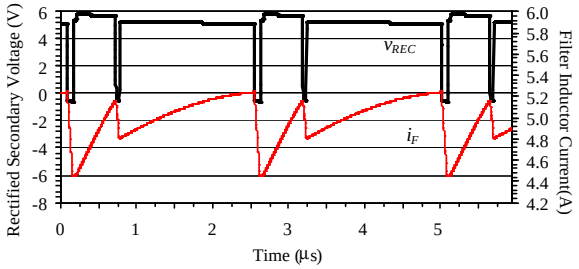

Fig. 9 Transformer secondary side rectified voltage, v_{REC} and output filter inductor ripple current, i_F for unbalanced AHB

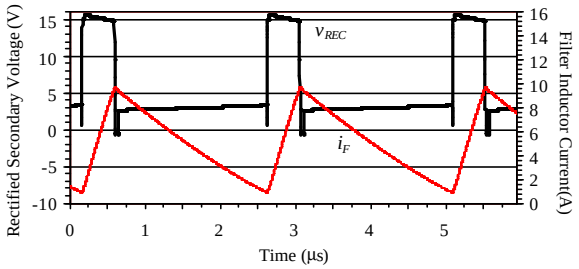

Fig. 10 Transformer secondary side rectified voltage, v_{REC} and output filter inductor ripple current, i_F for balanced AHB

B. Current Mode Control Dynamic Simulation Results

We have assumed that we can achieve a greater bandwidth by decreasing the output filter inductance. The validity of this assumption is demonstrated by simulation of the current mode controlled unbalanced AHB without voltage feedback compensation (open-loop). The network analysis tools of Simplis were used to obtain the curves of Fig. 11. It is clear that for a given magnitude and for frequencies greater than approximately 30kHz, the topology with the 1µH output filter inductor has a much wider bandwidth than that with the 10µH inductor.

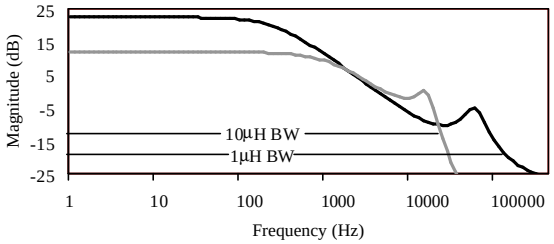

Fig. 11 Current mode control bandwidth comparison

C. Closed-Loop Dynamic Simulation Results

Closed-loop simulation results were obtained for the unbalanced AHB using Simplis. The following circuit parameters and components were used: 1) *Q1-Q4*: IRF540, 2) Diodes: ideal (0.7V drop), 3) *Q5*: 2N3906, 4) C_B=9.4µF and L_M=25µH, 5) L_{LK}=150nH, 6) C_F=40µF and L_F=1µH. The feedback path was isolated using a TL431 voltage reference and a 4N25 opto-coupler. The loop gain was determined using the frequency analysis tools. A bandwidth of 75kHz was achieved at a phase margin of 57° (Fig. 12) for 5A of load current. Time domain transient response results are given for the output voltage in Fig. 13 for a 4% step load change from 5A to 5.2A. The rise time to reach the vicinity of its final set point is approximately 10µs.

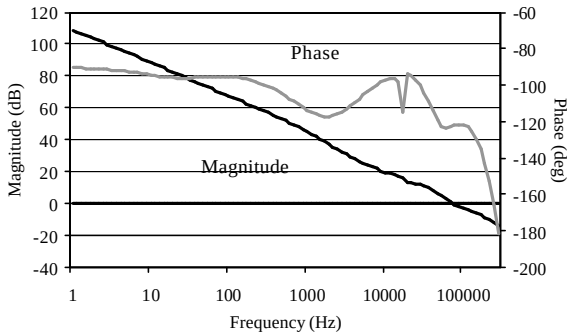

Fig. 12 AHB magnitude and phase loop response

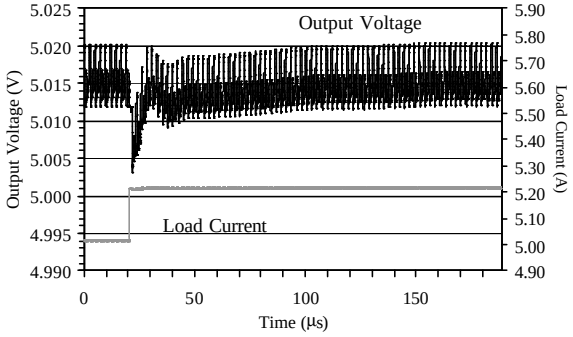

Fig. 13 Closed-loop AHB output voltage transient for 200mA step load change

D. Averaged Model Simulation Results

The averaged AHB model of Fig. 7 was simulated using SPICE and compared to the current mode controlled

AHB without voltage feedback or compensation (open-loop) circuit using Simplis. The MOSFETS used did not include gate capacitance, so no dead-time was included between the switching transitions. All other circuit parameters used were the same as in sub-section A above for the unbalanced AHB. Results are included for a 5% step in control current, i_C (Fig. 14), a 5% step in input voltage, v_{IN} (Fig. 15) and a 5% step in load current, i_L (Fig. 16). It is noted that there is good agreement during the transient period between the model and the open-loop current mode controlled AHB.

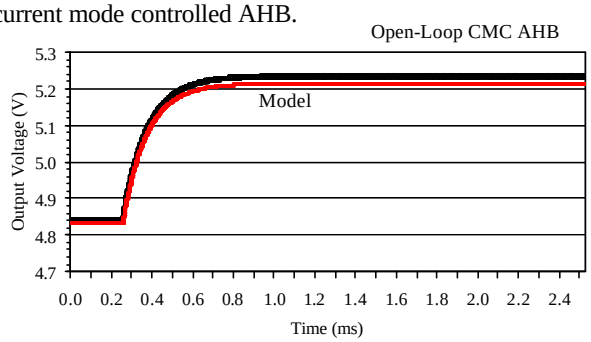

Fig. 14 Output voltage transient for a step in i_C

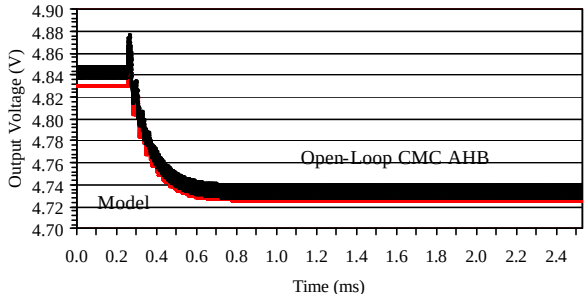

Fig. 15 Output voltage transient for a step in v_{IN}

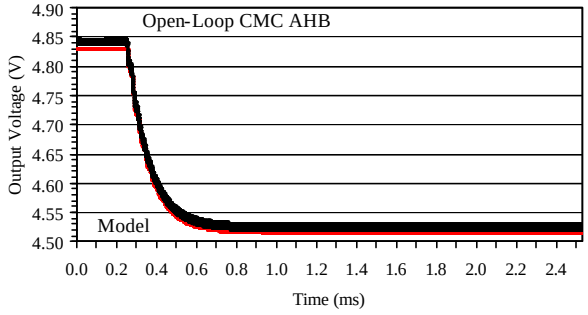

Fig. 16 Output voltage transient for a step in i_L

VI. Conclusion

An asymmetrical half-bridge topology that can achieve zero voltage switching was presented in this paper. Unbalanced secondary windings were used to reduce the secondary rectified voltage and output filter inductor ripple current. This topology achieves a very high loop bandwidth, compared to the active clamp forward topology, because the system pole due to the output filter inductor can be moved to higher frequencies.

Self-driven synchronous rectifiers have been used, which improves efficiency in comparison to conventional diode rectifiers for low output voltage applications. A simple auxiliary circuit has been presented that can be used to drive synchronous rectifiers for any self-driven complementary control topology and eliminate problematic gate voltage stresses.

A large signal current mode control model of the asymmetrical half-bridge has been presented that uses the same topology as the switching topology, but uses averaged dependent sources in place of the switches. The steady-state and small signal models can be easily derived from the large signal model.

Simulation results have been presented for the open and closed-loop asymmetrical half-bridge with unbalanced secondary windings and the unified current mode control model. A bandwidth, of 75kHz at a phase margin of 57° was achieved for the closed-loop circuit. The open-loop simulation results were used to demonstrate that the output filter inductor ripple current was reduced by over 90% with the unbalanced secondary windings compared to balanced secondary windings. The averaged current mode control model results accurately tracked those of the switching circuit for 5% changes in the control variable, input voltage and load current.

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