A New Predictive Control Strategy for Power Factor Correction

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***Abstract*—A new predictive control strategy for PFC is presented. Its basic idea is that all of the duty cycles required to achieve unity power factor in a half line period are generated in advance by using a predictive algorithm. Based on the average output voltage in the previous half line period, the duty cycles in the current half line period can be calculated by the predictive algorithm, which is derived from the differential equations of Boost topology. An optimization process is incorporated with the predictive algorithm to fine tune the parameter of model for the purpose of further reducing the harmonic current. Benefited from the proposed digital control strategy, the switching frequency of the PFC does not directly depend on the processing speed of the DSP. Simulation results show that the proposed strategy works well and unity power factor can be achieved with wide input voltage and load current variation range.**

Keywords-predictive algorithm; digital control; power factor correction; optimization

I. INTRODUCTION

Power Factor Correction (PFC) is necessary for AC-to-DC switched mode power supply in order to comply with the requirements of international standards, such as IEC-1000-3-2 and IEEE-519. PFC can reduce the harmonics in the line current, increase the efficiency and capacity of the power system, and also save the bill of customers. In order to achieve unity power factor in the switched mode power supply, many control methods are explored, including average current control [1], peak current control, hysteretic control, nonlinear carrier control, etc.. All of these control methods had been implemented by the analog circuits. Among these PFC control methods, average current mode control is the most popular. Several commercial ICs, such as UC3854/3855 and ML4824 are available for the PFC applications.

With the development of the digital technique, more and more control algorithms can be implemented in power electronics by the digital chips: microprocessors or digital signal processors (DSP). One reason is that the digital control can implement advanced and complicated algorithm. Another reason is that digital control has many advantages over analog control, including programmability, adaptability, less part count, less susceptibility to environmental variations, and more immunity to the input voltage distortion, etc.. In addition, it is possible to achieve higher performance in digital implementation than that in analog implementation with the same cost. So it is necessary to explore digital control techniques for PFC application.

Digital controlled PFC implementations have been explored by many researchers all over the world. Basically, most of the digital implementations for PFC are based on average current mode control. Some works have been done to make the digital control a competitive option in PFC implementation as compared with analog control. Unfortunately, all of the existing control technique cannot take full advantages of the DSP and the switching frequency of the converter is limited by the speed of the DSP.

A new predictive control strategy suitable for digital implementation of PFC is proposed in this paper. The basic idea of the proposed digital control PFC algorithm is that all of the duty cycles required to achieve unity power factor in a half line period are calculated in advance by using a predictive algorithm. The proposed PFC control strategy is based on the prediction, not feedback, to achieve power factor correction. Using the proposed method, the switching frequency of the PFC does not directly depend on the processing speed of the digital controller. Therefore a relatively low performance/low cost DSP or microprocessor can be used to realize digital control PFC system operating at high switching frequency.

In this paper, the existing digital control methods for PFC are reviewed and their problems are highlighted in section II. The principle of the new predictive control strategy for digital PFC implementation is presented in section III. The further improvement with optimization of control parameter is described in detail in section IV. The required CPU time to implement the proposed PFC control algorithm is estimated in section V. In section VI, the advantages of the proposed PFC control strategy are summarized. The simulation results are presented in section VII. The conclusion is drawn in the last section.

II. PROBLEMS OF THE CONVENTIONAL DIGITAL PFC CONTROL

The switching frequency is limited in the conventional digital controlled PFC system because of the sampling delay and the necessary processing time. Average current control,

which is one of the main conventional analog control strategies, as shown in Fig.1, is used in digital controlled PFC [2-5]. In Fig.1, the average inductor current i_L is forced to follow the reference current i_{ref}, which is proportional to the rectified voltage, so that unity power factor is achieved. In the average current control, DSP or microprocessor is used to calculate the duty cycle for the switch S in every switching cycle T_s to achieve PFC based on the feedback current i_L and the reference current i_{ref}. In [6], single sampling in single period method (SSSP) is adopted and the 50kHz switching signal is controlled by the DSP (TMS320F240, 20MHz). The digital average current control method was implemented in these PFC applications. The whole process in a digital controlled PFC based on average current control include output voltage sampling, voltage error calculation, voltage PI regulation, reference current generation, current error calculation, current PI regulation and duty cycle generation. It is roughly estimated that 11 arithmetic operations are required. In addition, two sampling operations, one operation for addressing the PWM I/O port to output the duty cycle are necessary to achieve PFC implementation. All these operations have to be finished within the t_{on} time of the switch. Because this process is iteratively running in every switching cycle, the high performance DSP is tied up to achieve PFC and the switching frequency is limited. In fact, all these digital implementations are based on average current mode control. Its disadvantage is obvious in the digital implementation although it works well in analog controlled PFC system.

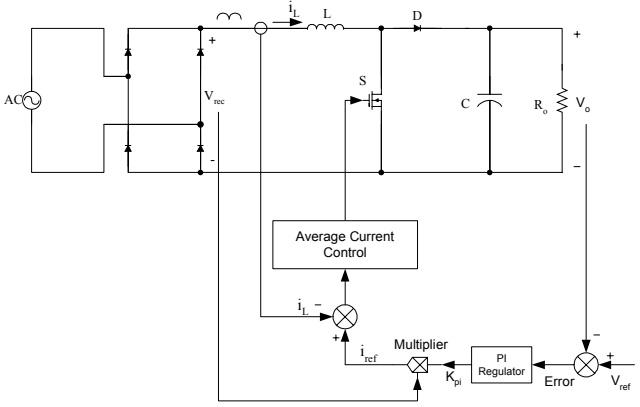


Figure 1. Average current control of the Boost PFC

It is tried to solve the above problems with limited success in several papers. A digital control method is presented [7], in which the duty cycle is only updated once in several switching cycles in order to reduce the calculation time and increase the switching frequency of the PFC converter. The problem is that its harmonics is increased significantly if the duty cycles are not updated in too many switching cycles. It is also difficult to be implemented by the hardware because there is no consideration about the inductance drift due to the current and temperature variation. A PFC control method based on DSP, which consists of two parallel loops, is explored in [8]. However, the duty cycle is still required to be calculated in every switching cycle. So its CPU requirement is no less than that based on the conventional average current control. The same problems as that with conventional average current mode control are still existed in that digital PFC implementation.

Based on above analysis, the first problem of the existing digital control is that the switching frequency is limited due to the sampling, calculation and processing time. Further more, even operating at a relatively low switching frequency, the high performance DSP is still tied up by the PFC stage in switched mode power supply (SMPS). In the digital controlled PFC system, if the switching frequency is 200kHz, one switching cycle is only 5us. If the duty cycle is 0.5 at some time instant, all of the works should be finished by the DSP in 2.5us(5us*0.5). This imposes very high requirement for the speed of the DSP. Second, the higher the switching frequency, the faster the DSP required. So the implementation of the digital control method in the PFC application is limited due to the high cost. Third, even if the fastest DSP is used in the digital controlled PFC system, the switching frequency cannot reach the same level as that in the analog controlled PFC system.

The new predictive control strategy is proposed to solve the above mentioned problems in digital controlled PFC.

III. Principle of the New Predictive PFC Control Strategy

The topology of Boost converter is shown in Fig.2. The proposed predictive PFC algorithm is derived based on the following assumptions:

(1) Boost converter operates at continuous conduction mode

(2) The switching frequency is much higher than the line frequency. So the input voltage V_{in} can be assumed as a constant during one switching cycle

Based on these assumptions, when the switch S is on and/or off, the circuit of Fig.3 (a) and/or (b) are obtained and the inductor voltage can be expressed as (1) and (2), respectively.

$$L\frac{di_L}{dt} = V_{in} \qquad t_k \le t < t_k + d_k T_s \tag{1}$$

$$L\frac{di_L}{dt} = V_{in} - V_o \qquad t_k + d_k T_s \le t < t_{k+1} \tag{2}$$

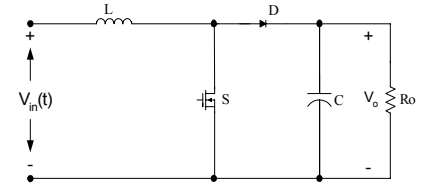
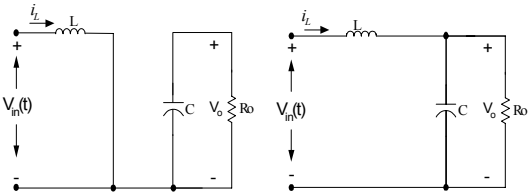


Figure 2. Boost converter topology



(a) switch is on (b) switch is off

Figure 3. Boost converter circuit

The discrete form for the inductor current at the beginning of $(k+1)^{th}$ switch cycle in term of the inductor current at the beginning of k^{th} switching cycle can be derived from (1), (2) as

$$i_L(k+1) = i_L(k) + \frac{V_{in}(k)\cdot T_s}{L} - \frac{V_o(1-d(k))\cdot T_s}{L} \quad (3)$$

Where $d(k)$ and T_s are the duty cycle and switching period. $V_{in}(k)$ is the input voltage in k^{th} switching cycle. $i_L(k)$, $i_L(k+1)$ are the input current at the beginning of k^{th} and $(k+1)^{th}$ switching cycles, respectively.

When PFC is achieved based on Boost circuit, the inductor current should follow the reference current $i_{ref}(k)$, which is proportional to the rectified input voltage, as shown in Fig.4. At the same time, the output voltage should follow the reference voltage V_{ref}. That is

$$V_o = V_{ref} \quad (4)$$

$$i_L(k+1) = i_{ref}(k+1) \quad (5)$$

$$i_L(k) = i_{ref}(k) \quad (6)$$

Substituting (4) (5) (6) into (3), the duty cycle in k^{th} switching period, $d(k)$, can be calculated as

$$d(k) = \frac{V_{ref} - V_{in}(k)}{V_{ref}} + \frac{[i_{ref}(k+1) - i_{ref}(k)]\cdot \frac{L}{T_s}}{V_{ref}} \quad (7)$$

Where i_{ref} is the rectified sinusoidal waveform and its amplitude is determined by the outer voltage loop.

The predictive algorithm (7) can be used to generate the duty cycles and achieve reasonably good result in the implementation of PFC with Boost topology. In order to improve the performance, a more accurate model, as shown in Fig.5, is used to predict the required duty cycles. In this model, the impacts of the inductor winding resistance, R_L, the on resistance of switch, R_{on}, the voltage drop across diode, V_d, and the output voltage ripple, v_{o_ripple}, are considered. The duty cycles can be derived based on the model in Fig.5 as:

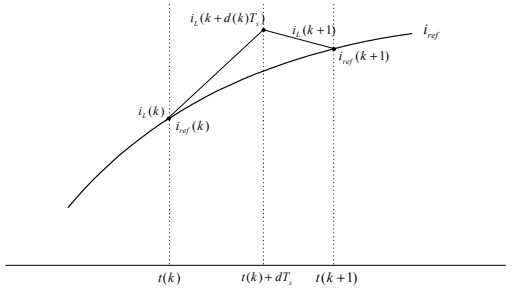


Figure 4. Input current waveform and reference current in one T_s

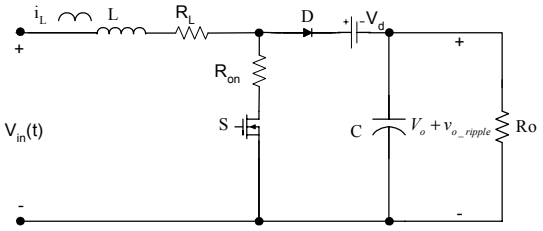


Figure 5. Accurate model of Boost converter

$$d(k) = \frac{(V_{ref} + v_{o\_ripple}(k) + V_d) + R_L i_{ref}(k) - v_{in}(k)}{(V_{ref} + v_{o\_ripple}(k) + V_d) - R_{on} i_{ref}(k)} + \frac{[i_{ref}(k+1) - i_{ref}(k)]\cdot \frac{L}{T_s}}{(V_{ref} + v_{o\_ripple}(k) + V_d) - R_{on} i_{ref}(k)} \quad (8)$$

where , v_{o_ripple} can be estimated as

$$v_{o\_ripple}(k) = -I_o \times \frac{1}{2\omega_{line} C}\sin(2\omega_{line} t_k) \quad (9)$$

(8) is the predictive algorithm, which is used to implement unity power factor in this paper.

It should be noted that there are still two approximations in the predictive algorithm (8). First, the average current in every switching cycle should follow the reference current in Fig.4. Here, it is the instantaneous current $i_L(k)$ and $i_L(k+1)$ that are forced to track the reference current i_{ref}. Second, the instantaneous current $i_L(k)$ is used in (8) to calculate the voltage drop across the inductor resistance and the on resistance of switch. In fact, the average current in one switching cycle should also be used to calculate the voltage drop. Because the inductor current ripple can be neglected, these two approximations are reasonable in the proposed predictive PFC algorithm. This condition of approximation is easier to be satisfied at high load than that at low load. It is verified by the simulation results in the section 7 that the power factor at low load is a little bit less than that at high load because of this approximation.

The digital controlled Boost PFC based on the predictive algorithm is shown in Fig.6. The duty cycles are generated by the predictive algorithm. The input voltage v_{in} is sensed for the predictive algorithm (8). The reference current, i_{ref}, is from the multiplier. Its amplitude is determined by the output of the PID controller in the voltage loop. Its phase and sinusoidal waveform are determined by the zero cross detection and the sine-wave-look-up-table. The output voltage V_o is controlled by the closed loop with a PID regulator. In this digital control system, the feedback signals are V_o and v_{in}. The output is the gate signal for the switch S. Because no current loop is needed in the calculation of the duty cycle, all the duty cycles required to achieve unity power factor in a half line period can be generated in advance with this predictive control strategy.

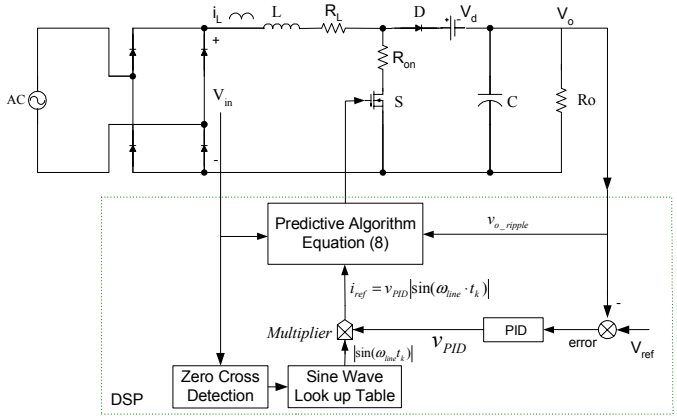


Figure 6. Digital predictive control for Boost PFC preregulator

IV. Further Improvement with Optimization Algorithm

An optimization process is incorporated into the predictive control strategy to further improve the performance of the digital controlled PFC. The parameter to be optimized is selected as the inductance value L in (8). The reason to optimize the value of L is that, among all of the parameters, it has the biggest impact on total harmonic distortion (THD). It is noted that the impacts from the mismatch of the other parameters can also be compensated by adjusting L value in (8). Actually, the optimized value of the inductor in (8) may be a little bit different from the physical value.

The purpose of the optimization process is to achieve the highest power factor by optimizing the inductance value L. In the rectifier cascaded by a PFC circuit, if THD of the line current is minimum, the distortion factor is maximum and the power factor becomes maximum too. Zero THD means unity power factor. Therefore, the THD of input current can be used as the objective function in the optimization algorithm. However, the THD is a complicated nonlinear function of the inductance value L and can only simply expressed as

$$(THD) = f(L) \tag{10}$$

Where (THD) is the Total Harmonic Distortion with the inductance value L. In order to simplify this problem, the other components which affect the THD are not considered in (10). The THD can be minimized by the optimization of the inductance value L based on (10). According to the secant approximation, the gradient of the function (10) can be calculated as

$$\nabla f(L) = \frac{df}{dL} \approx \frac{f(L+\Delta L) - f(L)}{\Delta L} \tag{11}$$

(11) can be achieved easily by a DSP. Once the gradient is known, the gradient descent algorithm can be achieved by

$$L_{update} = L + k\nabla f(L) \tag{12}$$

where k is an arbitrary step size. In this paper, the condition k<0 is required to minimize the objective function THD. Here, L_{update} is the updated inductance value of L and used in the predictive algorithm (8) to minimized the THD. It is not the physical value of the inductor. Gradient descant (12) can be implemented and iterated until the objective function approaches the minimum. So the inductance value of L in the predictive algorithm (8) can be optimized to realize the highest power factor.

The predictive strategy incorporating with the optimization process is shown in Fig.7. The inductor current i_L is sensed and the data of current in a half line period is stored in the memory of DSP. Fast Fourier Transform (FFT) is used to analyze the harmonic component of input current based on the data stored in the memory. Then the gradient descent is implemented by the DSP to achieve the optimized inductance value. The output of the optimization algorithm is the updated inductance value. This value is the input to the next module and used to calculate the duty cycles in the predictive algorithm (8). It should be noted that it is an optimization process, not a current control loop. In the practical application, whether or not the optimization algorithm is adopted is determined by the DSP according the practical situation and the performance requirement.

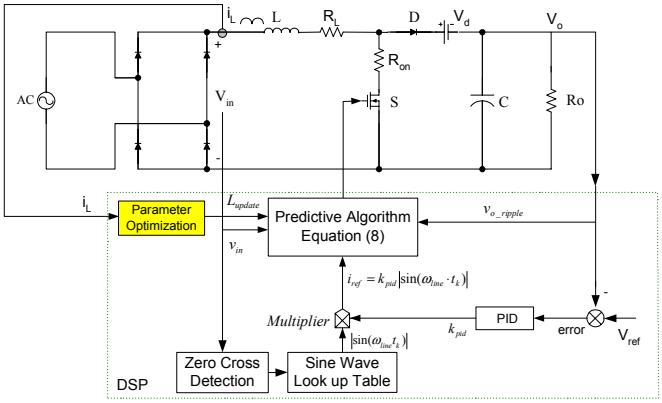


Figure 7. Parameter optimization for inductance value update

V. CPU Requirement Estimation

In this section, the required CPU time to implement the proposed control strategies with and/or without optimization are estimated.

There are mainly three parts in the time consumption for the CPU to achieve the predictive PFC control strategy without optimization: (I) data sampling, (II) PID algorithm implementation, (III) predictive algorithm implementation. If the optimization is incorporated with the predictive algorithm, two more modules are required in the routine: (IV) Fast Fourier Transform (FFT) and (V) gradient descent implementation.

The CPU requirements for these 5 implementation parts are analyzed here. Compared with the part (III) and (IV), the time consumption to achieve (I), (II) and (V) are negligible when the CPU requirement is estimated. First, in a typical DSP system, it takes one instruction to scale the value from analog-to-digital converter (AD), another instruction to address the memory. Therefore, if 64 sample points are needed in one half line period (10ms), 128 instruction cycles are required for data sampling. Second, for the PID algorithm, it is implemented only once in a half line period because the average voltage in every half line period is used to close the loop. Next, the part (V) gradient descent algorithm is implemented only once in a half line period. From the above analysis, it can be concluded that part (III) takes up the most of CPU time in the process without optimization. With the optimization, part (III) and (IV) consume the most of CPU time.

The requirement of the instruction cycles for the part (III), predictive algorithm, is estimated first. It is noted in (8) that

$$0 \le d(k) \le 1 \tag{13}$$

and the denominator in (8) can be approximated as a constant $(V_{ref} + V_d)$. So the duty cycle calculated from (8) can be got directly from the value of the numerator. It is also noted that L/T_s can be used as a constant. Hence, only 8 operations,

which are just for the calculation of the numerator, are required in calculating the duty cycle. Based on (9), a multiplication operation is required to calculate the voltage ripple. Here, $\frac{1}{2\omega_{line}C}\sin(2\omega_{line}t_k)$ is processed as one component and it can be got from the look up table. So the total operation number of the calculation for one duty cycle is 9. For a DSP with the hardware multiplier, typically, each multiplication can be obtained by four instruction cycles: (1) two cycles for data addressing for operands of multiplication, (2) one cycle for arithmetic operation and (3) one cycle for the data addressing for the product. Similarly, four instructions are required for each addition. So for every duty cycle, 36 (9×4) instructions are needed.

If the Boost PFC preregulator operates at 100kHz switching frequency and the input line frequency is 50Hz. There are 1,000 switching cycles in one half line period. In the DSP control system, the total number of the instruction cycles required for the calculation of these 1000 duty cycles is 36,000 ($36\times1{,}000$).

The requirement of the instruction cycles for part (IV), Fast Fourier Transform (FFT) calculation, is estimated secondly[9-10]. The radix-2 FFT algorithm can be used to calculate THD in DSP. It is used to estimate the CPU time requirement in this paper. If we use 64 sample points in half line period, there are 128 points in a line period. Assuming the line frequency is 50Hz, the sample frequency should be 6.4kHz ($=128\times50$). According to sampling theory, the sampling frequency of 6.4kHz can distinguish the signal at frequency of 3.2kHz ($=6.4kHz/2$). It is noted that 3.2kHz is 64^{th} ($=3.2kHz/50Hz$) harmonic frequency of 50Hz base frequency. Usually, the harmonics with the frequency lower than the 13^{th} contribute the most to THD. Therefore, 128 point radix-2 FFT is good enough to calculate THD in the proposed PFC control strategy.

Table 1 shows the required instruction cycles for FFT and predictive algorithm with different sampling points in a half line period[11]. Considering data sampling, PID algorithm implementation, gradient descent implementation, data processing and other overhead, 20% instruction cycle margin is added. Therefore, the new PFC control strategy without the optimization can be achieved by about 43,000(36000×1.2) instruction cycles. For the strategy with the optimization, about 65,000(54000×1.2) instruction cycles are required.

On the one hand, about 36,000 instruction cycles are required for the predictive algorithm only. For the strategy with parameter optimization in which 64 sampling points in a half line period is adopted for FFT, about 65,000 instruction cycles are required. On the other hand, for the cheapest control chip (TMS320LC2404A, 40MIPS, 16 bit fixed point) of TMS320 series of Texas Instrument, 400,000 instruction cycles can be completed in a half line period. Therefore, the capability of the DSP is more than enough for the calculation requirement. Higher switching frequency (e.g., 200kHz) can also be achieved easily based on the proposed predictive PFC control strategy.

VI. Advantages of the Proposed PFC Control Strategy

(1) All the duty cycles required to achieve unity power factor in a half line period are calculated in advance.
(2) The direct relation between the switching frequency and the processing speed of DSP is cut off.
(3) A relatively low performance/low cost DSP or microprocessor can be used to control PFC system operating at high switching frequency.
(4) Not only PFC, but also the other functions, such as parameter monitoring, communication with central control unit, even control of the following DC/DC stage, can also be achieved by the same DSP chip.

VII. Simulation Results

Simulation is performed by MATLAB to verify the proposed digital PFC control algorithm. Fig.8 (a) is the input current of the PFC Boost circuit under 1000w load (full load) with 220v (RMS) input voltage. Fig.8 (b) is the harmonics in the current waveform. Under the full load, the third harmonic is only 0.18A. The THD of the current is 2.73%. The predictive PFC control strategy can achieve very high power factor (0.9996).

The power factor at different load with the input voltage of 220v and 110v (RMS) are shown in Fig.9. It is shown that, with both 220v and 110v input voltage, the power factor is over 0.99 under the range from 25% to full load. The power factor at the low load is a little bit less than that at the high load due to the approximation in the derivation of predictive algorithm (8).

Table I Calculations and Instructions Cycles Required for Control Strategy with Optimization

(Line frequency $f_{line}=50Hz$ and switching frequency $f_s=100kHz$)

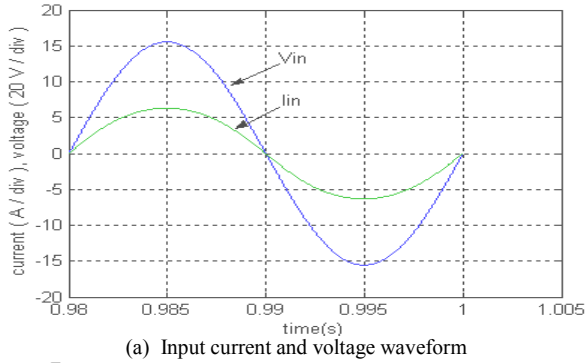
Sampling Point in 1/2 line Period	Point of Radix-2 FFT	Complex Mul*	Complex Add*	Real Mul*	Real Add*	I.C. for FFT	I.C. for Predictive Algorithm only	I.C. for Predictive Algorithm with Optimization
N_s	N	Mc	A_c	M_r	A_r	n_F	n_P	n_{p+opt}
32	64	192	384	768	1152	8000	36,000	44,000
64	128	448	896	1,792	2,688	18000	36,000	54,000
128	256	1,024	2,048	4,096	6,144	41000	36,000	77,000
256	512	2,304	4,608	9,216	13,824	93000	36,000	129,000

*Mul: Multiplication, Add: Addition, I.C.: Instruction Cycles

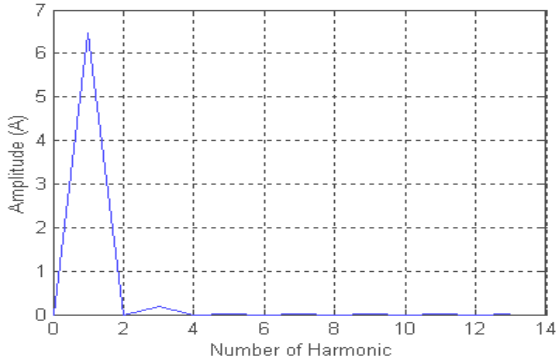
The power factor at the load of 1000w and 500w with different input voltage is shown in Fig. 10. The power factor is always over 0.99 with the input voltage range from 90v to 260v (RMS). It can also be found that the power factor with high input voltage low current is a little bit less that that with low input voltage high current, but still over 0.99. It is verified that the proposed PFC control strategy works well with wide input voltage and load current variation range.

The dynamic performance is also verified by simulation. The output voltage, current waveform, THD and power factor in transient state, in which the load is changed from 1000w (full load) to 250w, are shown in Fig.11 (a), (b) and (c), respectively. When the load is changed at time t=1s, as shown in Fig.11 (a), the output voltage overshoots to 404V. After about 200mS, the output voltage recovers to its stable value. The overshoot is less than 1%. In Fig.11 (b), the current waveform becomes distorted at the time of load changing, t=1s, and recovers back to sinusoidal waveform after 20 half line periods (200mS). At the stead state under 1000w load, the THD and power factor are 2.72% and 0.9996, respectively, as shown in Fig.11 (c). In the transient state, the worst case happens at t = 1.02 second. At that time, the THD and power factor are 0.6281 and 0.8468, respectively. The transient state continues about 200ms and back to the stead state again. At the stead state under 250w load, the THD and power factor are 11.24% and 0.9937, respectively.

The output voltage in transient state, in which the load is changed from 250w to 1000w, is shown in Fig.12. When the load is changed from 250w to 1000w at time t = 1s, the output voltage drops to 396.5V. The decrease is less than 1%. The output voltage recovers to its stable value in about 200mS.



(a) Input current and voltage waveform



(b) Harmonic components of input current

Figure 8. Input current waveform and its harmonic components

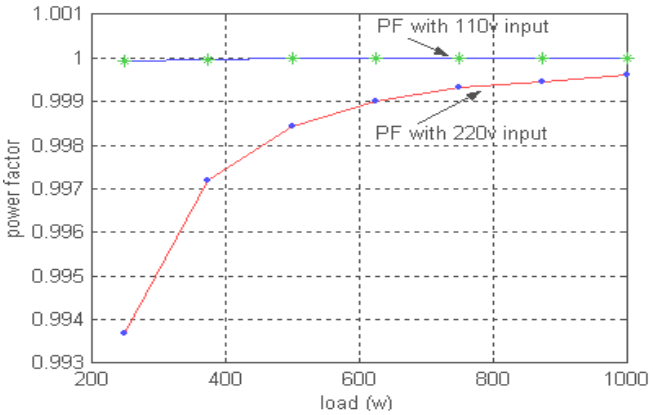


Figure 9. Power factor at different load

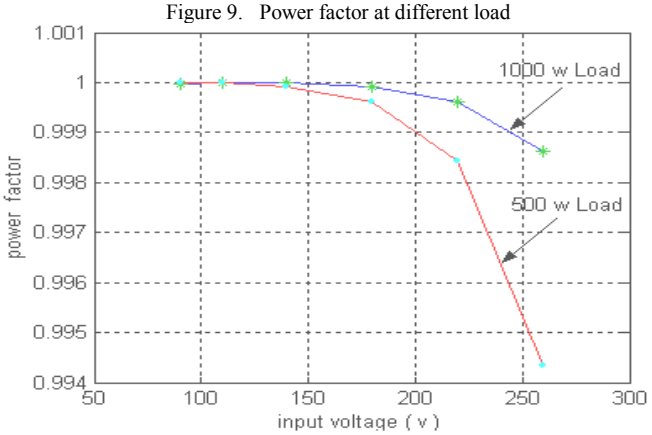
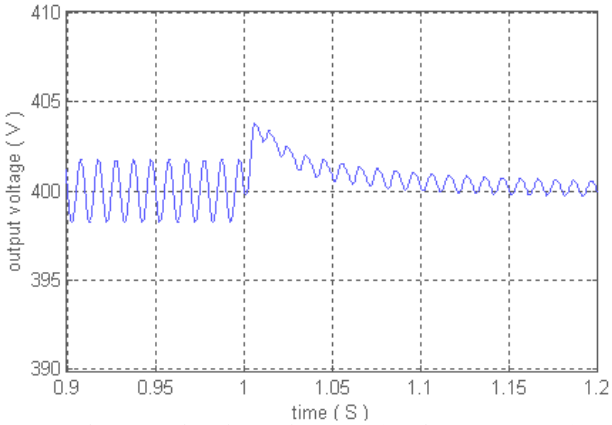
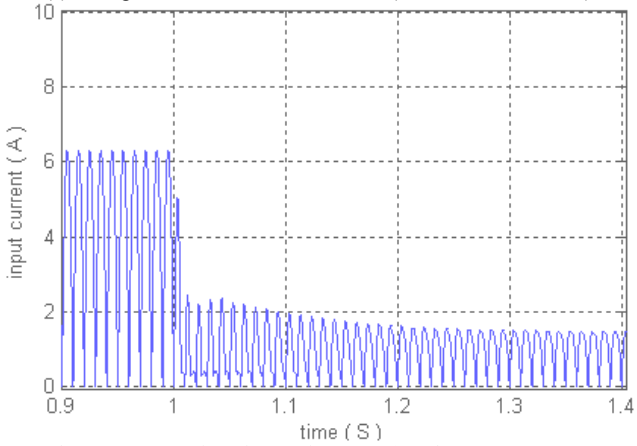


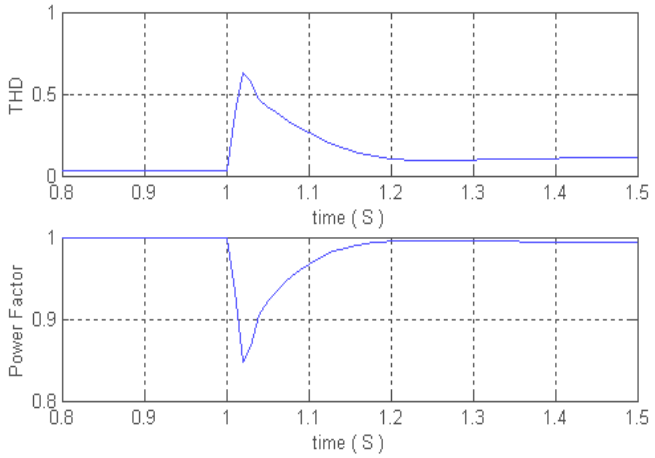
Figure 10. Power factor with different input voltage



(a) Voltage waveform in transient state (Load: 1000w to 250w)



(b) Current waveform in transient state (Load: 1000w to 250w)



(c) THD and power factor in transient state (Load: 1000w to 250w)

Figure 11. Dynamic performance with step load change

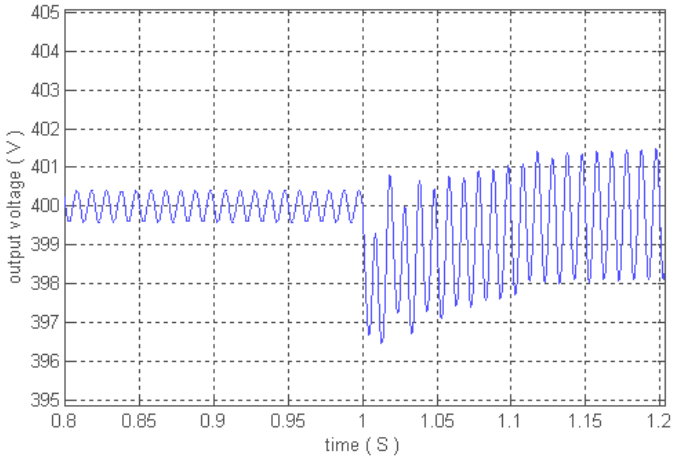


Figure 12. Voltage waveform during step load changed from 250w to 1000w

VIII. CONCLUSION

A new predictive algorithm is proposed for digital control PFC implementation. Based on the Boost topology, the predictive algorithm is derived in detail. By using this predictive control algorithm, all the duty cycles required to achieve unity power factor in a half line period are generated in advance. That means the switching frequency of the PFC is no longer directly dependent on the processing speed of the digital controller. An optimization of control parameter is incorporated into the predictive algorithm to further improve the performance of the PFC. Simulation results show that the proposed strategy works well and unity power factor can be achieved over wide input voltage and load current variation range.

The CPU requirement is also estimated in this paper. The estimation shows that, based on the predictive PFC control method, a cheapest DSP chip (TMS320LC2404A) of TMS320 series is much more than enough to achieve PFC operating at high switching frequency (e.g., 200KHz). Beside PFC, the other issues, such as parameter monitoring, communication, and even control of the following DC/DC stage, can also be achieved by the same DSP chip.

The proposed PFC control strategy is a practical digital implementation with high performance, low cost and potential development.

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