Analysis and Implementation of a New PFC Digital Control Method

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Abstract — A predictive algorithm for digital controlled PFC is introduced in this paper. Based on this algorithm, all of the duty cycles required to achieve unity power factor in a half line period can be calculated by the DSP in advance. The main advantage of this digital control PFC method is that the high switching frequency of the PFC can be achieved because it does not directly depend on the processing speed of DSP. The small signal model is set up for the purpose of designing the voltage loop and analyzing the dynamic performance of DSP controlled PFC system. Input voltage feed forward compensation makes the output voltage insensitive to the input voltage variation and guarantees the input current sinusoidal even if the input voltage is distorted. Simulation results show that the predictive algorithm for digital controlled PFC works well.

I. INTRODUCTION

Power Factor Correction (PFC) is necessary for AC-to-DC switched mode power supplies (SMPS). PFC could result in many benefits for SMPS, including: improving the efficiency and capacity of power system, reducing the harmonic of line current, improving the line voltage quality and reducing the utility bill of customers, etc. Several international standards, such as IEC-1000-3-2 and IEEE-519, were published to limit the harmonics of line current and improve the power factor of power supplies. Therefore, PFC has been designed as a compulsory module in many AC-to-DC converters. In the implementation, many kinds of analog PFC control chips manufactured from different companies are available in the market [1]. Most of control algorithms implemented by these PFC chips are average current mode control and/or peak current mode control. The power factor in these kinds of AC-to-DC converter is usually over 0.99.

Many researchers are working on the digital controlled PFC based on DSP or microprocessors. Digital control has many advantages compared with analog control, such as programmability, adaptability, less part count, less susceptibility to environmental variations, more immunity to input voltage distortion and easier system level management, etc. In addition, the recent development in digital control technique and the cost reduction make it more suitable to be used in power electronics. Average current mode control is implemented in digital controlled PFC implementation [2-3]. In average current mode control, as shown in Fig.1, DSP or microprocessor is used to calculate the duty cycle in every switching period to achieve PFC based on the feedback current and the reference current. Therefore, if the switching frequency is too high, the DSP does not have enough time to complete all the calculation and processing tasks. The problem of limited switching frequency is one of the main barriers of the digital implementation of PFC. It was explored to solve the above problems with limited success in several papers. A digital control method is presented [4], in which the duty cycle is updated once in several switching cycles in order to reduce the calculation time and increase the switching frequency of the PFC converter. The problem is that its harmonics are increased with the increased number of switching cycles in which the duty cycles are not updated. In addition, it is difficult to be implemented by the hardware because there is no consideration about the inductance drift due to the current and temperature variation. A PFC control method based on DSP, which consists of two parallel loops, is explored in [5]. However, its CPU requirement is no less than that based on the conventional average current control. In brief, all of the existing PFC control strategies cannot take full advantages of the digital control since they just implement the analog control law in digital form. Because of the sampling delay and necessary processing time, the switching frequency is limited even when the latest and fastest DSPs are used.

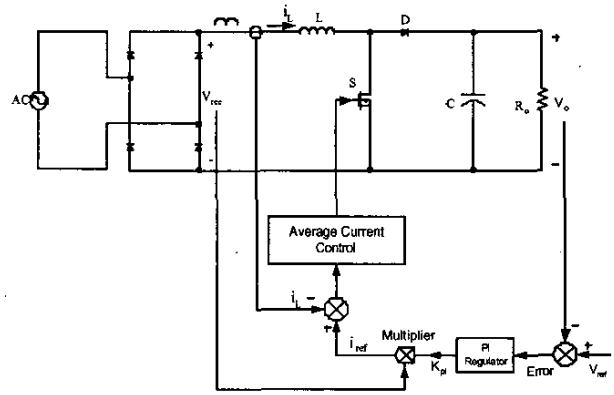

Figure 1. Average current control of the Boost PFC

The existed implementations of the digital controlled PFC have some limitations. First, the switching frequency is limited due to the sampling, calculation and processing time. Further more, even operating at a relatively low switching frequency, the high performance DSP is still exclusively tied by the PFC stage in switched mode power supply (SMPS). Second, the higher the switching frequency, the faster the DSP required. So the implementation of the digital control method in the PFC application is limited due to the high cost. Third, even if the fastest DSP is used in the digital controlled

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PFC system, the switching frequency cannot reach the same level as that in the analog controlled PFC system. All of these problems limit the implementation of digital controlled PFC.

Several approaches were explored to overcome the above limitations of digital controlled PFC, as described in Table 1. The first approach is a digital controller combined with an analog PFC control chip, e.g. UC3854 [6]. This approach is just using a control IC as the inner loop to share the PFC task with DSP. DSP is used to process all the other tasks except PFC, including voltage control loop. High switching frequency can be achieved. The disadvantage is that its control structure is complicated. The second approach is a FPGA combined with an analog to digital converter [7]. In order to implement this approach, a simple PFC control algorithm should be designed to make it suitable for FPGA. However its cost is high. The third approach is to achieve digital controlled PFC by using a low cost DSP based on a new control algorithm, which can achieve high switching frequency. It is the best approach with lowest cost and simplest structure among these three approaches [8]. A new PFC digital control method implemented by a DSP is explored and analyzed in this paper.

TABLE 1 APPROACHES TO SOLVE PROBLEMS OF DIGITAL CONTROLLED PFC

	Approaches	System Cost	Control Structure
1	Digital controller + Analog PFC control chip	Medium	Complicated
2	FPGA + A/D converter + PFC control algorithm	High	Medium
3	DSP + New PFC control algorithm	Low	Simple

The predictive PFC control strategy optimized for DSP implementation is introduced in section 2. The PFC control strategy is based on the predictive algorithm to achieve power factor correction. In this method, all of the duty cycles required to achieve high power factor in a half line period are calculated in advance. The major advantage of this method is that, the switching frequency of the PFC does not directly depend on the processing speed of DSP. In section 3, the model of Boost PFC based on predictive control method is set up and analyzed. The input voltage feed forward is incorporated with the predictive algorithm to compensate the duty cycles for the purpose of maintaining sinusoidal input current and stabilizing the output voltage when there exist variation and/or distortion in line voltage. It is analyzed in section 4. In section 5, the simulation results are presented. The conclusion is given in section 6.

II. PRINCIPLE OF PREDICTIVE CONTROL FOR PFC

The topology of Boost converter is shown in Fig.2. The proposed predictive PFC algorithm for DSP control is derived based on the assumptions: (1) Boost converter operates at continuous conduction mode (2) the switching frequency is much higher than the line frequency. With above assumptions, when the switch S is on and off, the inductor voltage is expressed as

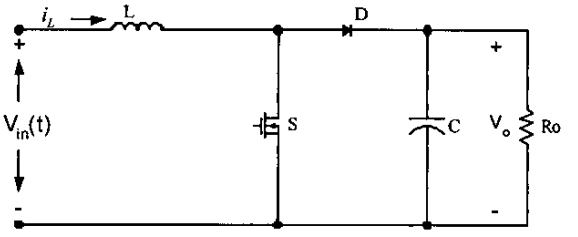

Fig.2 Boost converter topology

$$L\frac{di_L}{dt}=V_{in} \qquad t_k \le t < t_k+d_kT_s \qquad \text{switch on} \qquad (1)$$

$$L\frac{di_L}{dt}=V_{in}-V_o \qquad t_k+d_kT_s \le t < t_{k+1} \qquad \text{switch off} \qquad (2)$$

The discrete form for the inductor current at the beginning of $(k+1)^{th}$ switch cycle in term of the inductor current at the beginning of k^{th} switching cycle can be derived from (1) and (2) as

$$i_L(k+1)=i_L(k)+\frac{V_{in}(k)\cdot T_s}{L}-\frac{V_o(1-d(k))\cdot T_s}{L} \qquad (3)$$

Where $d(k)$ and T_s are the duty cycle and switching period. $V_{in}(k)$ is the input voltage in k^{th} switching cycle. $i_L(k)$, $i_L(k+1)$ are the inductor currents at the beginning of k^{th} and $(k+1)^{th}$ switching cycles, respectively.

When Boost converter is operating at unity power factor, the inductor current should follow the reference current i_{ref}, which is proportional to the rectified input voltage, as shown in Fig.3. At the same time, the output voltage should follow the reference voltage V_{ref}. That is

$$V_o = V_{ref} \qquad (4)$$

$$i_L(k+1)=i_{ref}(k+1) \qquad (5)$$

$$i_L(k)=i_{ref}(k) \qquad (6)$$

Substituting (4) (5) (6) into (3), the duty cycle in k^{th} switching period, $d(k)$, can be calculated as

$$d(k)=\frac{[i_{ref}(k+1)-i_{ref}(k)]}{V_{ref}}\cdot\frac{L}{T_s}+\frac{V_{ref}-V_{in}(k)}{V_{ref}} \qquad (7)$$

Where i_{ref} is the rectified sinusoidal waveform and its amplitude is determined by the outer voltage loop.

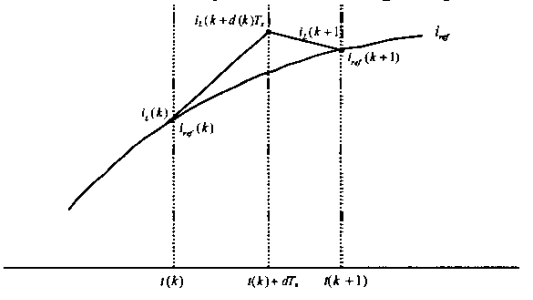

Fig.3 Inductor current waveform and reference current in one T_s

The predictive algorithm (7) can be used to generate the duty cycles by DSP in the PFC implementation. In order to achieve unity power factor, a more accurate model, as shown in Fig.4, is used to predict the required duty cycles. The inductor winding resistance, R_L, the on resistance of switch, R_{on}, the voltage drop across diode, V_d, and the output voltage ripple, v_{o_ripple}, are considered in this model. The duty cycles can be derived based on this accurate model as

$$d(k)=\frac{[i_{ref}(k+1)-i_{ref}(k)]}{(V_{ref}+v_{o\_ripple})+V_d-R_{on}i_{ref}(k)}\cdot\frac{L}{T_s}-\frac{V_{in}-(V_{ref}+v_{o\_ripple})-V_d-R_Li_{ref}(k)}{(V_{ref}+v_{o\_ripple})+V_d-R_{on}i_{ref}(k)} \quad (8)$$

Where, v_{o_ripple} can be estimated as

$$v_{o\_ripple}(k)=-I_o\times\frac{1}{2\omega_{line}C}\sin(2\omega_{line}t_k) \quad (9)$$

(8) is the predictive algorithm used to implement unity power factor. All of the duty cycles required to achieve unity power factor in a half line period are calculated by DSP according (8) in advance. One of the advantages of this algorithm is that the requirement for DSP to achieve PFC is reduced. So the high switching frequency of digital controlled PFC can be achieved based on the low cost digital controller.

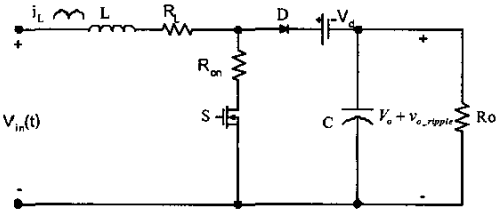

Figure 4. Accurate model of Boost converter

The digital controlled Boost PFC based on the predictive algorithm is shown in Fig.5. The duty cycles are generated by the predictive algorithm. The input voltage v_{in} is sensed as the feed forward to the predictive algorithm (8). The input feed forward compensation will be discussed in detail in section 4. The reference current, i_{ref}, is obtained from the multiplier. Its amplitude is determined by the output of the PID controller in the voltage loop. Its phase and sinusoidal waveform are determined by the zero cross detection and the sine-wave-look-up-table. The output voltage, V_o, is controlled by the closed loop with a PID regulator. In this digital control system, the feedback signal is V_o. The output of the DSP is the gate signal for the switch S. There is no current loop in this control system. All the duty cycles required to achieve unity power factor in a half line period can be generated in advance with this predictive control strategy.

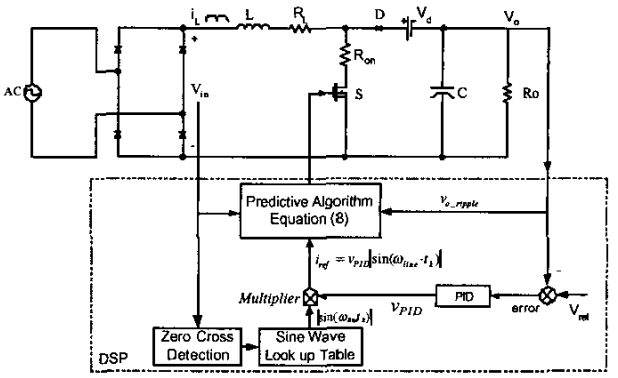

Fig.5 DSP controlled Boost PFC based on predictive algorithm

III. Model of Boost PFC Based on Predictive Control

3.1 Control-to-output Transfer Function

It is necessary to setup a model so that the dynamic performance of the DSP controlled PFC can be analyzed. At the same time, the design of PID regulator can be guided based on this model. The small signal model is derived based on the conditions: (1) the AC-to-DC converter can be modeled as a loss-free resistor, (2) the high-frequency switching ripple can be neglected, (3) the control varies at frequency sufficiently less than the AC line frequency, (4) small signal conditions are met. Based on above assumption, a small signal model of PFC based on Boost converter can be described as the equivalent circuit, as shown in Fig.6 [9][10]. j_1, j_2 are the coefficients which describe how the output of PID regulator influences the input and output current of AC-to-DC converter. r_1, r_2 are the equivalent ac resistances, which describe the input and output characteristic of converter. g_2 describes how the input voltage affects the of output current. R is the incremental resistor of the load. $\hat{v}_{pid}$ is the output of PID regulator in Fig.5. $\hat{v}$ is the output voltage of PFC. All of these parameters are evaluated at the quiescent operating point. This model is based on the average value in a half line period and valid for the voltage regulation frequency sufficiently less than the line frequency. The control-to-output transfer function is derived from Fig.6 as

$$G_P(s)=\frac{\hat{v}(s)}{\hat{v}_{pid}(s)}=j_2\frac{r_2//R}{1+sC\cdot(r_2//R)} \quad (10)$$

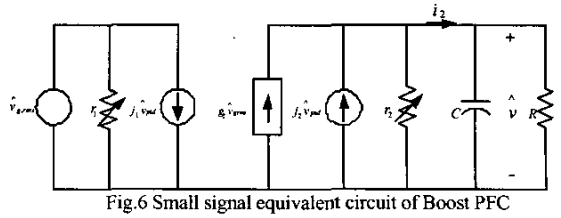

Fig.6 Small signal equivalent circuit of Boost PFC

Where $j_2 = \frac{P}{VV_{pid}}$ and $r_2 = \frac{V^2}{P}$, V, V_{pid} and P are the output voltage, output of PID regulator and average power of Boost PFC at the quiescent operating point, respectively.

3.2 Small Signal Model of Closed Loop

The block diagram of the Boost PFC with closed voltage loop is shown in Fig.7. The feedback of output voltage is an average value in a half line period. Therefore, the sampling period is $T = 10ms$. In Fig.7, one sampling period delay is considered. The loop transfer function is derived as

$$\phi(S) = \frac{1}{80} \cdot \frac{1}{sT}(1 - e^{-Ts}) \cdot (k_p + \frac{k_i}{s}) \cdot j_2 \frac{r_2 // R}{1 + sC \cdot (r_2 // R)} \quad (11)$$

Where k_p, k_i are the proportional coefficient and integral coefficient of PI regulator, respectively. The feedback coefficient is $1/80$.

3.3 Dynamic Performance Analysis

The dynamic performance of the digital predictive control PFC system was analyzed based on the above model. The parameters used in the analysis are: $p_{load} = 1000W$ (resistive load), $V_o = 400V$, $V_{in,RMS} = 220V$, sampling period $T = 10ms$, proportional coefficient $k_p = 80$ and integral coefficient $k_I = 1500$. The Bode plot of the loop transfer function $\phi(S)$ is shown in Fig.8, in which the bandwidth is about 12Hz and the phase margin is about 60 degree. The phase margin and gain margin are sufficient enough for the PFC system with closed loop.

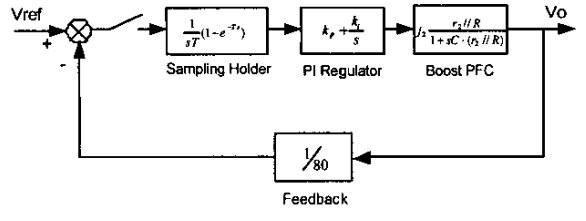

Fig.7 Block diagram of Boost PFC system with closed voltage loop

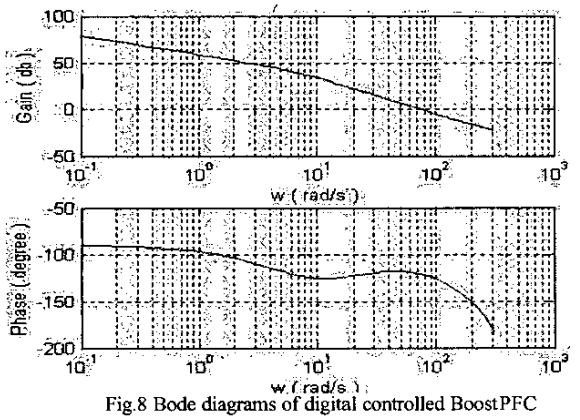

Fig.8 Bode diagrams of digital controlled BoostPFC

IV. Input Voltage Feed Forward Compensation

A compensation module based on the input voltage feed forward is introduced in the predictive algorithm (8) to achieve better dynamic and steady state characteristics. Two types of performance can be improved by input voltage feed forward: (1) stabilizing the output voltage for a step change in the line voltage (2) compensating the calculated duty cycles to guarantee sinusoidal line current when there is distortion in the line voltage.

In predictive algorithm, the input voltage, $V_{in}(k) = |V_1 \sin(\omega_{line} \cdot t_k)|$, is an ideal sinusoidal waveform which is generated based on a lookup table, so that the duty cycle can be calculated in advance. However, the line voltage could be distorted or varied. In the case of input voltage feedforward, the real time input voltage is sensed and used to modify the duty cycle. When the input voltage variation is sensed, the duty cycles, which are generated by DSP in advance based on (8), will be updated to be

$$d_{update}(k) = d(k) + \Delta d(k) \quad (12)$$

Where, $d_{update}(k)$, is the duty cycle sent to gate of Boost MOSFET, and $d(k)$ is the duty cycle calculated by (8). $\Delta d(k)$ is the compensated component

$$\Delta d(k) = \frac{\Delta v_{in}(k)}{V_{ref}} \quad (13)$$

Where, $\Delta v_{in}(k) = V_{in}(k) - v_{in}(k)$, is the input voltage variation. $v_{in}(k)$ is the sensed value of input voltage. $\Delta v_{in}(k)$ is the difference between $v_{in}(k)$ and $V_{in}(k)$. (13) is derived from (7) just for the purpose of simplification in expression. It should be noted that $v_{in}(k)$ will be stored in the look up table used as the updated $V_{in}(k)$ in the next half line period. This input voltage compensation can be implemented easily by a DSP because only little calculation is required.

It is analyzed here in detail for the Boost PFC to be controlled by predictive algorithm if there are harmonics in the input voltage, v_{in}, expressed as

$$v_{in}(k) = \left| V_1 \sin(\omega_{line} \cdot t_k) + \sum_{i=3,5,\cdots}^{\infty} V_i \sin(i \cdot \omega_{line} \cdot t_k) \right| \quad (14)$$

The variation between the ideal input voltage, $V_{in}(k)$, and the feed forward input voltage, $v_{in}(k)$, is

$$\Delta v_{in}(k) = \left| V_1 \sin(\omega_{line} \cdot t_k) \right| - \left| V_1 \sin(\omega_{line} \cdot t_k) + \sum_{i=3,5,\cdots}^{\infty} V_i \sin(i \cdot \omega_{line} \cdot t_k) \right| \quad (15)$$

Then the duty cycles can be calculated after input voltage compensation according to (12) and (13). Now one more question remained: where do the voltage harmonics drop? Substituting (7) into (12), the duty cycles calculated after input voltage feed forward compensation are derived as

$$d_{update}(k) = \frac{[i_{ref}(k+1) - i_{ref}(k)]}{V_{ref}} \cdot \frac{L}{T_s} + \frac{V_{ref} - |V_1 \sin(\omega_{line} \cdot t_k)|}{V_{ref}} + \Delta d(k) \quad (16)$$

According to the average equivalent circuit model of Boost topology as shown in Fig. 9, the voltage drop on the diode is

$$v_d(k) = d_{update}(k) \cdot V_o \qquad (17)$$

In the stead state, $V_o = V_{ref}$, the voltage across the diode is derived by substituting (13), (15) and (16) into (17), as

$$v_d(k) = V_{ref} + [i_{ref}(k+1) - i_{ref}(k)] \cdot \frac{L}{T_s} - \left| V_1 \sin(\omega_{line} \cdot t_k) + \sum_{i=3,5,..} V_i \sin(i \cdot \omega_{line} \cdot t_k) \right| \qquad (18)$$

It is shown from (18) that the harmonics drop across the diode. The voltage across diode for distorted input voltage is shown in Fig.16.

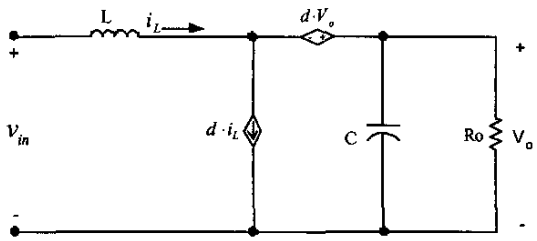

Fig.9 Average equivalent circuit model of Boost topology

The input voltage feed forward solves two problems. First, it stabilizes the PFC system and improves its dynamic performance when there is input voltage step change. Therefore, the output voltage is insensitive to the input voltage variation. Second, it can achieve high power factor even when there is distortion in the line voltage. Therefore, the input current can be still sinusoidal in this situation. The input voltage feed forward compensation technique is simulated in section 5.

V. SIMULATION RESULTS

Simulation is performed by using MATLAB to verify the proposed digital PFC control algorithm.

The power factor at different loads for input voltages of 220v and 110v (RMS) are shown in Fig.10. It is shown that, for both 220v and 110v input voltage, the power factor is over 0.99 with range from 25% to full load. The power factor at low load is a little bit less than that at high load due to the approximation in the derivation of predictive algorithm (8).

The power factor at the loads of 1000w and 500w for different input voltage is shown in Fig. 11. The power factor is always over 0.99 for the input voltage range from 90v to 260v (RMS). It can also be found that the power factor for high input voltage and low current is a little bit less than that for low input voltage and high current, but still over 0.99. It is verified that the proposed PFC control strategy works well for wide input voltage and load current variation range.

The dynamic performance is also simulated. The output voltage in transient state, in which the load is changed from 1000w (full load) to 250w, is shown in Fig.12. When the load is changed at time t=1s, the output voltage overshoots to 404V. After about 200mS, the output voltage stabilize to be the reference value. The overshoot is less than 1%.

The output voltage in transient state, in which the load is changed from 250w to 1000w, is shown in Fig.13. When the load is changed from 250w to 1000w at time t = 1s, the output voltage drops to 396.5V. The decrease is less than 1%. The output voltage recovers to its stable value in about 200mS.

The output voltage for a step change in the line voltage is shown in Fig.14. When input voltage is changed from 220v (RMS value) to 190v at time t=0.205s, the output voltage almost does not change. The output voltage is magnified in the middle of Fig.14. Its average value in a half line period is only decreased from 400.2v to 399.7v. So the output voltage is insensitive to the input voltage feed forward compensation.

Fig.15 and Fig.16 show what happens when the input voltage is distorted. In order to make the result obvious, there is only third harmonic in the line voltage. The magnitude of the third harmonic is 15% of the fundamental component. The input voltage and current waveform are shown in Fig. 15. The input current can still remain sinusoidal when the input voltage is highly distorted. The power factor under this situation is 0.998.

The voltage across the diode is shown in Fig.16. By comparing the Fig.15 and Fig.16, it is obviously that the harmonics of voltage drop across the diode.

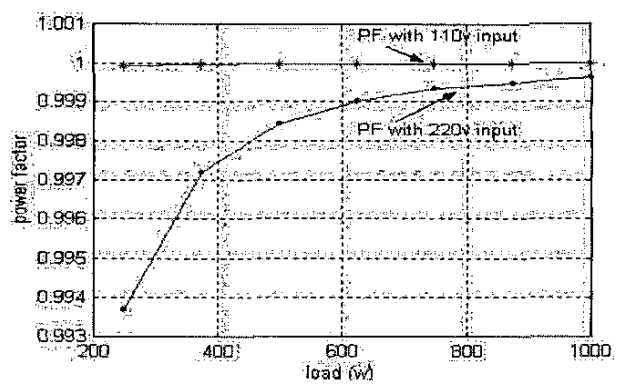

Fig.10 Power factor for different load currents

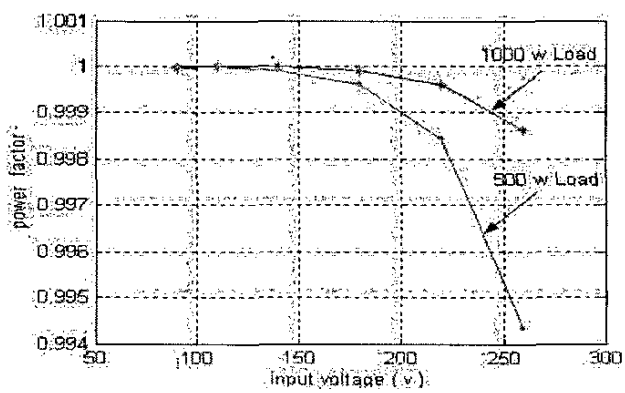

Fig.11 Power factor for different input voltages

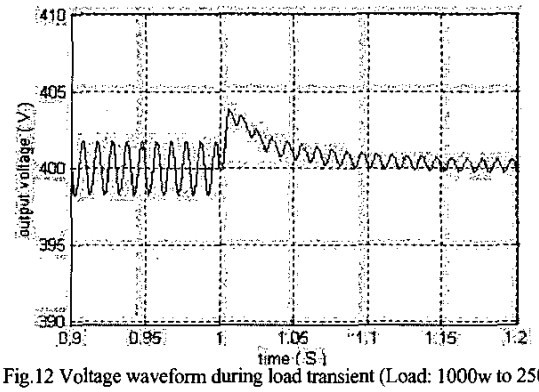

Fig.12 Voltage waveform during load transient (Load: 1000w to 250w)

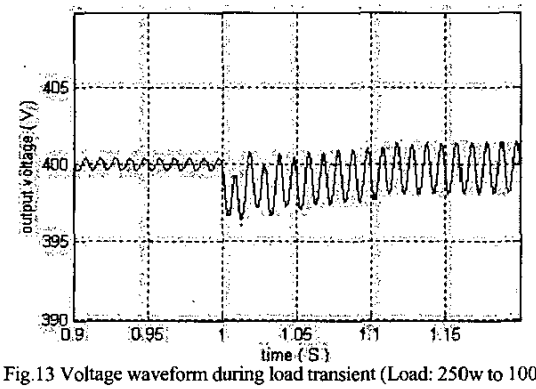

Fig.13 Voltage waveform during load transient (Load: 250w to 1000w)

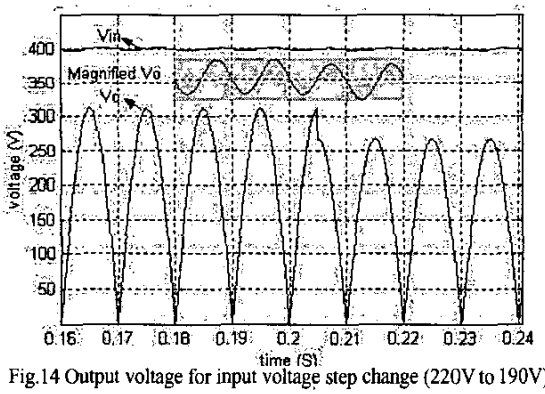

Fig.14 Output voltage for input voltage step change (220V to 190V)

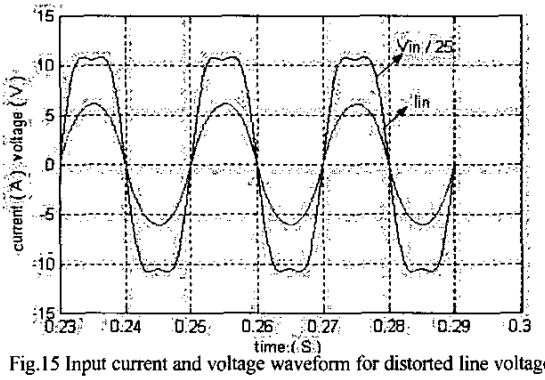

Fig.15 Input current and voltage waveform for distorted line voltage

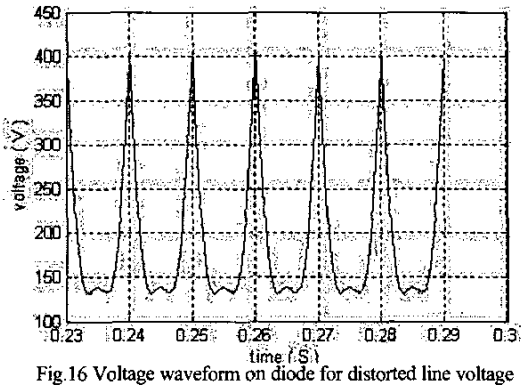

Fig.16 Voltage waveform on diode for distorted line voltage

VI. CONCLUSION

The digital control method for PFC is introduced in this paper. The predictive algorithm to achieve unity power factor is derived based on the Boost topology. The main advantage of this digital control PFC method is that all of the duty cycles required in a half line period can be calculated in advance. The high switching frequency of the PFC can be achieved because it does not directly depend on the processing speed of DSP.

A small signal model was setup to analyze the dynamic performance of the PFC system. The parameters of PID regulator can be designed based on this model. An input voltage compensation technique is proposed and incorporated with the predictive algorithm. Benefited from the input voltage feed forward, the stable output voltage and sinusoidal input current were achieved when there is variation/distortion in line voltage. Simulation results show that the digital controlled PFC works well in both steady and dynamic states.

REFERENCE

[1] P. C. Todd, "UC3854 Controlled Power Factor Correction Circuit Design", U-134, Unitrode Application Note, pp.3-269 - 3-288

[2] Minghua Fu, Qing Chen, "A DSP Based Controller for Power Factor Correction in a Rectifier circuit", APEC, pp. 144 -149

[3] Simone Buso, Paolo Mattavelli, Leopoldo Rossetto and Giorgio Spiazzi, "Simple Digital Control Improving Dynamic Performance of Power Factor Pre-regulators", IEEE Transaction on Power Electronics, Vol.13, No.5, Sep. 1998, pp.814-823

[4] Stephane Bibian, Hua Jin, "Digital Control with Improved Performance for Boost Power Factor Correction Circuits", APEC 2001, pp.137 -143

[5] Sangsun Kim, P. Enjeta, " Control of Multiple Single Phase PFC Modules with a Single Low-Cost DSP", APEC 2003, pp.375-381

[6] Ahmed H. Mitwalli, Steven B. Leeb, George C. Verghese, V. Joseph Thottuvelil, "An Adaptive Digital Controller for a Unity Power Factor Converter", IEEE Transaction on Power Electronics, Vol.11, No.2, March 1996, pp. 374-382

[7] P. Zumel, A. de Castro, O. Gaecia, T. Riesgo, J. Uceda, "Concurrent and Simple Digital Controller of an AC/DC Converter with Power Factor Correction", APEC 2002, pp. 469-475

[8] Wanfeng Zhang, Guang Feng, Yanfei Liu, Bin Wu, "A New Predictive Control Strategy for Power Factor Correction", APEC 2003, pp.403-409

[9] R. B. Ridley, "Average Small-signal Analysis of the Boost Power Factor Correction Circuit", Proceeding of the Virginia Power Electronics Center Seminar, Blacksburg, VA, Sept. 1989, pp.108-120

[10] Robert W. Erickson, Dragan Maksimovic, "Fundamentals of Power Electronics", Second Edition, Kluwer Academic Publishers, Massachusetts 02061, 2001, pp.668-673