DSP Implementation of Predictive Control Strategy for Power Factor Correction (PFC)

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Abstract — **A predictive algorithm for digital control PFC is presented in this paper. Based on this algorithm, all of the duty cycles required to achieve unity power factor in one half line period are calculated in advance by the DSP. A Boost converter controlled by these pre-calculated duty cycles can achieve sinusoidal current waveform. Input voltage feed-forward compensation makes the output voltage insensitive to the input voltage variation and guarantees sinusoidal input current even if the input voltage is distorted. A prototype of Boost PFC controlled by a DSP evaluation board was setup to implement the proposed predictive control strategy. Test results show that the proposed predictive strategy for PFC achieves unity power factor.**

Keywords-predictive algorithm; digital control; power factor correction

I. INTRODUCTION

With the development of digital techniques, more and more control algorithms are implemented in power electronics circuits by the digital chips, such as microprocessors or digital signal processors (DSP). One reason is that digital control can implement more complicated algorithms. Another reason is that digital control has many advantages over analog control, including programmability, adaptability, low part count and reduced susceptibility to environmental variations, etc. In addition, it is possible to achieve better performance in digital implementation than that in analog implementation with the same cost. As a result, it is prudent to explore digital control techniques for PFC application.

Digital control PFC implementations have been explored by many researchers [1-3]. Basically, most of the digital implementations for PFC are based on average current mode control. Some works have been done to make the digital control a competitive option to analog controlled PFC implementation. Unfortunately, all of the existing control method cannot take full advantages of the digital technique.

A predictive control strategy suitable for digital implementation of PFC is proposed in this paper. The basic idea of the proposed digital control PFC algorithm is that all the duty cycles required to achieve unity power factor in a half line period are calculated in advance by using a predictive algorithm. The proposed PFC control strategy is based on the prediction, not feedback, to achieve power factor correction. Because the computation requirement to implement this control strategy is low, a 40*MHz*, 16bit, fixed point DSP can be used to realize digital control PFC system operating at high switching frequency.

In this paper, the existing digital control methods for PFC are reviewed and their limitations are highlighted in section II. The principle of the predictive control strategy for digital PFC implementation is presented in section III. In section IV, the input voltage fed-forward is incorporated with the predictive algorithm to compensate the duty cycles for the purpose of maintaining sinusoidal input current and stabilizing the output voltage when there exist variation or distortion in line voltage. The DSP implementation is described in section V. The simulation and experimental results are given in section VI. The conclusion is presented in section VII.

II. LIMITATIONS OF EXISTING DIGITAL PFC CONTROL

The switching frequency is limited in the conventional digital control PFC system because of the sampling time delay and the necessary processing time. Average current mode control, which is one of the main conventional analog control strategies, as shown in Fig.1, is widely used in digital control PFC [1][2]. In Fig. 1, the average inductor current, i_L, is forced to follow the reference current, i_{ref}, which is proportional to the rectified voltage, so that unity power factor is achieved. In digital implementation of average current mode control, the DSP or microprocessor is used to calculate the duty cycle in every switching cycle, T_s, based on the feedback current, i_L, and the reference current, i_{ref}. The switch S is controlled by the calculated duty cycles to achieve unity power factor. In [3], single sampling in single period method (SSSP) is adopted. 50kHz switching gate signal is controlled by the DSP (TMS320F240, 20MHz). The digital average current mode control was implemented in these PFC applications. The whole process in a digital control PFC based on average current mode control includes: (a) voltage and current sampling, (b) voltage error calculation, (c) voltage PI regulation, (d) reference current calculation, (e) current error calculation, (f) current PI regulation and (g) duty cycle generation. In addition, the other operations are necessary for the PWM I/O port to output the duty cycle. All these operations have to be finished within every switching cycle. Because this process is iteratively running in every switching

cycle, the DSP is almost tied up by all these operations and calculations. Therefore, the switching frequency is limited due to the speed limitation of DSP. This disadvantage is common to all existing digital average current mode control implementations.

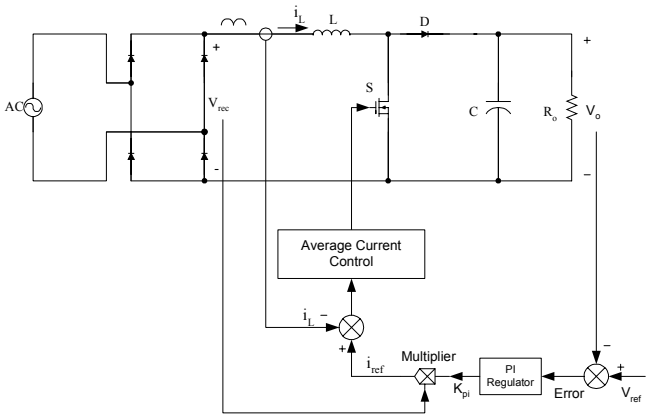


Fig. 1 Average current mode control of Boost PFC

Efforts have been tried to solve the above problems. A digital control method was presented in [4] for the purpose of reducing the computation time and increasing the switching frequency by updating the duty cycles once in several or several tens switching cycles. Unfortunately, the harmonics in the line current are increased in the Boost PFC controlled by that method. Digital current program control using predictive algorithm was presented in [5]. In that paper, the duty cycle, *d(n+1)*, was calculated based on the value of the present duty cycle *d(n)* and sensed inductor current, input voltage and output voltage. Unity power factor was achieved. However, the duty cycle calculation requires the duty cycle value in the previous switching cycle and the computation requirement is not obviously reduced compared to that in the digital PFC implementation based on current mode control.

It is observed from the above analysis that the existed implementations of the digital control PFC have the following limitations. First, the switching frequency is limited due to the sampling, computation and processing time. Even operating at a relatively low switching frequency, the DSP is still tied up by the PFC stage in switched mode power supply (SMPS). Second, the higher the switching frequency, the faster the DSP required. Consequently, the implementation of the digital control method in the PFC application is limited due to the high cost. Third, even if the fastest DSP was used in digital control PFC systems, the switching frequency cannot reach the same level as that in analog controlled PFC systems.

Several control strategy were explored to overcome the above limitations of digital control PFC. The first approach is a digital controller combined with an analog PFC control chip, e.g. UC3854 [6]. That approach uses an analog control IC in the inner loop. The DSP provide the reference current signal to the analog control IC. Using that method, the duty cycle is directly determined by the analog circuit. The DSP only handles the low frequency tasks for the outer voltage loop. Therefore, the switching frequency does not depend on the speed of DSP and high switching frequency can be achieved. However, its control structure is complicated and the cost is increased as both analog chip and DSP are required. The second approach is using a FPGA combined with an analog to digital converter (ADC) [7][8]. A simple PFC control algorithm, which is actually "a digital version of charge control", is specifically designed to be suitable for FPGA in that implementation. The switch turns "on" at the beginning of every switching period and "off" when the mean value of input current reaches the reference value. The mean value of input current is the sum of the input current samples divided by the number of samples in one switching cycle. In order to guarantee the resolution of the duty cycles, a fast ADC is required in the integral operation for the calculation of input current mean value. This increases the cost of the control system. Furthermore, there is a trade-off between the switching frequency and the duty cycles resolution. Hence the switching frequency is limited in that method because the duty cycle resolution should be remained at a satisfactory level.

The proposed digital control PFC strategy can achieve unity power factor operating at high switching frequency by using a low cost DSP based on a predictive control algorithm.

III. PRINCIPLE OF PREDICTIVE PFC CONTROL STRATEGY

The topology of Boost converter is shown in Fig. 2. The proposed predictive PFC algorithm is derived based on the following assumptions: (1) Boost converter operates at continuous conduction mode, (2) The switching frequency is much higher than the line frequency. So the input voltage V_{in} can be assumed as a constant during one switching cycle. Based on these assumptions, when the switch S is on or off, the circuit of Fig. 3 (a) or (b) are obtained and the inductor current can be described as (1) and (2), respectively.

$$L\frac{di_L}{dt} = V_{in} \qquad t_k \le t < t_k + d_k T_s \tag{1}$$

$$L\frac{di_L}{dt} = V_{in} - V_o \qquad t_k + d_k T_s \le t < t_{k+1} \tag{2}$$

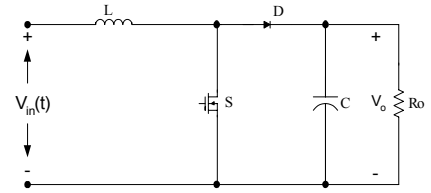


Fig. 2 Boost converter topology

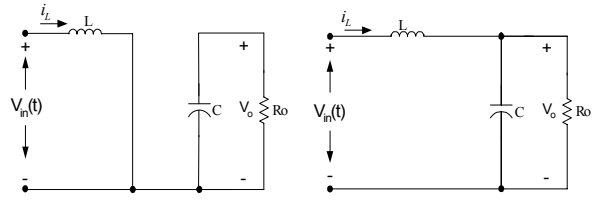


Fig. 3 Boost converter circuit

The discrete form for the inductor current at the beginning of $(k+1)^{th}$ switch cycle in term of the inductor current at the beginning of k^{th} switching cycle can be derived from (1), (2) as

$$i_L(k+1) = i_L(k) + \frac{V_{in}(k)\cdot T_s}{L} - \frac{V_o(k)\cdot(1-d(k))\cdot T_s}{L} \quad (3)$$

where $d(k)$ and T_s are the duty cycle and switching period. $V_{in}(k)$ is the input voltage in k^{th} switching cycle. $i_L(k)$, $i_L(k+1)$ are the inductor current at the beginning of k^{th} and $(k+1)^{th}$ switching cycles, respectively.

When PFC is achieved, the inductor current should follow the reference current $i_{ref}(k)$, which is proportional to the rectified input voltage, as shown in Fig. 4. At the same time, the output voltage should follow the reference voltage V_{ref}. That is

$$V_o(k) = V_{ref} \quad (4)$$

$$i_L(k+1) = i_{ref}(k+1) \quad (5)$$

$$i_L(k) = i_{ref}(k) \quad (6)$$

Substituting (4) (5) (6) into (3), the duty cycle in k^{th} switching period, $d(k)$, can be calculated as

$$d(k) = \frac{V_{ref} - V_{in}(k)}{V_{ref}} + \frac{[i_{ref}(k+1) - i_{ref}(k)]}{V_{ref}} \cdot \frac{L}{T_s} \quad (7)$$

where,

$$i_{ref}(k) = v_{PID} \cdot \left|\sin(\omega_{line} \cdot t(k))\right| \quad (8)$$

v_{PID} is the peak value of the reference current, which is regulated by the output of the voltage loop PID controller, as shown in Fig. 7. $|sin(\omega_{line}\cdot t(k)|$ is the rectified line frequency sinusoidal waveform, which is stored as a look up table. In DSP implementation, the limitation value of the PID regulator is easily determined based on the rated load.

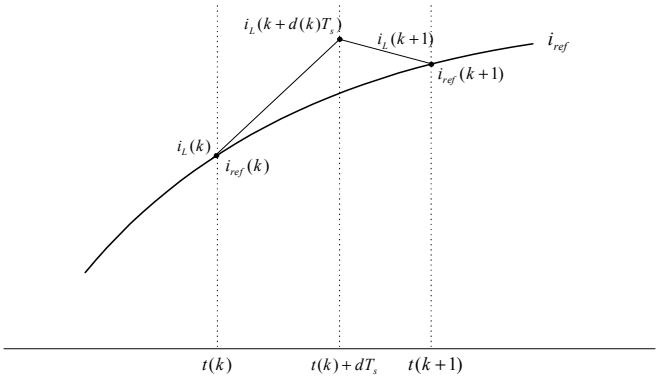


Fig. 4 Input current waveform and reference current in one T_s

The predictive algorithm (7) can be used to generate the duty cycles and achieve near unity power factor in the implementation of PFC with Boost topology. In order to improve the inductor current waveform further, a more accurate model, as shown in Fig.5, could be used to predict the required duty cycles. In this model, the impacts of the inductor winding resistance, R_L, the on resistance of switch, R_{on}, the voltage drop across diode, V_d, and the output voltage ripple, v_{o_ripple}, are considered. However, the switching loss and dead time are not considered in this model because their effect on inductor current waveform can be neglected. Based on the model in Fig. 5, the duty cycles can be derived as:

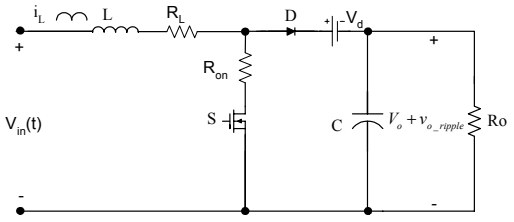


Fig. 5 Accurate model of Boost converter

$$d(k) = \frac{(V_{ref} + v_{o\_ripple}(k) + V_d) + R_L i_{ref}(k) - v_{in}(k)}{(V_{ref} + v_{o\_ripple}(k) + V_d) - R_{on} i_{ref}(k)} + \frac{[i_{ref}(k+1) - i_{ref}(k)]\cdot \frac{L}{T_s}}{(V_{ref} + v_{o\_ripple}(k) + V_d) - R_{on} i_{ref}(k)} \quad (9)$$

where , v_{o_ripple} can be estimated as

$$v_{o\_ripple}(k) = -I_o \times \frac{1}{2\omega_{line} C}\sin(2\omega_{line} t_k) \quad (10)$$

(7) and (9) are the predictive algorithms, which is used to implement power factor correction in this paper.

The proposed digital control strategy for PFC is actually a "valley tracking reference current algorithm". It is the valley values of current, $i_L(k)$ and $i_L(k+1)$, that are forced to track the reference current, i_{ref}, as shown in Fig. 4. Theoretically, the mean value of the inductor current in every switching cycle should follow the reference current. Hence, there is an approximation in the predictive algorithm (7) and (9). If the inductor current ripple in one switching cycle can be neglected compared with the amplitude of inductor current, the proposed control algorithm works well. This approximation condition is easier to be satisfied for high load than that for light load. In the experimental results of section VI, the power factor for light load is a little bit less than that for high load because of this approximation.

Further investigation to the proposed predictive PFC algorithm is necessary to understand the philosophy behind it. Actually, there are two components in (7), expressed as

$$d(k) = d_1(k) + d_2(k) \quad (11)$$

The first component, $d_1(k)$, expressed as

$$d_1(k) = \frac{L}{T_s}\frac{i_{ref}(k+1) - i_{ref}(k)}{V_{ref}} \quad (12)$$

is determined by the output of voltage loop and the reference sinusoidal waveform.

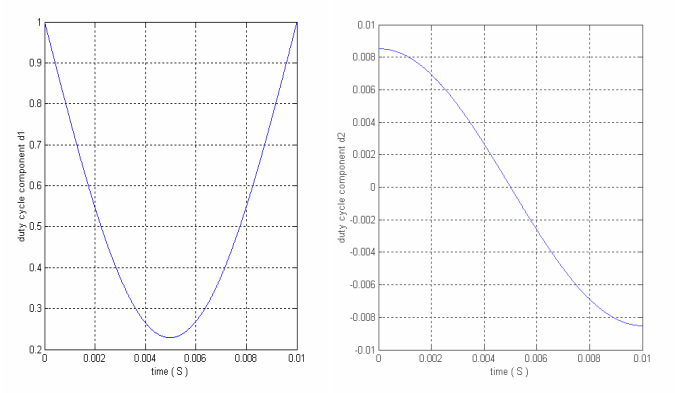
The second component, $d_2(k)$, expressed as

$$d_2(k) = 1 - \frac{V_{in}(k)}{V_{ref}} \quad (13)$$

is determined by the input voltage fed-forward. $d_2(k)$ can guarantee the output voltage, V_o, be stable for the transient state of input voltage change.

Under the parameters of V_{in}=220V(RMS), V_o=400V, P_{load}=1000W, f_{sw}=160kHz, f_{line}=50Hz, and L=1.2mH, the curves of d_1 and d_2 in one half line period are shown in Fig. 6 (a) and (b), respectively. In Fig. 6 (a), the minimum value of d_1 is determined by the reference voltage V_{ref} and the peak value of the input voltage. In Fig. 6 (b), the peak-to-peak

value of d_2 is regulated by the output of the PID controller. Eventually, the duty cycle, which is the sum of the $d_1(k)$ and $d_2(k)$, is a little bit unsymmetrical during one half line period.



(a) d_1 (b) d_2

Fig. 6 Duty cycle component curves during one half line period

The block diagram of the digital controlled Boost PFC based on the predictive algorithm is shown in Fig. 7. The duty cycles are generated by the predictive algorithm. The rectified voltage v_{in} is sensed for peak value and zero cross signal detection. The peak value of the rectified voltage is used in the predictive algorithm implementation. The reference current, i_{ref}, is from the multiplier. Its amplitude is determined by the output of the PID controller in the voltage loop. Its phase and sinusoidal waveform are determined by the zero cross signal and the sine-wave-look-up-table. The output voltage V_o is controlled by the closed loop using a PID regulator. In this digital control system, the feedback signals are V_o and v_{in}. The output is the gate signal for the switch. Consequently, no current loop is needed in the calculation of the duty cycle, all the duty cycles required to achieve unity power factor in a half line period can be generated in advance with this predictive control strategy. The input voltage feed-forward will discussed in section IV.

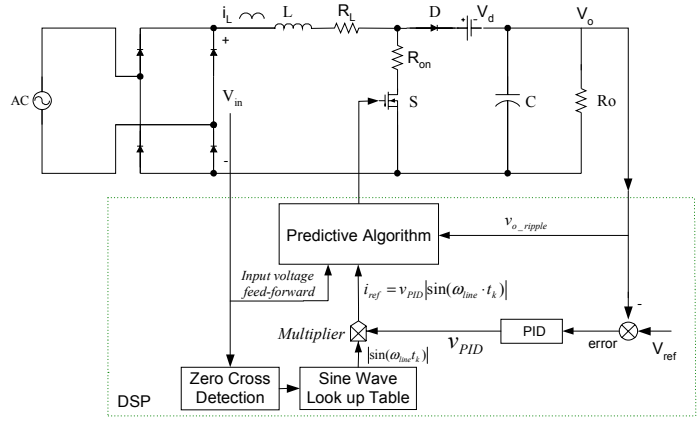


Fig. 7 Digital predictive control with input voltage feed-forward

IV. INPUT VOLTAGE FEED-FORWARD COMPENSATION

In order to achieve better dynamic and steady state characteristics, the input voltage feed-forward is introduced in the predictive algorithm to compensate the duty cycle during every switching cycle, as shown in Fig. 7. Two types of performance can be improved by the input voltage feed-forward: (1) stabilizing the output voltage for the variation of line voltage (2) compensating the calculated duty cycles to guarantee sinusoidal line current when the line voltage has distortion.

In predictive algorithm (7) or (9), the input voltage, $V_{in}(k)=|V_1 sin(\omega_{line} \cdot t(k)|$, is an ideal sinusoidal waveform which is generated based on a lookup table. Therefore, the duty cycle can be calculated in advance. However, the line voltage may be distorted or varied. In the case of input voltage feed-forward, the instantaneous value of input voltage is sensed and used to modify the duty cycle. When the input voltage variation is sensed, the duty cycles, which are generated in advance based on (7), will be updated to be

$$d_{update}(k) = d(k) + \Delta d(k) \tag{14}$$

Where, $d_{update}(k)$, is the duty cycle sent to the gate of MOSFET, and $d(k)$ is the duty cycle calculated by (7). $\Delta d(k)$ is the compensated component

$$\Delta d(k) = \frac{\Delta v_{in}(k)}{V_{ref}} \tag{15}$$

where, $\Delta v_{in}(k)=V_{in}(k)-v_{in}(k)$, is the input voltage variation. $v_{in}(k)$ is the sensed instantaneous value of input voltage. $V_{in}(k)$ is the input voltage used in the predictive algorithm. It is an ideal sinusoidal waveform generated from a lookup table. $\Delta v_{in}(k)$ is the difference between $v_{in}(k)$ and $V_{in}(k)$. It should be noted that the instantaneous value, $v_{in}(k)$, can be stored in the look up table used as the $V_{in}(k)$ in the next half line period. This input voltage compensation can be implemented by a DSP with very low computation requirement.

If the input voltage has harmonics, $v_{in}(k)$ can be expressed as

$$v_{in}(k) = \left| V_1 \sin(\omega_{line} \cdot t_k) + \sum_{i=3,5,\cdots}^{\infty} V_i \sin(i \cdot \omega_{line} \cdot t_k) \right| \tag{16}$$

The variation between the ideal input voltage, $V_{in}(k)$, and the feed-forward input voltage, $v_{in}(k)$, is

$$\Delta v_{in}(k) = \left| V_1 \sin(\omega_{line} \cdot t_k) \right| - \left| V_1 \sin(\omega_{line} \cdot t_k) + \sum_{i=3,5,\cdots}^{\infty} V_i \sin(i \cdot \omega_{line} \cdot t_k) \right| \tag{17}$$

Then the duty cycles can be updated by the input voltage compensation according to (14) and (15). It is noted from the following analysis that the harmonic components of input voltage are applied to the diode.

Substituting (7) into (14), the duty cycles calculated after input voltage feed-forward compensation are derived as

$$d_{update}(k) = \frac{[i_{ref}(k+1) - i_{ref}(k)]}{V_{ref}} \cdot \frac{L}{T_s} + \frac{V_{ref} - \left| V_1 \sin(\omega_{line} \cdot t_k) \right|}{V_{ref}} + \Delta d(k) \tag{18}$$

Fig. 8 shows the average equivalent circuit model of Boost topology [9]. The voltage drop on the diode is

$$v_d(k) = d_{update}(k) \cdot V_o \tag{19}$$

In the stead state, V_o=V_{ref}, the voltage across the diode is derived by substituting (15), (17) and (18) into (19), as

$$v_d(k) = V_{ref} + [i_{ref}(k+1) - i_{ref}(k)] \cdot \frac{L}{T_s} - \left| V_1 \sin(\omega_{line} \cdot t_k) + \sum_{i=3,5,\cdots}^{\infty} V_i \sin(i \cdot \omega_{line} \cdot t_k) \right| \tag{20}$$

It is shown from (20) that the harmonics voltage drops across the diode.

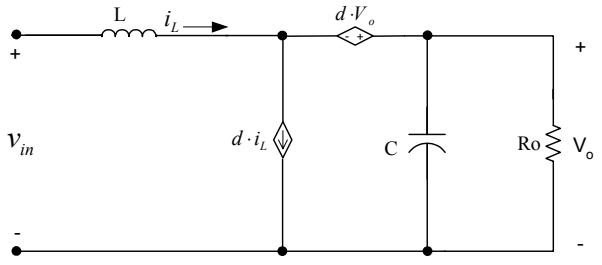


Fig. 8 Average equivalent circuit model of Boost topology

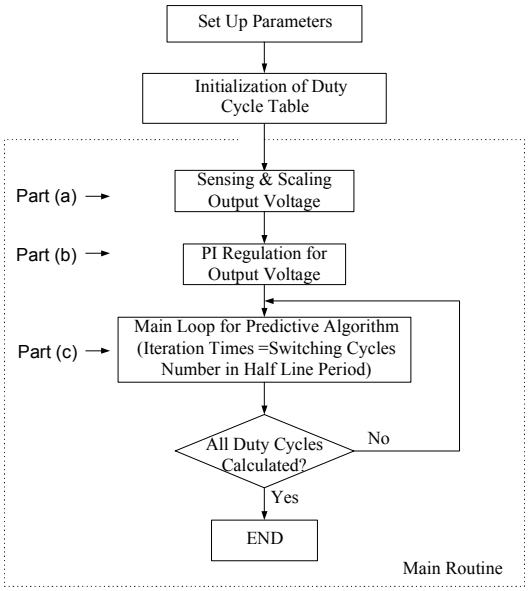
The input voltage feed-forward solves two problems. First, it stabilizes the PFC system and improves its dynamic performance when there is input voltage step change. Therefore, the output voltage is insensitive to the input voltage variation. Second, it can achieve high power factor even when there is distortion in the line voltage. Therefore, the input current can still be sinusoidal under this situation.

V. DSP IMPLEMENTATION

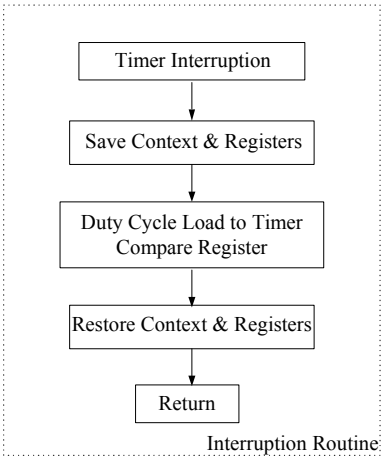
The software flowchart to implement the proposed PFC control method is shown in Fig. 9. The main routine is described in Fig. 9(a). There are mainly three parts in the main routine: (a) output voltage sampling and scaling, (b) PI regulation for output voltage, (c) predictive algorithm implementation for duty cycle calculation. These three operations are performed in every half line period. The calculated duty cycles are stored in the memory of DSP. In the interruption routine, as shown in Fig. 9(b), the duty cycle is loaded from the memory to the timer compare register to generate the gate pulse for the switch of PFC. The interruption service routine is performed in every switching cycle.

The proposed predictive algorithm is implemented by a low cost DSP with Boost circuit as the power stage. The hardware implementation is shown in Fig. 10, which is a Boost circuit controlled by a DSP evaluation board. A 40*MHz*, 16Bit, fixed point DSP is used to achieve the PFC implementation operating at 160*kHz* switching frequency.

The output voltage is sensed and feedback to the DSP via 10bit A/D converter. The feedback output voltage signal is compared with the reference voltage and the difference between them produces the error signal for the voltage regulator. The input voltage is sensed for the zero crossing signal detection and input voltage feed-forward. The gate signal is calculated by the predictive algorithm and provided for the switch via the PWM module inside DSP.



(a)



(b)

Fig. 9 Software flowchart for predictive algorithm implementation

Fig. 10 Boost PFC circuit controlled by DSP evaluation board

VI. SIMULATION AND EXPERIMENTAL RESULTS

The simulation results based on Matlab are shown in Fig11-13. The parameters used in the simulation are: V_{in}=55V(RMS), V_{out}=100V, f_{sw}=160kHz, f_{line}=50Hz, L=1.2mH, I_o=4A(full load). When the output currents are 4A for full load, the input current and voltage waveforms are shown in Fig.11. THD of the input current is 2.31%. Power factor is 0.999. When the output currents are 2A for half load, the input current and voltage waveforms are shown in Fig.12. THD of the input current is 6.05%. Power factor is 0.998. The input current and voltage waveforms are shown in Fig.13 when the input voltage is distorted. In order to make the result obvious, there is only third harmonic in the line voltage. The magnitude of the third harmonic is 10% of the fundamental component. The input current can still remain sinusoidal when the input voltage is distorted. THD of the input current is 5.15%. The power factor under this situation is 0.998.

The experiment results are shown in Fig.14-17. The operating parameters are the same as that used in the simulation. When the output current is 4A for the full load, the input line current and voltage waveform are shown in Fig. 14. The harmonic analysis of input current is shown in Fig. 15. The third and fifth harmonics of line current are about 1.86% and 2.08% of the fundamental component, respectively. THD of line current is 3.1%. Power factor is 0.999.

When the output current is 2A for 50% of the full load, the input line current and voltage waveform are shown in Fig. 16. The harmonic analysis of input current is shown in Fig. 17. The third and fifth harmonics of line current are about 6.04% and 1.80% of the fundamental component, respectively. THD of line current is 7.1%. Power factor is 0.997.The testing results show that the proposed digital control strategy for PFC can achieve near unity power factor in the steady state. It is noted that, the THD for low load is little bit higher that that for full load. This testing result verifies the theoretical analysis in section III.

VII. CONCLUSION

A predictive algorithm is proposed for digital control PFC implementation. Based on the Boost topology, the predictive algorithm is derived. By using this control strategy, all the duty cycles required to achieve unity power factor in a half line period are generated in advance. Because the speed of DSP is no longer the critical factor for high switching frequency PFC by using the proposed control strategy, a low cost DSP can be used to implement PFC operating at high switching frequency.

Simulation results show that, based on the predictive PFC control algorithm, unity power factor can be achieved over wide input voltage and load current range. A prototype of Boost PFC controlled by a DSP evaluation board was built to verify the proposed digital control PFC strategy. Power factor for the full and half load is calculated based on the THD value from FFT analysis. The experimental results show that the power factor over 0.99 can be achieved by using the proposed digital control strategy.

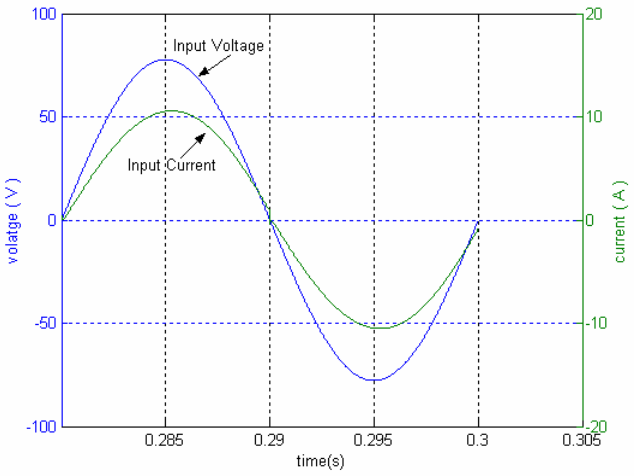


Fig. 11 Input current and voltage waveforms for full load

(Io=4A, THD=2.31%, P. F. = 0.999)

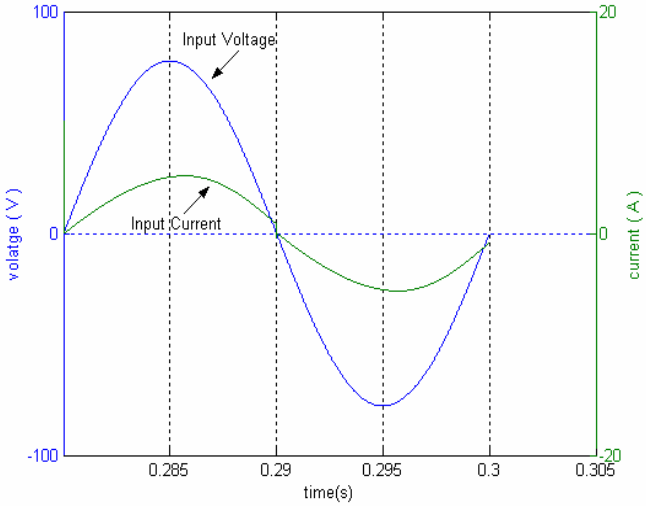


Fig. 12 Input current and voltage waveforms for half load

(Io=2A, THD=6.05%, P. F. = 0.998)

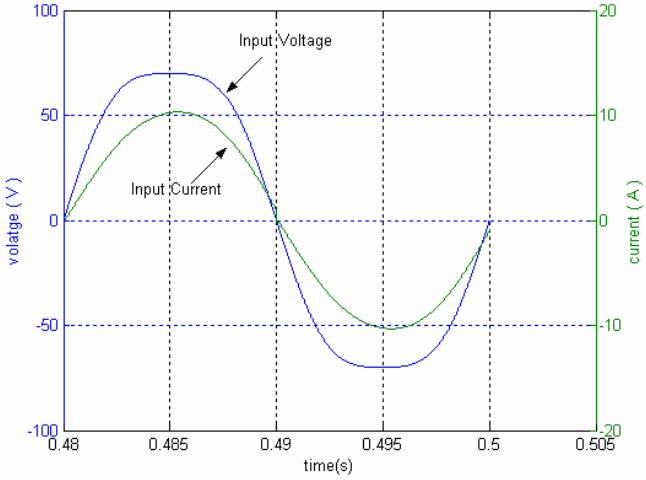


Fig. 13 Input current waveform for distorted input voltage

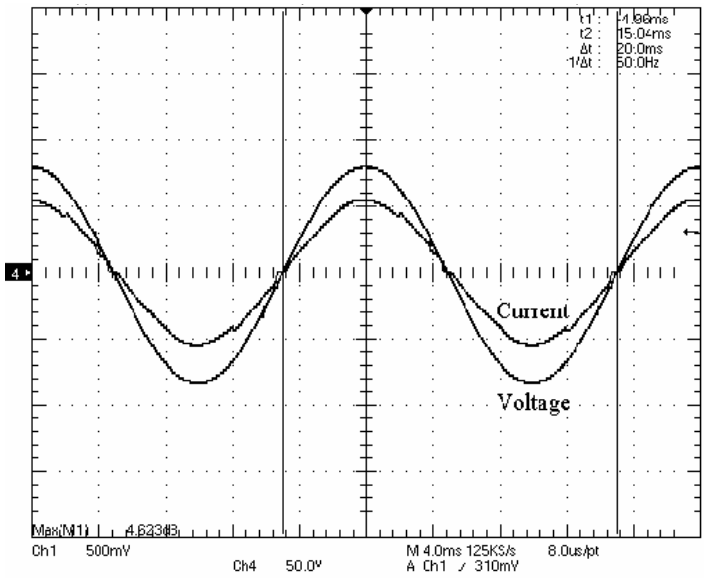


Fig. 14 Line voltage and current waveform (Full Load)

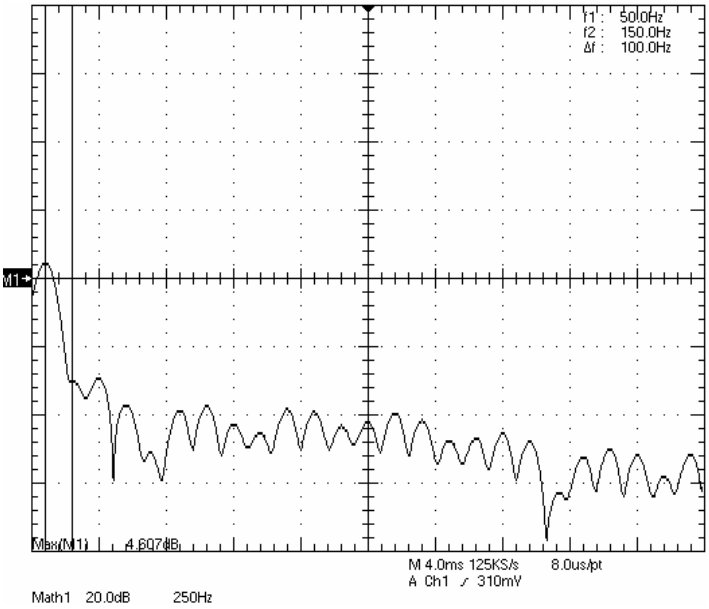


Fig. 15 Harmonic analysis of line current (Full Load)

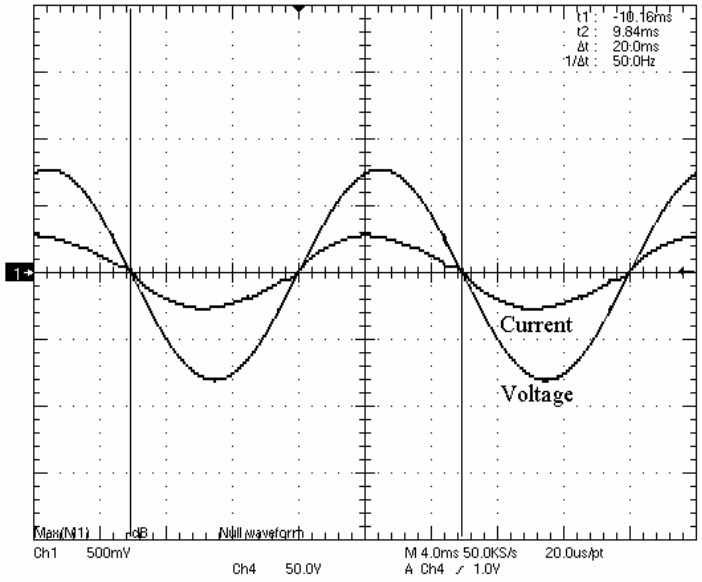


Fig. 16 Line voltage and current waveform (50% Load)

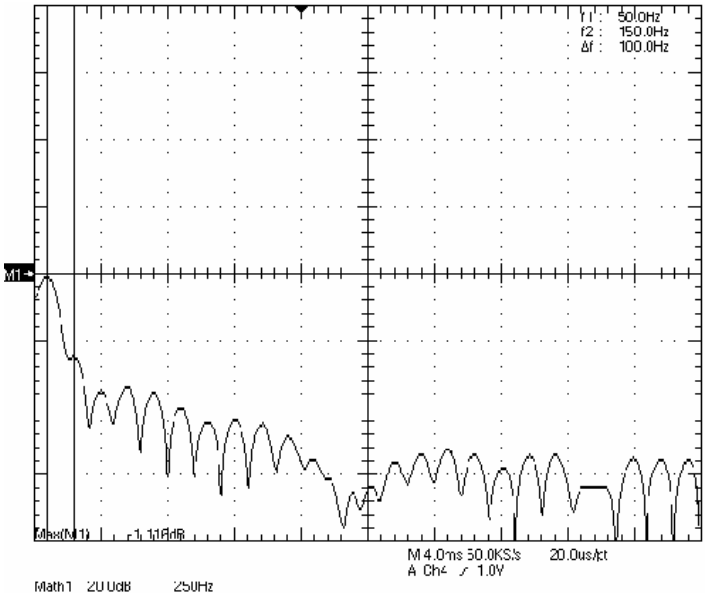


Fig. 17 Harmonic analysis of line current (50% Load)

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