A Digital Power Factor Correction (PFC) Control Strategy Optimized for DSP

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***Abstract*—A predictive algorithm for digital control power factor correction (PFC) is presented in this paper. Based on this algorithm, all of the duty cycles required to achieve unity power factor in one half line period are calculated in advance by digital signal processors (DSPs). A Boost converter controlled by these precalculated duty cycles can achieve sinusoidal current waveform. One main advantage is that the digital control PFC implementation based on this control strategy can operate at a high switching frequency which is not directly dependent on the processing speed of DSP. Input voltage feed-forward compensation makes the output voltage insensitive to the input voltage variation and guarantees sinusoidal input current even if the input voltage is distorted. A prototype of Boost PFC controlled by a DSP evaluation board was set up to implement the proposed predictive control strategy. Both the simulation and experimental results show that the proposed predictive strategy for PFC achieves near unity power factor.**

***Index Terms*—Digital control, power factor correction (PFC), predictive algorithm.**

I. Introduction

POWER factor correction (PFC) is necessary for ac-to-dc switched mode power supply in order to comply with the requirements of international standards, such as IEC-1000–3–2 and IEEE-519. PFC can reduce the harmonics in the line current, increase the efficiency and capacity of power systems, and reduce customers' utility bills. In order to achieve unity power factor in the switched mode power supply, many control methods are explored, including average current control [1], peak current control [2], hysteretic control [3], nonlinear carrier control [4], etc. All of these control methods have been implemented by the analog circuits. Several commercial integrated circuits (ICs) for current mode control, such as UC3854/3855 and ML4824 are available for the PFC applications.

With the development of digital techniques, more and more control algorithms are implemented in power electronics circuits by the digital chips, such as microprocessors or digital signal processors (DSPs). One reason is that digital control can implement more complicated algorithms. Another reason is that digital control has many advantages over analog control, including programmability, adaptability, low part count and reduced susceptibility to environmental variations, etc. In addition, it is possible to achieve better performance in digital implementation than that in analog implementation with the same cost. As a result, it is prudent to explore digital control techniques for PFC application.

Digital control PFC implementations have been explored by many researchers [5]–[7]. Basically, most of the digital implementations for PFC are based on average current mode control. Some works have been done to make the digital control a competitive option to analog controlled PFC implementation. Unfortunately, all of the existing control method cannot take full advantages of the digital technique and the switching frequency of the converter is limited by the speed of the DSP.

A predictive control strategy suitable for digital implementation of PFC is proposed in this paper. The basic idea of the proposed digital control PFC algorithm is that all the duty cycles required to achieve unity power factor in a half line period are calculated in advance by using a predictive algorithm. The proposed PFC control strategy is based on the prediction, not feedback, to achieve power factor correction. By using the proposed method, the switching frequency of the PFC does not directly depend on the processing speed of the digital controller. Therefore, a relatively low cost DSP or microprocessor can be used to realize digital control PFC system operating at high switching frequency.

In this paper, the existing digital control methods for PFC are reviewed, and their limitations are highlighted in Section II. The principle of the predictive control strategy for digital PFC implementation is presented in Section III. In Section IV, the input voltage feed-forward is incorporated with the predictive algorithm to compensate the duty cycles for the purpose of maintaining sinusoidal input current and stabilizing the output voltage when there exist variation and/or distortion in line voltage. The computation requirement for DSP to implement the proposed PFC control algorithm is estimated in Section V. Simulations were performed to verify the digital control PFC strategy in Section VI. In Section VII, the hardware implementation and experimental results are presented. The conclusion is presented in Section VIII.

II. Limitations of the Conventional Digital PFC Control

The switching frequency is limited in the conventional digital control PFC system because of the sampling time delay and the necessary processing time. Average current mode control, which is one of the main conventional analog control strategies, as shown in Fig. 1, is widely used in digital control PFC [5], [6]. In Fig. 1, the average inductor current, i_L, is forced to follow the reference current $i_{\rm ref}$, which is proportional to the rectified

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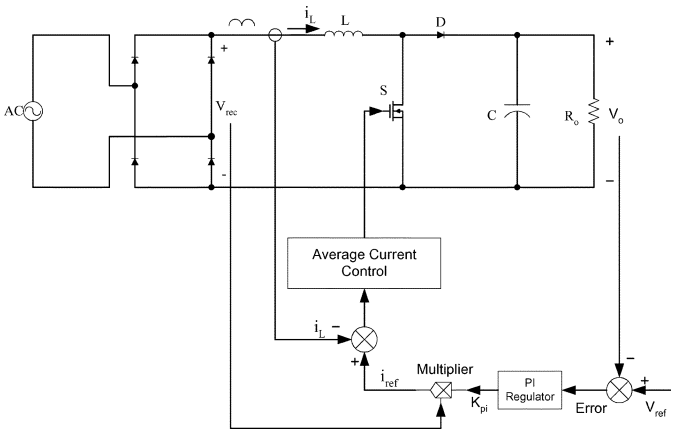

Fig. 1. Average current mode control of Boost PFC.

voltage, so that unity power factor is achieved. In digital implementation of average current mode control, the DSP or microprocessor is used to calculate the duty cycle in every switching cycle T_s based on the feedback current i_L and the reference current $i_{\rm ref}$. The switch S is controlled by the calculated duty cycles to achieve unity power factor. In [7], single sampling in single period method (SSSP) is adopted. A 50-kHz switching gate signal is controlled by the DSP (TMS320F240, 20 MHz). The digital average current mode control was implemented in these PFC applications. The whole process in a digital control PFC based on average current mode control includes a) voltage and current sampling, b) voltage error calculation, c) voltage PI regulation, d) reference current calculation, e) current error calculation, f) current PI regulation, and g) duty cycle generation. It is estimated that 11 arithmetic operations are required in each switching cycle. In addition, other operations are necessary for the pulse-width modulated (PWM) input/output (I/O) port to output the duty cycle. All these operations have to be finished within every switching cycle. Because this process is iteratively running in every switching cycle, the DSP is almost tied up by all these operations and calculations. Therefore, the switching frequency is limited due to the speed limitation of DSP. This disadvantage is common to all existing digital implementations based on average current mode control.

Efforts have been tried to solve the above problems. A digital control method was presented in [8] for the purpose of reducing the computation time and increasing the switching frequency by updating the duty cycles once in several or several tens switching cycles. Using that method, the same duty cycle is applied in several or several tens switching cycles so that the computation requirement for updating the duty cycles is reduced. Unfortunately, the harmonics in the line current are increased in the Boost PFC controlled by that method.

A PFC control method based on DSP, which consists of one open loop and one closed loop paralleling together, was explored in [9]. The open loop determines the duty cycle component based on the input voltage and output voltage. The closed loop parallels with the open loop and determines the second duty cycle component, which is "a small amount of variation depending on load condition." Actually, the construction of the closed loop is the same as that in current mode control. Therefore the duty cycle still had to be calculated in every switching cycle. As a result, its computation requirement is no less than that in the digital implementation based on average current mode control.

In [10], a predictive digital current program control was investigated and used in the implementation of PFC. In that paper, the duty cycle for the next switching period is predicted based on the sampled current, input and output voltage, and duty cycle in the present switching period. Similar to the average current mode control, that control method is also based on the idea that the duty cycle is calculated one by one in every switching cycle. In fact, the computation requirement on DSP is higher than that in digital implementation based on average current mode control.

It is observed from the above analysis that the existed implementations of the digital control PFC have the following limitations. First, the switching frequency is limited due to the sampling, computation and processing time. Even operating at a relatively low switching frequency, the DSP is still tied up by the PFC stage in switched mode power supply (SMPS). In the digital control PFC system, if the switching frequency is 200 kHz, one switching cycle is only 5 μs. If the duty cycle is 0.5, all of the works should be finished by the DSP in 2.5 μs (5 μs$\times$ 0.5). This imposes a very high requirement for the speed of the DSP. Second, the higher the switching frequency, the faster the DSP required. Consequently, the implementation of the digital control method in the PFC application is limited due to the high cost. Third, even if the fastest DSP was used in digital control PFC systems, the switching frequency cannot reach the same level as that in analog controlled PFC systems.

Several control strategy were explored to overcome the above limitations of digital control PFC. The first approach is a digital controller combined with an analog PFC control chip, e.g., UC3854 [11]. That approach uses an analog control IC in the inner loop. The DSP provide the reference current signal to the analog control IC. Using that method, the duty cycle is directly determined by the analog circuit. The DSP only handles the low frequency tasks for the outer voltage loop. Therefore, the switching frequency does not depend on the speed of DSP and high switching frequency can be achieved. However, its control structure is complicated, and the cost is increased as both analog chip and DSP are required. The second approach is using a FPGA combined with an analog to digital converter (ADC) [12], [13]. A simple PFC control algorithm, which is actually "a digital version of charge control," is specifically designed to be suitable for FPGA in that implementation. The switch turns "on" at the beginning of every switching period and "off" when the mean value of input current reaches the reference value. The mean value of input current is the sum of the input current samples divided by the number of samples in one switching cycle. In order to guarantee the resolution of the duty cycles, a fast ADC is required in the integral operation for the calculation of input current mean value. This increases the cost of the control system. Furthermore, there is a tradeoff between the switching frequency and the duty cycles resolution. Hence, the switching frequency is limited in that method because the duty cycle resolution should be remained at a satisfactory level. A digital offline control technique, named stored-duty-ratio (SDR) control, was proposed in [14] and [15]. In that method, the duty cycles are calculated in advance based on the power balance equation of Boost topology. Those calculated duty cycles are stored in the memory and used to control the switch to achieve PFC. Because the duty cycles are calculated

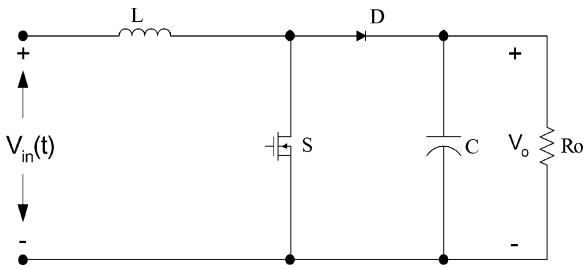

Fig. 2. Boost converter topology.

offline, neither current sensing, input voltage sensing, nor CPU is required in that method. In "uncontrolled version of SDR control," there is only one set of stored duty cycles to control the switch. Therefore, there is only one operating point at which the input current could exactly follow the sinusoidal waveform. This is because the offline duty cycle calculation is based on one specific operating point. In "controlled version of SDR control," there are eight sets of stored duty cycles to control the switch. Therefore, there are only eight operating points at which the input current could exactly follow the sinusoidal waveform. This is because the offline duty cycle calculation is based on eight specific operating points. Because of the limitation of the above offline calculation, that method can achieve the power factor over 0.99 only in a very narrow input voltage range (200–225 V) [14], which is close to the operating points used in the offline duty cycles calculation.

This paper proposes a new digital control strategy to achieve PFC implementation. Different from the offline stored-duty-ratio (SDR) control in [14] and [15], the proposed online PFC control method can guarantee the sinusoidal current waveform under the distorted input voltage condition and wide input voltage range because input voltage feed-forward is introduced in the proposed PFC control algorithm. At the same time, different from the digital PFC implementation based on conventional average current control, there is only voltage loop, no current loop in the proposed PFC control algorithm. The sinusoidal current waveform is guaranteed by the predictive algorithm, not current feedback control.

III. Principle of Predictive PFC Control Strategy

The topology of Boost converter is shown in Fig. 2. The proposed predictive PFC algorithm is derived based on the following assumptions.

1) Boost converter operates at continuous conduction mode.
2) The switching frequency is much higher than the line frequency, so the input voltage $V_{\rm in}$ can be assumed as a constant during one switching cycle.

Based on these assumptions, when the switch S is on or off, the circuit of Fig. 3(a) or (b) are obtained and the inductor current can be described as (1) and (2), respectively

$$L\frac{di_L}{\mathrm{dt}} = V_{\rm in} \quad t_k \le t < t_k + d_k T_s \tag{1}$$

$$L\frac{di_L}{dt} = V_{\rm in} - V_o \quad t_k + d_k T_s \le t < t_{k+1}. \tag{2}$$

The discrete form for the inductor current at the beginning of $(k+1)\mathrm{th}$ switch cycle in term of the inductor current at the

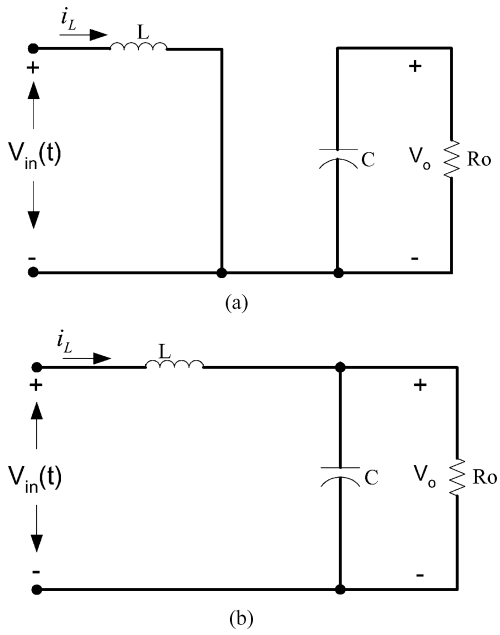

Fig. 3. Boost converter circuit: (a) switch is on and (b) switch is off.

beginning of $k\mathrm{th}$ switching cycle can be derived from (1) and (2) as

$$i_L(k+1) = i_L(k) + \frac{V_{\rm in}(k)\cdot T_s}{L} - \frac{V_o(k)\cdot(1-d(k))\cdot T_s}{L} \tag{3}$$

where $d(k)$ and T_s are the duty cycle and switching period. $V_{\rm in}(k)$ is the input voltage in $k^{\rm th}$ switching cycle. $i_L(k)$, $i_L(k+1)$ are the inductor current at the beginning of $k^{\rm th}$ and $(k+1)^{\rm th}$ switching cycles, respectively.

When PFC is achieved, the inductor current should follow the reference current $i_{\rm ref}(k)$, which is proportional to the rectified input voltage, as shown in Fig. 4. At the same time, the output voltage should follow the reference voltage $V_{\rm ref}$. That is

$$V_o(k) = V_{\rm ref} \tag{4}$$

$$i_L(k+1) = i_{\rm ref}(k+1) \tag{5}$$

$$i_L(k) = i_{\rm ref}(k). \tag{6}$$

Substituting (4)–(6) into (3), the duty cycle in $k\mathrm{th}$ switching period $d(k)$ can be calculated as

$$d(k) = \frac{V_{\rm ref} - V_{\rm in}(k)}{V_{\rm ref}} + \frac{[i_{\rm ref}(k+1) - i_{\rm ref}(k)]\cdot\frac{L}{T_s}}{V_{\rm ref}} \tag{7}$$

where

$$i_{\rm ref}(k) = v_{\rm PID}\cdot\left|\sin(\omega_{\rm line}\cdot t_k)\right|. \tag{8}$$

$v_{\rm PID}$ is the output of the PID regulator. It is determined by the closed voltage loop. $|\sin(\omega_{\rm line}\cdot t_k)|$ is the rectified sinusoidal waveform with the line frequency. In DSP implementation, this sinusoidal waveform is stored in a look up table. It should be noted from (8) that $v_{\rm PID}$ has an exact physics meaning that is the peak value of the reference current. In DSP implementation, the limitation value of the PID regulator is easily determined based on the rated load according to this physics meaning.

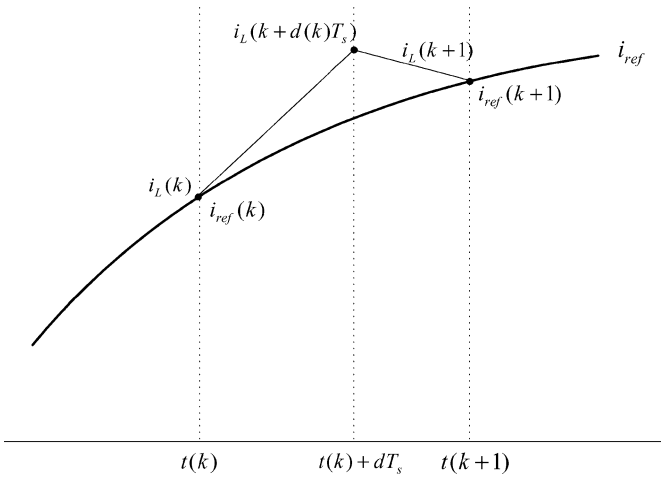

Fig. 4. Input current waveform and reference current in one T_s.

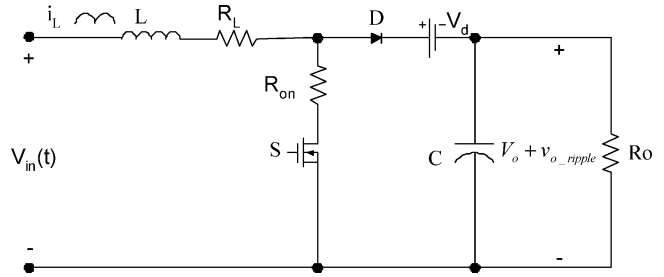

Fig. 5. Accurate model of Boost converter.

The predictive algorithm (7) can be used to generate the duty cycles and achieve near unity power factor in the implementation of PFC with Boost topology. In order to improve the inductor current waveform further, a more accurate model, as shown in Fig. 5, is used to predict the required duty cycles. In this model, the impacts of the inductor winding resistance R_L, the on resistance of switch $R_{\rm on}$, the voltage drop across diode V_d, and the output voltage ripple $v_{\rm o\_ripple}$, are considered.

Based on the model in Fig. 5, the duty cycles can be derived as

$$d(k)=\frac{(V_{\rm ref}+v_{\rm o\_ripple}(k)+V_d)+R_L i_{\rm ref}(k)-v_{\rm in}(k)}{(V_{\rm ref}+v_{\rm o\_ripple}(k)+V_d)-R_{\rm on}i_{\rm ref}(k)} +\frac{[i_{\rm ref}(k+1)-i_{\rm ref}(k)]\cdot\frac{L}{T_s}}{(V_{\rm ref}+v_{\rm o\_ripple}(k)+V_d)-R_{\rm on}i_{\rm ref}(k)} \quad (9)$$

where $v_{\rm o\_ripple}$ can be estimated as

$$v_{\rm o\_ripple}(k)=-I_o\times\frac{1}{2\omega_{\rm line}C}\sin(2\omega_{\rm line}t_k) \quad (10)$$

where I_o is the load current. Equations (7) and (9) are the predictive algorithms, which is used to implement power factor correction in this paper. The modeling topologies in Figs. 2 and 5 are used to derive the duty cycle calculation algorithm because the derived (7) and (9) have the simple forms, require low calculation for digital implementation and the test results are good enough. The switching delay and switching loss are not included in the model because the consideration of them would make the algorithm too complicated to be implemented.

The proposed digital control strategy for PFC is actually a "valley tracking reference current algorithm." It is the valley values of current $i_L(k)$ and $i_L(k+1)$ that are forced to track the reference current, $i_{\rm ref}$, as shown in Fig. 4. Theoretically, the mean value of the inductor current in every switching cycle should follow the reference current. Hence, there is an approximation in the predictive algorithm (7) and (9). If the inductor current ripple in one switching cycle can be neglected compared with the amplitude of inductor current, the proposed control algorithm works well. This approximation condition is easier to be satisfied for high load than that for light load. In the simulation and experimental results of Sections VI and VII, the power factor for light load is a little bit less than that for high load because of this approximation.

Further investigation to the proposed predictive PFC algorithm is necessary to understand the philosophy behind it. Actually, there are two components in (7), expressed as

$$d(k)=d_1(k)+d_2(k). \quad (11)$$

The first component $d_1(k)$ is

$$d_1(k)=\frac{V_{\rm ref}-v_{\rm in}(k)}{V_{\rm ref}}. \quad (12)$$

This component is determined by the input and output voltage equilibrium of Boost topology. Therefore, d_1 is defined as voltage equilibrium component (VEC). In the practical PFC system, d_1 is not enough due to the following two reasons. First, it can't realize the regulation of the output voltage because it is determined by the open loop parameters. Second, it cannot achieve the unity power factor either, because the practical issues, such as the energy stored in or released from the inductor, are not considered.

The second component $d_2(k)$ is expressed as

$$d_2(k)=\frac{[i_{\rm ref}(k+1)-i_{\rm ref}(k)]\cdot\frac{L}{T_s}}{V_{\rm ref}}. \quad (13)$$

This component is named as current forcing component (CFC) because the numerator of (13) is the inductor current differentiation in one switching cycle $V_L(t)=L(di_L(t)/dt)\approx(L/T_s)[i_L(k+1)-i_L(k)]$. Therefore, this part actually has cosine shape. The integral of $V_L(t)$ to time is the inductor current, $i_L=(1/L)\int V_L(t)dt$, which is in sinusoidal shape. d_2 is related to the voltage feedback because the amplitude of the reference current $i_{\rm ref}$ is determined by the PID regulator, referring to (8). After d_2 is introduced, not only the output voltage can be regulated to follow the reference, but also the line current can achieve sinusoidal waveform.

Under the parameters of $V_{\rm in}=220$ V(RMS), $V_{\rm out}=400$ V, $P_{\rm load}=1000$ W, $f_{\rm sw}=160$ kHz, $f_{\rm line}=50$ Hz and $L=1.2$ mH, the curves of d_1 and d_2 in one half line period are shown in Fig. 6(a) and (b), respectively. In Fig. 6(a), the minimum value of d_1 is determined by the reference voltage $V_{\rm ref}$ and the peak value of the input voltage. In Fig. 6(b), the peak-to-peak value of d_2 is regulated by the output of the PID controller. Eventually, the duty cycle, which is the sum of the $d_1(k)$ and $d_2(k)$, is a little bit unsymmetrical during one half line period.

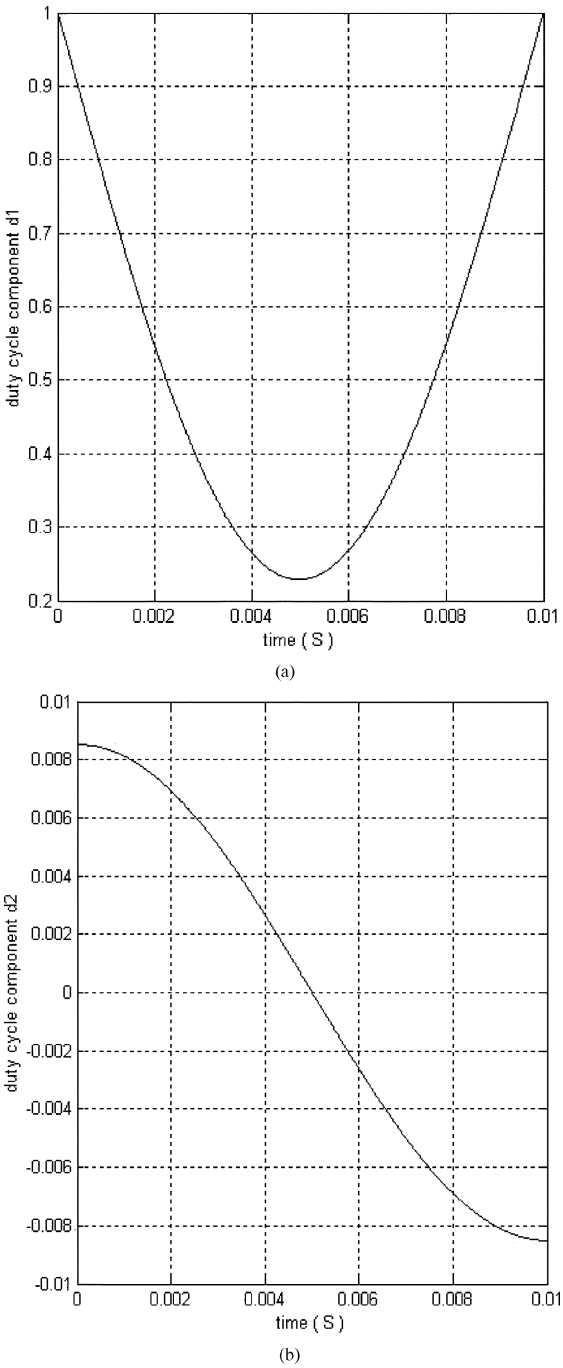

Fig. 6. Duty cycle component curves during one half line period (a) d_1 and (b) d_2.

The block diagram of the digital controlled Boost PFC based on the predictive algorithm is shown in Fig. 7. The duty cycles are generated by the predictive algorithm. The rectified voltage $v_{\rm in}$ is sensed for peak value and zero cross signal detection. The peak value of the rectified voltage is used in the predictive algorithm implementation (Note that the input voltage feed-forward in Fig. 7 will be introduced in Section IV). The reference current, $i_{\rm ref}$, is from the multiplier. Its amplitude is determined by the output of the PID controller in the voltage loop. Its phase and sinusoidal waveform are determined by the zero cross signal and the sine-wave-look-up-table. The output voltage V_o is controlled by the closed loop using a PID regulator. In this digital control

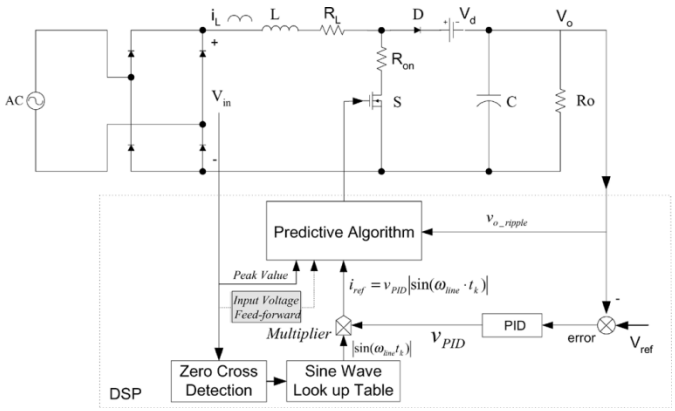

Fig. 7. Diagram of digital predictive control for Boost PFC.

system, the feedback signal is V_o. The output of the digital control system is the gate signal for the switch S. Consequently, no current loop is needed for the duty cycle calculation. All the duty cycles required to achieve unity power factor in a half line period can be generated in advance by using this predictive control algorithm.

IV. Input Voltage Feed-Forward Compensation

In order to achieve better dynamic and steady state characteristics, the input voltage feed-forward is introduced in the predictive algorithm to compensate the duty cycle during every switching cycle, as shown in Fig. 7. Two types of performance can be improved by the input voltage feed-forward: 1) stabilizing the output voltage for the variation of line voltage and 2) compensating the calculated duty cycles to guarantee sinusoidal line current when the line voltage has distortion.

In predictive algorithm (7) or (9), the input voltage $V_{\rm in}(k) = |V_1 \sin(\omega_{\rm line} \cdot t_k)|$ (V_1 is the peak value of the input voltage) is an ideal sinusoidal waveform which is generated based on a lookup table. Therefore, the duty cycle can be calculated in advance. However, the line voltage may be distorted or varied. In the case of input voltage feed-forward, the instantaneous value of input voltage is sensed and used to modify the duty cycle. When the input voltage variation is sensed, the duty cycles, which are generated in advance based on (7), will be updated to be

$$d_{\rm update}(k) = d(k) + \Delta d(k) \tag{14}$$

where $d_{\rm update}(k)$ is the duty cycle sent to control the gate of MOSFET, and $d(k)$ is the duty cycle calculated by (7). $\Delta d(k)$ is the compensated component

$$\Delta d(k) = \frac{\Delta v_{\rm in}(k)}{V_{\rm ref}} \tag{15}$$

where $\Delta v_{\rm in}(k) = V_{\rm in}(k) - v_{\rm in}(k)$ is the input voltage variation. $v_{\rm in}(k)$ is the sensed instantaneous value of input voltage. $V_{\rm in}(k)$ is the input voltage used in the predictive algorithm. It is an ideal sinusoidal waveform generated from a lookup table. It should be noted that the instantaneous value $v_{\rm in}(k)$ can be stored in the look up table used as the $V_{\rm in}(k)$ in the next half line period. This input voltage compensation can be implemented by a DSP with very low computation requirement.

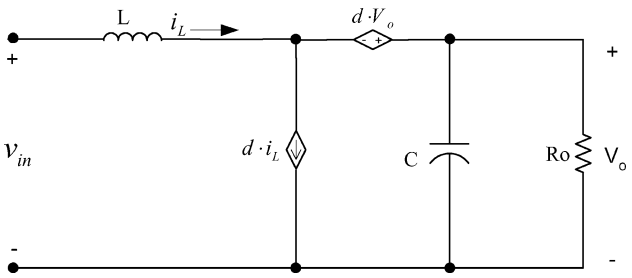

Fig. 8. Average equivalent circuit model of Boost topology.

If the input voltage has harmonics, $v_{\text{in}}(k)$ can be expressed as

$$v_{\text{in}}(k) = \left| V_1 \sin(\omega_{\text{line}} \cdot t_k) + \sum_{i=3,5,\ldots}^{\infty} V_i \sin(i \cdot \omega_{\text{line}} \cdot t_k) \right|. \tag{16}$$

The variation between the ideal input voltage $V_{\text{in}}(k)$ and the feed-forward input voltage $v_{\text{in}}(k)$ is

$$\Delta v_{\text{in}}(k) = |V_1 \sin(\omega_{\text{line}} \cdot t_k)| - \left| V_1 \sin(\omega_{\text{line}} \cdot t_k) + \sum_{i=3,5,\ldots}^{\infty} V_i \sin(i \cdot \omega_{\text{line}} \cdot t_k) \right|. \tag{17}$$

Then, the duty cycles can be updated by the input voltage compensation according to (14) and (15). It is noted from the following analysis that the harmonic components of input voltage are applied to the diode.

Substituting (7) into (14), the duty cycles calculated after input voltage feed-forward compensation are derived as

$$d_{\text{update}}(k) = \frac{[i_{\text{ref}}(k+1) - i_{\text{ref}}(k)]}{V_{\text{ref}}} \cdot \frac{L}{T_s} + \frac{V_{\text{ref}} - |V_1 \sin(\omega_{\text{line}} \cdot t_k)|}{V_{\text{ref}}} + \Delta d(k). \tag{18}$$

Fig. 8 shows the average equivalent circuit model of Boost topology [16]. The voltage drop on the diode is

$$v_d(k) = d_{\text{update}}(k) \cdot V_o. \tag{19}$$

In the steady state, $V_o = V_{\text{ref}}$, the voltage across the diode is derived by substituting (15), (17), and (18) into (19), as

$$v_d(k) = V_{\text{ref}} + [i_{\text{ref}}(k+1) - i_{\text{ref}}(k)] \cdot \frac{L}{T_s} - \left| V_1 \sin(\omega_{\text{line}} \cdot t_k) + \sum_{i=3,5,\ldots}^{\infty} V_i \sin(i \cdot \omega_{\text{line}} \cdot t_k) \right|. \tag{20}$$

It is shown from (20) that the harmonics voltage drops across the diode. This is verified by the experimental results in Section VII, Fig. 20.

The input voltage feed-forward solves two problems. First, it stabilizes the PFC system and improves its dynamic performance when there is input voltage step change. Therefore, the output voltage is insensitive to the input voltage variation. Second, it can achieve high power factor even when there is distortion in the line voltage. Therefore, the input current can still be sinusoidal under this situation.

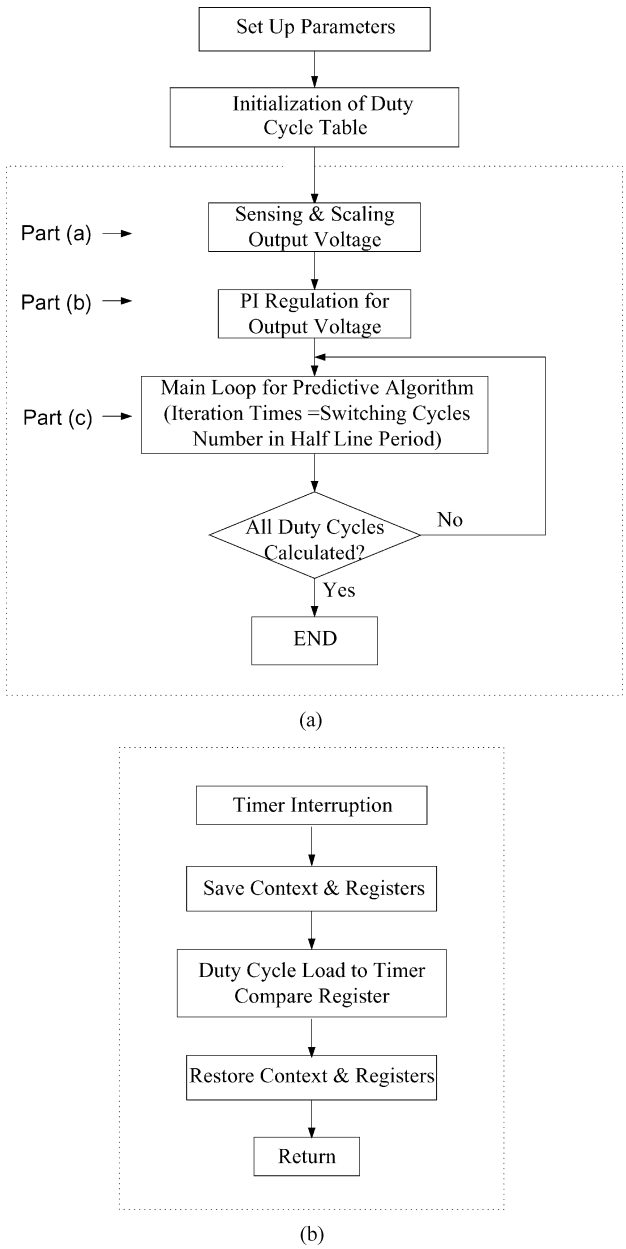

Fig. 9. Software flowchart for predictive algorithm implementation: (a) main routine and (b) interruption routine.

V. Computation Requirement Estimation

In this section, the computation requirement to implement the proposed control strategies is estimated.

It is observed from the software flowchart, as shown in Fig. 9(a), there are mainly three time consumption parts in the main routine for DSP to achieve the PFC control strategy: a) output voltage sampling and scaling, b) PI regulation for output voltage, and c) predictive algorithm implementation for duty cycle calculation. For part a), all the operations needed are scaling the value from analog-to-digital converter (A/D) and addressing the memory in a typical DSP system. If the sampling

frequency is 6.4 kHz for voltage loop and line frequency is 50 Hz, only 64 sample points are performed in one half line period (10 mS). It should be noted that 6.4 kHz sampling frequency is enough for the voltage loop, in which the bandwidth is only about $5 \sim 20$ Hz for PFC. For part b), the PI regulation is implemented only once in one half line period because the average value of the output voltage in one half line period is used to close the loop. For part c), the calculation for duty cycles by the predictive algorithm will be iterated till all the duty cycles in one half line period are updated. So compared to part a) and b), the predictive algorithm implementation loop [part c)] takes up most of computation time in the main routine process.

The requirement of the instruction cycles for part c), predictive algorithm implementation, is estimated here. It is noted in (9) that

$$0 \le d(k) \le 1 \tag{21}$$

and the denominator in (9) can be approximated as a constant $(V_{\text{ref}} + V_d)$. So the duty cycle calculated from (9) can be obtained directly from the value of the numerator. It is also noted that L/T_s is used as a constant. Hence, only eight operations, which are required just for the calculation of the numerator, are required in calculation of the duty cycle. For (10), $(1/2\omega_{\text{line}}C)\sin(2\omega_{\text{line}}t_k)$ is processed as one component and it can be obtained from the look up table. Therefore, only one multiplication operation is required to calculate the voltage ripple. So the total operation number of the calculation for one duty cycle is 9. For a DSP with the hardware multiplier, typically, each multiplication can be obtained by four instruction cycles: 1) two cycles for data addressing for operands of multiplication, 2) one cycle for arithmetic operation, and 3) one cycle for the data addressing for the product. Similarly, four instructions are required for each addition. Therefore, for every duty cycle, the required instructions number $T_{\text{each\_duty}}$ is

$$T_{\text{each\_duty}} = 4 \times 9 = 36. \tag{22}$$

If the Boost PFC preregulator operates at 160 kHz switching frequency and the input line frequency is 50 Hz, there are 1,600 switching cycles in one half line period. In the DSP controlled PFC based on this predictive algorithm, the instruction cycles, $T_{\text{all\_duty}}$, required for the calculation of all these 1,600 duty cycles is

$$T_{\text{all\_duty}} = 36 \times 1600 = 57\,600. \tag{23}$$

Because part a) and b) are not included and some other operations maybe missed in the above estimation, 50% instruction cycle margin is added over $T_{\text{all\_duty}}$ from (23). Then, the instruction cycle requirement for the whole main routine $T_{\text{main\_routine}}$ is

$$T_{\text{main\_routine}} = (1 + 50\%) \times 57\,600 \approx 90\,000. \tag{24}$$

Timer interruption service routine (TISR) is the second important part for time consumption, as shown in Fig. 9(b). In DSP implementation, the gate signal is from the PWM output port which is controlled by the timer compare interruption. The duty cycle is controlled by the data in the timer compare register. This data is updated according to the precalculated lookup table during every switching cycle. The input voltage feed-forward is also performed in the TISR. 40 instruction cycles are required for each TISR operation. In one half line period for 50-Hz line frequency, we iterated 1,600 TISR for 160-kHz switching frequency. So, the instruction cycles required for all TISR in one half line period T_{TISR} is

$$T_{\text{TISR}} = 40 \times 1600 = 64\,000. \tag{25}$$

In one half line period, the total instruction cycle requirement including the main routine and TISR, T_{total}, is

$$T_{\text{total}} = 90\,000 + 64\,000 = 154\,000. \tag{26}$$

The CPU requirement can be estimated from the point view of every switching cycle. For 160 kHz switching frequency, the switching cycle T_{sw} is

$$T_{\text{sw}} = \frac{1}{160 \times 10^3} = 6.25\ \mu\text{s}. \tag{27}$$

If the 154 000 instruction cycles averagely performed in every T_{sw}, the computation time required for a 40-MHz DSP, T_{required}, is

$$T_{\text{required}} = \frac{154\,000}{1600} \times \frac{1}{40 \cdot 10^6} \approx 2.5\ \mu\text{s} < 6.25\ \mu\text{s}. \tag{28}$$

In fact, these 154 000 instruction cycles are not averagely performed in every switching cycle. The predictive algorithm continuously calculates the duty cycles. Once the interruption happens, the main routine for duty cycle calculation is suspended and TISR is performed. The operation returns from interruption service routine to the main routine when the TISR is finished. After all the duty cycles are calculated and stored in the look up table, the DSP operation will focus on TISR, and no operation is needed for the main routine.

From the point view of every half line period, about 154 000 instruction cycles are required to implement the predictive algorithm. On the other hand, for a 40 MIPS, 16 b, fixed point DSP, 400 000 instruction cycles can be completed in one half line period. Therefore, the capability of the DSP has enough margin for the calculation requirement. The speed of DSP is no longer the critical factor for high switching frequency.

VI. Simulation Results

Simulation is performed by MATLAB to verify the proposed digital PFC control algorithm. The input voltage, output voltage and full load used in the simulation are $V_{\text{in}} = 55$ V(RMS), $V_{\text{out}} = 100$ V, and $P_{\text{load}} = 400$ W. The other parameters are the same as that used in Section III.

Fig. 10(a) is the input current of the PFC Boost circuit for 400-W load (full load) at input voltage of 55 V (RMS). Fig. 10(b) is the harmonic components in the current waveform. For the full load, the third harmonic component is only 0.2147A. The THD of the current is 2.29%. The proposed PFC control strategy can achieve the power factor as 0.9997.

The power factor for different loads at input voltages of 55 V (RMS) are shown in Fig. 11. It is shown that the power factor is over 0.99 with the range from 25% to full load. The power

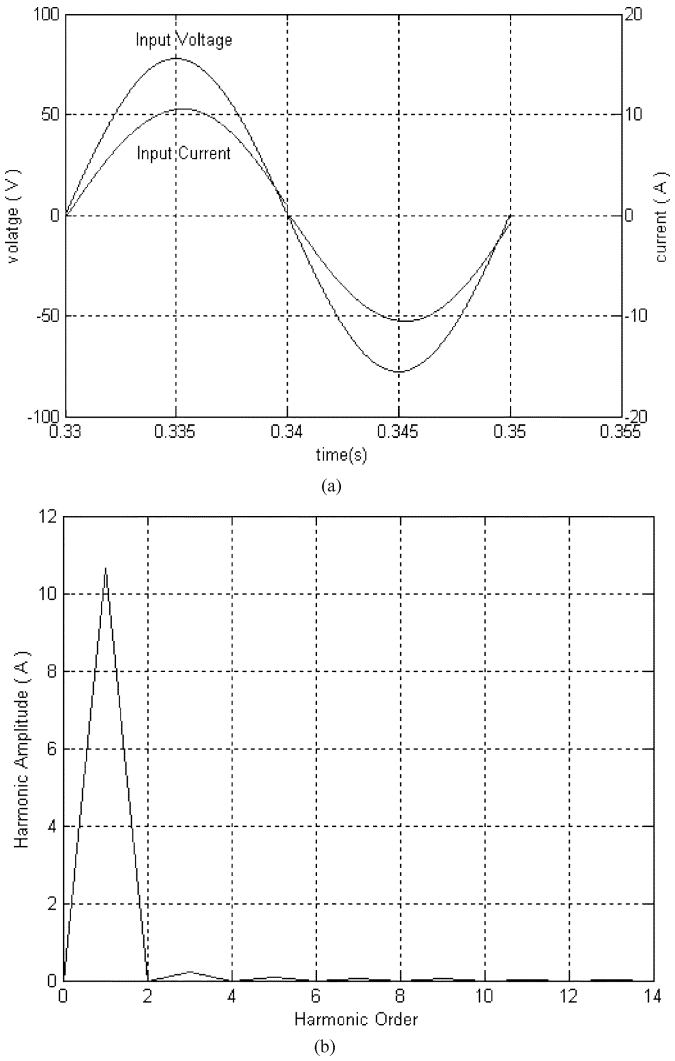

Fig. 10. Input current waveform and its harmonic components (a) input current and voltage waveform and (b) harmonic components of input current.

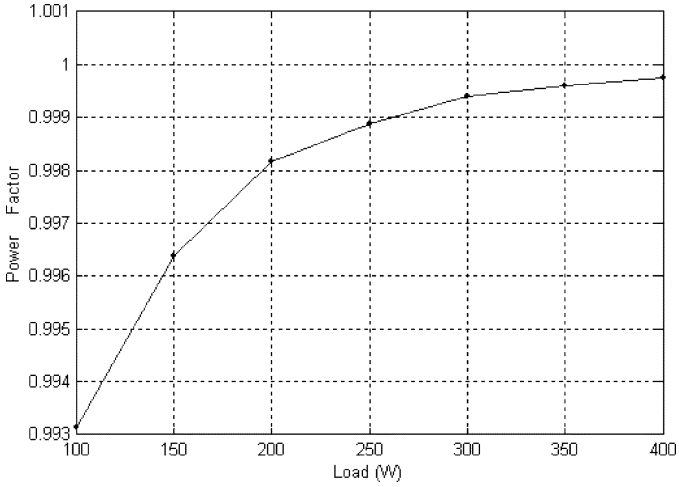

Fig. 11. Power factor for different loads ($V_{\rm in} = 55$ V).

factor for light load is a little bit less than that for high load due to the approximation in the derivation of predictive algorithm (7) and (9).

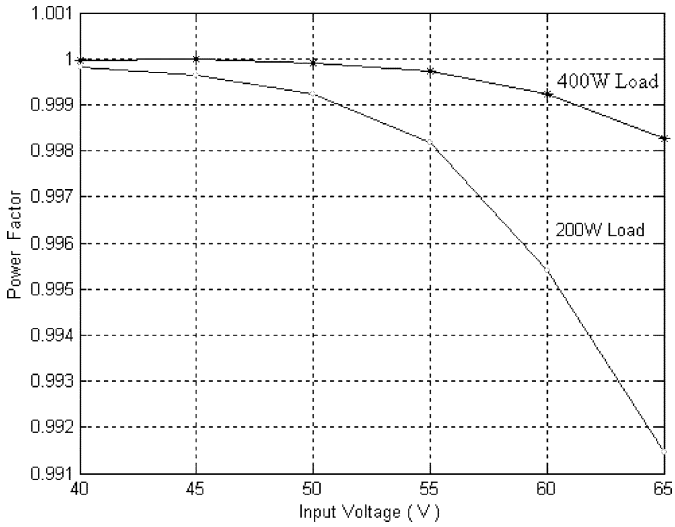

Fig. 12. Power factor at different input voltages.

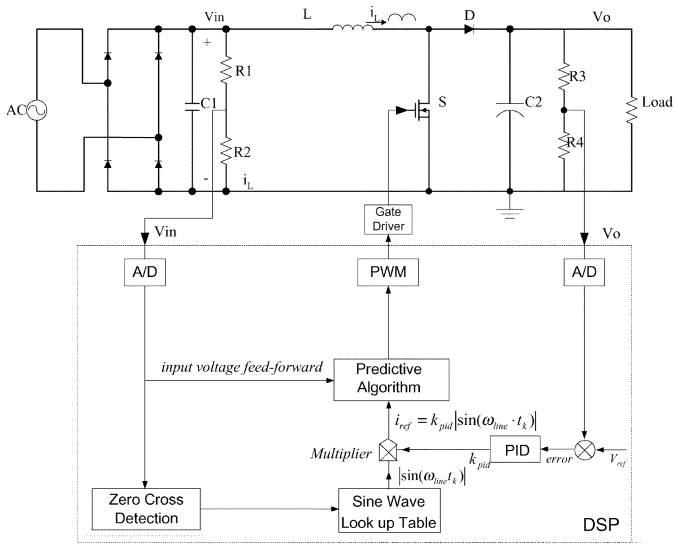

Fig. 13. Diagram of hardware implementation.

The power factor for full load of 400 W and half load of 200 W at different input voltages is shown in Fig. 12. The power factor is always over 0.99 at input voltage range from 40 to 65 V(RMS). It can be found that the power factor at high input voltage low current is a little bit less than that at low input voltage high current, but still over 0.99. It is verified that the proposed PFC control strategy works well for wide input voltage and load current range.

VII. Hardware Implementation and Experimental Results

The new digital control PFC strategy based on predictive algorithm can be implemented by a low cost DSP with Boost circuit as the power stage. The hardware implementation is shown in Fig. 13.

The output voltage is sensed and fedback to the DSP via 10-b A/D converter. The feedback output voltage signal is compared with the reference voltage and the difference between them produces the error signal for the voltage regulator. The input voltage is sensed for the zero crossing signal detection and input voltage

Fig. 14. Boost PFC circuit controlled by DSP evaluation board.

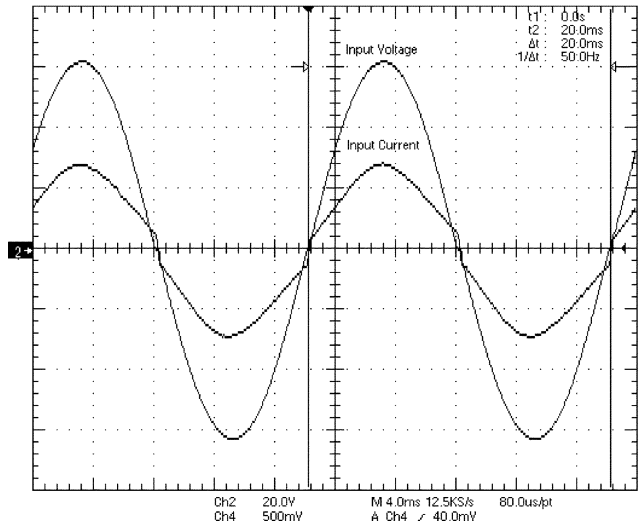

Fig. 15. Line current and voltage waveforms ($V_{\rm in} = 45$ V, $P_{\rm load} = 400$ W, $P.F. = 0.997, THD = 7.3\%$).

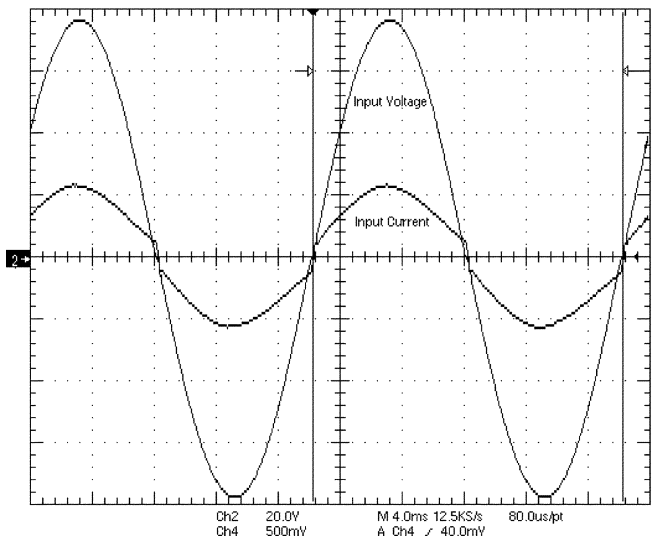

Fig. 16. Line current and voltage waveforms ($V_{\rm in} = 55$ V, $P_{\rm load} = 400$ W, $P.F. = 0.996, THD = 8.5\%$).

feed-forward. The gate signal is calculated by the predictive algorithm and provided for the switch via the PWM module inside DSP. A Boost circuit controlled by a DSP evaluation board is shown in Fig. 14.

In the hardware implementation, the main component values of the Boost circuit are $L = 1.2$ mH, output filter capacitor $C = 2200\ \mu$F. The switch is MOSFET IRFS37N50A, and the diode is SDT12S60. The test operating parameters are chosen as rated input voltage $V_{\rm in} = 55$ V(RMS), output power $P_{\rm load} = 400$ W(full load), output voltage $V_{\rm out} = 100$ V, switching frequency $f_{\rm sw} = 160$ kHz and line frequency $f_{\rm line} = 50$ Hz. For the proof of concept, the input/output voltage are selected as "55 V(RMS)/100 V" in order to minimize the impact of practical problems. As compared with "220 V(RMS)/400 V" implementation, the input current would be the same if the load current is same. A1.2-mH inductor used in the implementation is for the purpose of reducing the ripple current. In practical design, smaller inductor can be used.

In the PFC implementation, the bandwidth of voltage loop should be much lower than the double line frequency (100 Hz). Otherwise, the inductor current waveform would be distorted and the harmonic current would be increased. In this paper, a proportional-integral (PI) regulator is used in the voltage loop. The proportional and integral coefficient parameters are designed, respectively, to satisfied with the bandwidth requirement as $k_p = 10$ and $k_i = 500$. The sampling frequency for voltage loop is chosen as 6.4 kHz. The bandwidth of the voltage loop is about 10 Hz.

In practical implementation, soft-start and protection should be also considered. The conventional resistive method can be used for soft-start. When the Boost circuit starts, the resistor with an appropriate rating is connected in series with the main power circuit. This resistor is shorted after the output capacitor is charged. In the implementation, the inductor current is sensed and compared with an over-current protection level. Once the sensed inductor current is higher than that level. A protection logic signal is generated and used to turn off the gate signal. At the same time, this protection logic signal is transferred to DSP so that the protection mode routine is activated. Over-voltage protection can be done in DSP software routine as both the output and input voltage are sensed. Once over-voltage condition is detected, the Boost converter is shut down.

The experimental results in the steady state for different input voltage and output power are shown in Figs. 15–18. When the output power is 400 W (output current $I_o = 4$ A), the input line current and voltage waveforms at input voltage of 45 V are shown in Fig. 15. The power factor under this operating condition is 0.997 (THD $= 7.3\%$). The input line current and voltage waveforms at input voltage of 55 V are shown in Fig. 16. The power factor under this operating condition is 0.996 (THD $= 8.5\%$). The input line current and voltage waveforms at input voltage of 65 V are shown in Fig. 17. In channel 2 of Fig. 17, 50 V/division is used to show the whole input voltage waveform (this is different from that in Figs. 15 and 16). The power factor under this operating condition is 0.994 (THD $= 10.6\%$). It is noted that, when the output power is fixed, the lower the input voltage, the higher the input current and the lower the THD. This verifies the simulation results of Fig. 12 in Section VI.

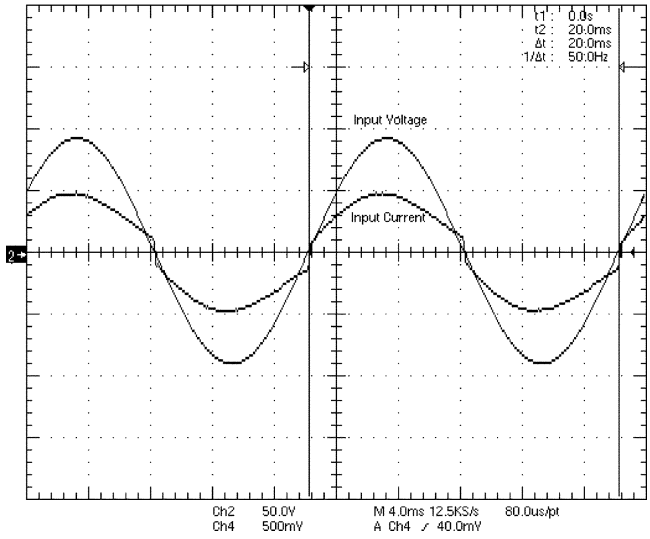

Fig. 17. Line current and voltage waveforms ($V_{\text{in}} = 65$ V, $P_{\text{load}} = 400$ W, $P.F. = 0.994, THD = 10.6\%$).

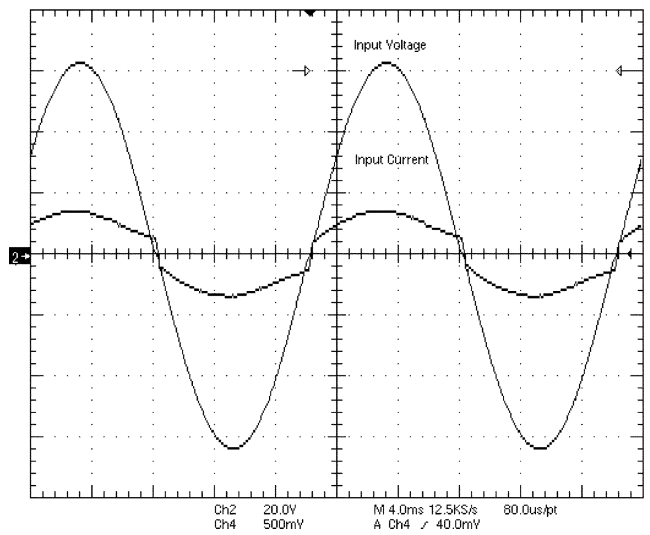

Fig. 18. Line current and voltage waveforms ($V_{\text{in}} = 45$ V, $P_{\text{load}} = 200$ W, $P.F. = 0.991, THD = 13.2\%$).

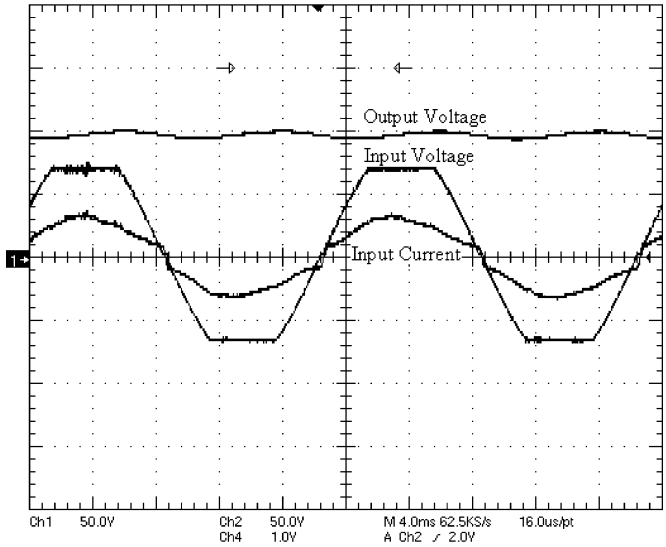

Fig. 19. Line current under distorted input voltage.

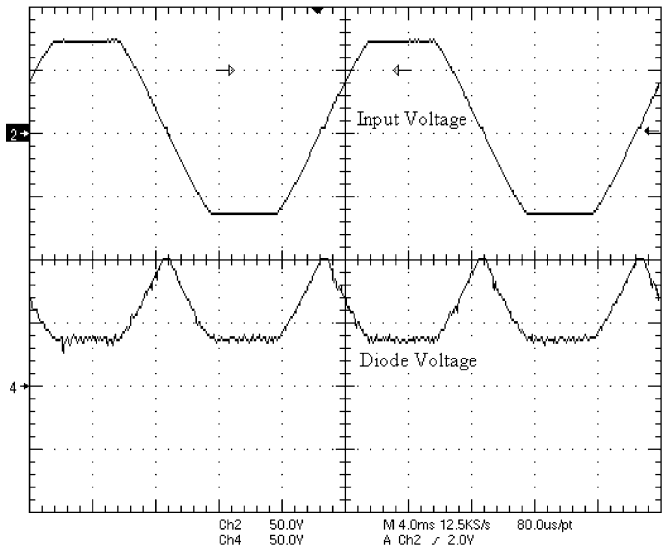

Fig. 20. Voltage waveform on diode for distorted input voltage.

When the output power is 200 W (output current $I_o = 2$ A), the input line current and voltage waveforms at input voltage of 45 V are shown in Fig. 18. The power factor under this operating condition is 0.991 (THD $= 13.2\%$). It is noted from Figs. 15 and 18 that, when the input voltage is fixed, the higher the load, the higher the input current and the lower the THD. This verifies the simulation results of Fig. 11 in Section VI.

The experimental results for steady state show that the proposed digital PFC control strategy can achieve near unity power factor in the steady state under wide input voltage and output power condition.

The input current waveform under distorted input voltage condition is shown in Fig. 19. The input voltage is set to 55 V and clipped at 85% of the peak value. The THD of input current is 12.5% under this condition. The test result show that the proposed PFC control method can still achieve sinusoidal input current even under the distorted input voltage condition. This is because the input voltage feed-forward is applied in the digital control algorithm. Fig. 20 shows that the diode voltage from cathode to anode under distorted input voltage condition. This verifies that the harmonics of the input voltage drop on the diode.

In the transient state of step input voltage change, the output voltage and input current waveform are shown in Figs. 21 and 22. In Fig. 21, the input voltage is changed from 45–55 V at the cursor position. The output voltage overshoot in the transient state is 2.9 V. In Fig. 22, the input voltage is changed from 55–45 V at the cursor position. The output voltage drop in the transient state is 2.3 V. The input current can remain sinusoidal waveform in the transient state of step input voltage change.

In the transient state of step load change, the output voltage and input current waveform are shown in Figs. 23 and 24. The output voltage is changed from 96.6–100.1 V when the output power changed from 400–200 W (output current I_o changed from 4–2 A). The output voltage is changed from 99.8–96.8 V

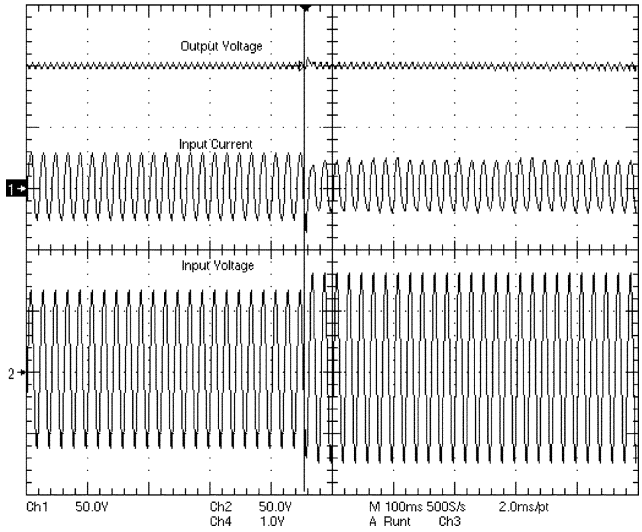

Fig. 21. Line current and output voltage for input voltage change ($V_{\rm in}$: 45 to 55 V).

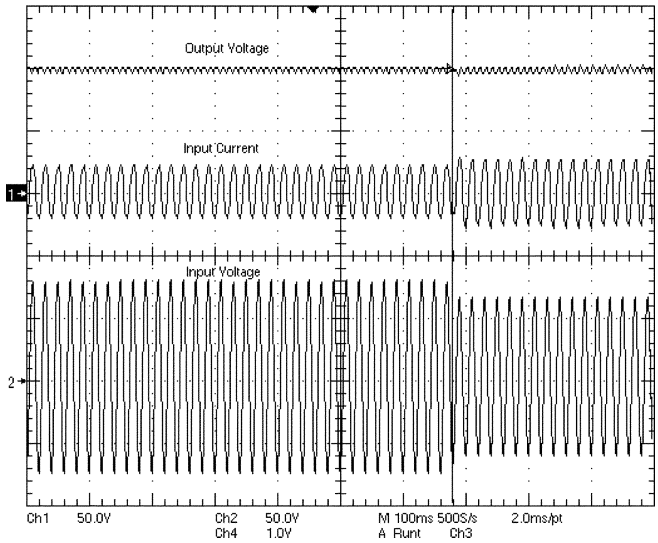

Fig. 22. Line current and output voltage for input voltage change ($V_{\rm in}$: 55–45 V).

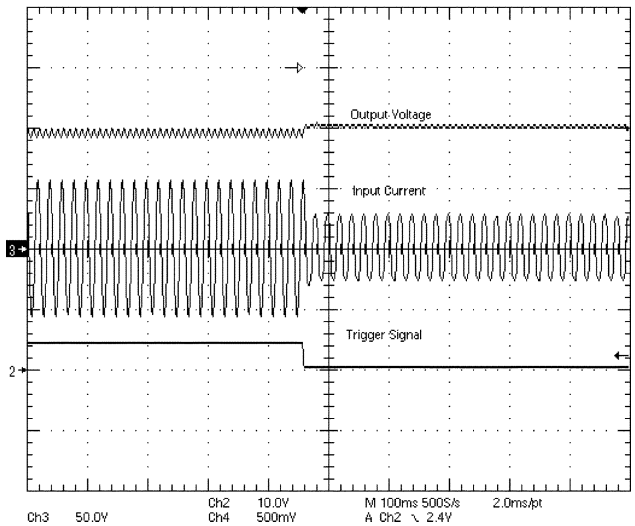

Fig. 23. Line current and output voltage for step load change (Full load to half load).

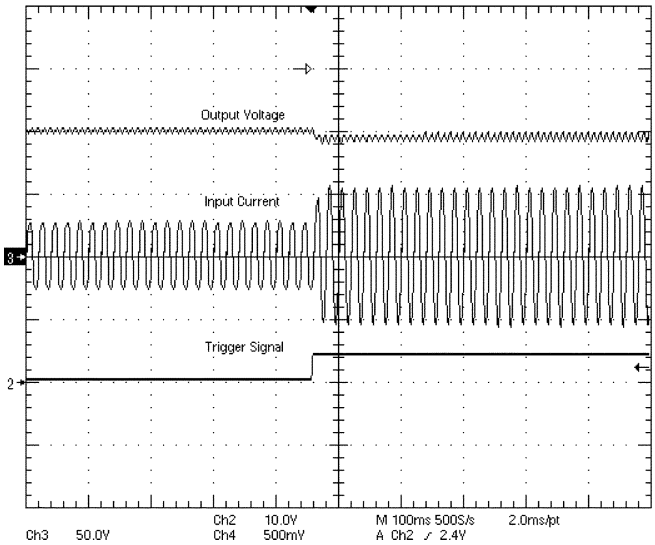

Fig. 24. Line current and output voltage for step load change (Half load to full load).

when the output power changed from 200–400 W (output current I_o changed from 2–4 A). The input current can remain sinusoidal waveform in the transient state of step load change.

VIII. Conclusion

A predictive algorithm is proposed for digital control PFC implementation. Based on the Boost topology, the predictive algorithm is derived in detail. By using this control strategy, all the duty cycles required to achieve unity power factor in a half line period are generated in advance. Because the speed of DSP is no longer the critical factor for high switching frequency PFC by using the proposed control strategy, a low cost DSP can be used to implement PFC operating at high switching frequency.

Simulation results show that, based on the predictive PFC control algorithm, near unity power factor can be achieved in the steady state under wide input voltage and load current conditions. A prototype of Boost PFC controlled by a DSP evaluation board was built to verify the proposed digital control PFC strategy. The experimental results show that the power factor over 0.99 can be achieved under wide input voltage and output power conditions. A sinusoidal current waveform with low THD can be achieved for distorted input voltage. The proposed PFC control strategy can achieve sinusoidal current waveform in the transient state for step load change and input voltage change.

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