A New Duty Cycle Parallel Control Method and FPGA Implementation for AC-DC Converters with Power Factor Correction (PFC)

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Abstract — **A new duty cycle parallel control method for AC-DC converter with power factor correction is proposed. The duty cycle required to achieve unity power factor consists of two terms: current term and voltage term. They are calculated directly based on the reference current and sensed inductor current, input voltage and output voltage. It requires only one multiplication and three addition operations for digital implementation so that the proposed PFC control method can be implemented by a low cost DSP, microprocessor, FPGA or an ASIC to achieve high switching frequency. This duty cycle parallel control essentially distinguishes from the conventional current mode control in which there are two regulators, one for voltage regulation and one for current regulation. Test results for a digital PFC implementation show that the proposed method can achieve unity power factor under both steady and transient state. Sinusoidal input current can be achieved under non-sinusoidal input voltage condition. The switching frequency of FPGA control Boost PFC is 400kHz. The proposed duty cycle parallel control strategy has high potential for the next generation of high switching frequency PFC implementation, due to its lower calculation requirement, lower cost and better performance than average current mode control.**

I. INTRODUCTION

With the development of digital technique, many advanced control strategies can be implemented by digital processors. Digital control is the trend in switching mode power supply applications in the future. However, it still faces several technique "bottlenecks" in the digital implementation of high switching frequency power supplies, including AC-DC and DC-DC converters. For AC-DC with power factor correction, there are several disadvantages in the existing digital control PFC implementation based on conventional current mode control, such as high computation requirement, limited switching frequency and high cost [1][2]. Predictive control methods are being explored and implemented in digital controlled PFC in order to take full advantage of digital techniques. Digital current program control using predictive algorithm was presented in [3]. In that paper, the duty cycle, d(n+1), was calculated based on the value of the present duty cycle d(n) and sensed inductor current, input voltage and output voltage. Unity power factor was achieved. The first disadvantage is that the duty cycle calculation requires the duty cycle value in the previous switching cycle. Second, the computation requirement is not obviously reduced compared to that in the digital PFC implementation based on current mode control. Reference [4] proposed dead-beat predictive control in which a predicted duty cycle was used to control the switch during a control period which is equivalent to several or several tens switching cycles. The duty cycles were fixed during one control period. Computation was reduced in that control method. However, the harmonics in the line current was increased compared to the control method in which the duty cycle was calculated in every switching cycle. The computation requirement in digital PFC implementations was reduced further by the techniques proposed in [5] [6] because all the duty cycles for a half line period were calculated in advance based on the voltage loop and the input voltage feed-forward. However, the current waveform is sensitive to the parameters of the model and the capability of the regulation to the step load change is not satisfied when the load variation is wide. A simple PFC control algorithm, which is actually "a digital version of charge control", was specifically designed and implemented by a FPGA combined with an analog to digital converter (ADC) [7][8]. The switch turns "on" at the beginning of every switching period and "off" when the mean value of input current reaches the reference value. The mean value of input current is the sum of the input current samples divided by the number of samples in one switching cycle. In order to guarantee the resolution of the duty cycles, a fast ADC is required in the integral operation for the calculation of input current mean value. Therefore, the cost of the control system is increased.

A new duty cycle parallel control method for digital power factor correction implementation is proposed in this paper. The duty cycle required to achieve unity power factor is calculated in parallel based on the reference current and sensed inductor current, input voltage and reference output voltage. According to the proposed control method, the duty cycle is composed of two parallel terms. The first term is called current term and it depends on the inductor current change between the inductor current value at the beginning of the switching cycle and the reference current value at the end of that switching cycle. The second term is called voltage term. It depends on the input voltage and the reference output

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voltage. This term is determined by the volt-second balance of the Boost converter. This control philosophy essentially distinguishes from the conventional current mode control and any other control methods with two regulators, one for voltage regulation and one for current regulation. For digital implementation, the proposed duty cycle control method requires only one multiplication and three addition operations so that it can be implemented by a low cost DSP, microprocessor, FPGA or ASIC to achieve high switching frequency. The proposed duty cycle parallel control for PFC implementation overcomes the disadvantages of the existing digital PFC techniques mentioned above, such as high computation requirement, model sensitivity and increased harmonics, etc.

II. Duty Cycle Parallel Control Algorithm for PFC with Boost Topology

Boost topology used in PFC implementation is shown Fig. 1. The proposed digital control PFC algorithm is derived based on the assumptions that the Boost converter operates at continuous conduction mode (CCM) and the switching frequency is much higher than the line frequency (the input voltage, V_{in}, can be assumed as a constant in one switching cycle, T_s). Therefore, when the switch S is on or off, the Boost converter is described as two equivalent circuits, as shown in Fig. 2. Differential equation (1) and (2) describe the inductor current in one switching cycle when switch is on or off, respectively.

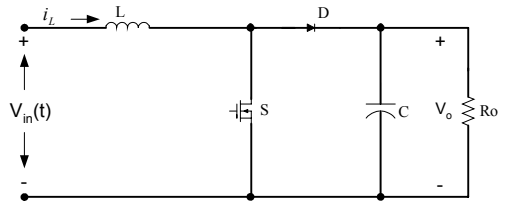
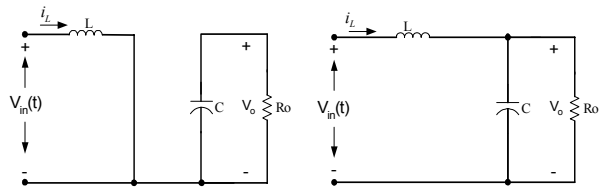


Fig. 1 Boost converter topology



(a) switch is on (b) switch is off

Fig. 2 Boost converter equivalent circuit

$$L\frac{di_L}{dt} = V_{in} \qquad t_n \le t < t_n + d_n T_s \qquad (1)$$

$$L\frac{di_L}{dt} = V_{in} - V_o \qquad t_n + d_n T_s \le t < t_{n+1} \qquad (2)$$

Substituting $\frac{di_L}{dt} \approx \frac{i_L(n+\Delta t) - i_L(n)}{\Delta t}$ *(Δt→0)* into (1) and (2), the inductor current at the end of one switching cycle can be expressed as

$$i_L(n+1) = i_L(n) + \frac{V_{in}(n)\cdot T_s}{L} - \frac{V_o(1-d(n))\cdot T_s}{L} \qquad (3)$$

Equation (3) can be rearranged as:

$$d(n) = \frac{L}{T_s}\frac{i_L(n+1) - i_L(n)}{V_o} + \frac{V_o - V_{in}(n)}{V_o} \qquad (4)$$

It is observed from (4) that the duty cycle in each switching cycle could be determined properly to achieve unity power factor. In a properly designed AC-to-DC converter with PFC, $i_L(n+1)$ is forced to follow the reference current, $i_{ref}(n+1)$, which is a rectified sinusoidal waveform, as shown in Fig. 3. V_o is controlled to follow the reference voltage, V_{ref}. Substituting $i_{ref}(n+1)$, V_{ref} for $i_L(n+1)$ and V_o in (4), the duty cycle can be derived as

$$d(n) = \frac{L}{T_s}\frac{i_{ref}(n+1) - i_L(n)}{V_{ref}} + \frac{V_{ref} - V_{in}(n)}{V_{ref}} \qquad (5)$$

where $i_L(n)$ is the sensed current. The duty cycle calculated by (5) can achieve unity power factor in Boost converter. In Fig.3, the duty cycle $d(n)$ calculated by (5) forces the inductor current changed from $i_L(n)$ to $i_L(n+1)$. $i_L(n+1)$ is not exactly the same as $i_{ref}(n+1)$, but should be very close to it.

There are two terms in (5), expressed as

$$d(n) = d_1(n) + d_2(n) \qquad (6)$$

The first term, $d_1(n)$, expressed as

$$d_1(n) = \frac{(i_{ref}(n+1) - i_L(n))\cdot\frac{L}{T_s}}{V_{ref}} \qquad (7)$$

is defined as current term. Under the steady state, the inductor current, $i_L(n+1)$, follows the reference current, $i_{ref}(n+1)$, at the end of that switching cycle. In (7), the reference current is determined as

$$i_{ref}(n+1) = k_{PID}\cdot\left|\sin(\omega_{line}\cdot t(n+1))\right| \qquad (8)$$

k_{PID} is the peak value of the reference current, which is the output of voltage loop regulator. $|sin(\omega_{line}\cdot t(n+1)|$ is the rectified line frequency sinusoidal waveform, which is stored in a look-up table. Under the transient state, if the load is increased, the output voltage is dropped. The error between the reference voltage and the feedback voltage is increased. Then, the output of voltage loop PID regulator, K_{pid}, is increased. Hence, the reference current is increased, which results in the current term, d_1, increasing. Eventually, the duty cycle is increased to force the output voltage to follow the reference voltage again. If load is decreased, the opposite process occurs. Therefore, $d_1(n)$ guarantees the output voltage be regulated to follow the reference voltage under transient state of load change.

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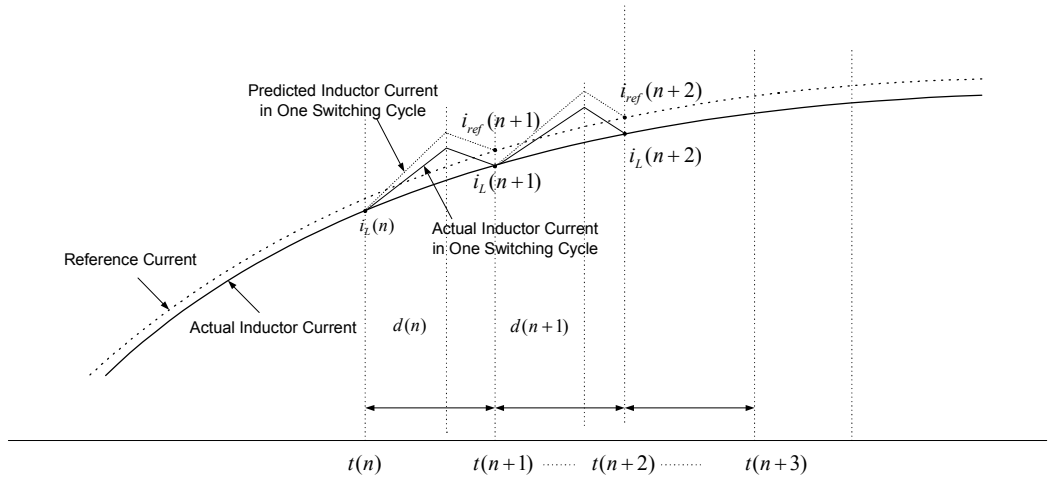

Fig. 3 Inductor current controlled by the directly calculated duty cycles

The second term, $d_2(n)$, expressed as

$$d_2(n) = 1 - \frac{V_{in}(n)}{V_{ref}} \tag{9}$$

is determined by the input and output voltage equilibrium of Boost topology. Therefore, d_2 is defined as voltage term. In (9), $V_{in}(n)$ is the instantaneous input voltage value sensed by the input voltage feed-forward. It is observed from (9) that, if the input voltage is increased under the transient state, $d_2(n)$ is decreased instantaneously. Therefore, the duty cycle is decreased without delay to regulate the output voltage for input voltage change.

Substitute (8) into (5), the proposed PFC control algorithm can be expressed as:

$$d(n) = \frac{k_{PID} \cdot \left|\sin(\omega_{line} \cdot t(n+1)\right| - i_L(n)}{K_c} + \frac{V_{ref} - V_{in}(n)}{V_{ref}} \tag{10}$$

where, $K_c = T_s \cdot V_{ref} / L$, is a constant which can be used to simplify the proposed PFC control algorithm in the implementation. Because the reference current in (10) is sinusoidal, the actual inductor current is forced to be sinusoidal and achieve unity power factor.

The block diagram of duty cycle parallel control for PFC implementation is shown in Fig. 4. In the figure, the voltage term block implements the calculation of equation (9) and the current term block implements the calculation of equation (7). With this duty cycle parallel control method, equation (10), the inductor current of the Boost converter will follow the reference current with a difference gap between the reference current value and actual inductor current value. This difference gap is determined by the load condition. At the same time, the output voltage of the Boost converter will exactly follow the reference voltage in the voltage closed loop implementation.

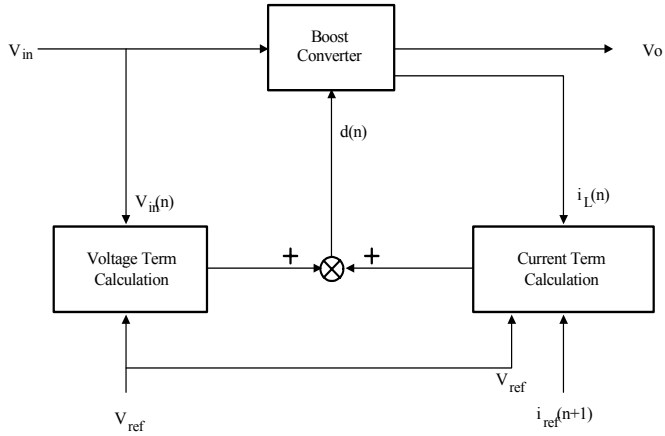

Fig. 4 Diagram of duty cycle parallel control

2.1 Simplification of the Proposed PFC Control Algorithm

In the digital implementation of the proposed duty cycle calculation algorithm, (6), (7) and (9) can be simplified by multiplying all the parameters with the constant K_c, as:

$$D(n) = D_1(n) + D_2(n) \tag{11}$$

$$D_1(n) = k_{pid} \cdot |\sin(\omega_{line} \cdot t(n+1))| - i_L(n) \tag{12}$$

$$D_2(n) = K_c - V_{in}^{'}(n) \tag{13}$$

where, $D_1(n) = d_1(n) \cdot K_c$, $D_2(n) = d_2(n) \cdot K_c$, $V_{in}^{'}(n) = \frac{V_{in}(n)}{V_{ref}} \cdot K_c = \frac{T_s}{L} V_{in}(n)$. $D(n)$, $D_1(n)$ and $D_2(n)$ are simplified values of duty cycle, $d(n)$, and its components, $d_1(n)$ and $d_2(n)$.

It is observed from (11), (12) and (13) that after simplification, only one multiplication and three additions (subtractions) are required in order to implement the proposed duty cycle control algorithm. Therefore the digital implementation of the proposed PFC control algorithm is very simple. A low cost DSP, microprocessor, FPGA or an ASIC

can be used to implement PFC operating at high switching frequency because of its low computation requirement.

III. FPGA IMPLEMENTATION

The proposed duty cycle parallel control strategy for PFC is verified by FPGA implementation. The proposed algorithm for duty cycle calculation algorithm can be implemented by FPGA in parallel, so that it is suitable for high switching frequency digital control PFC. The block diagram of FPGA implementation of duty cycle parallel control PFC is shown in Fig. 5.

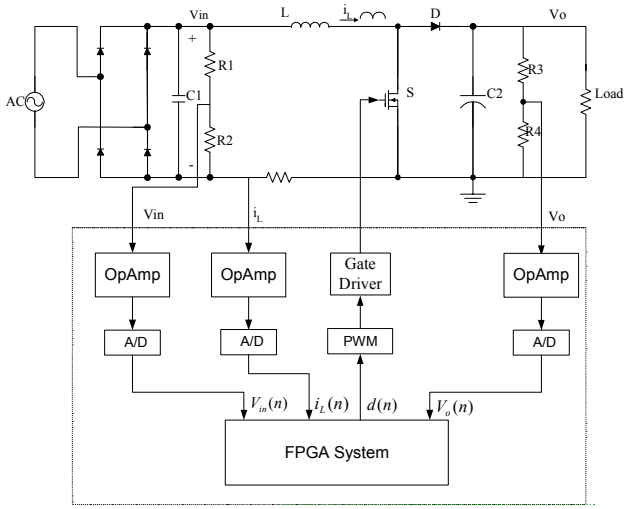

Fig. 5 Block diagram of FPGA implementation

In Fig. 5, the input voltage, inductor current and output voltage are sensed and input to the A/D converters via operating amplifiers (OpAmp). 10-bits A/D converter, AD 9215, is used in the designed system. The typical input signal range of AD9215 is 2V (peak to peak value). Hence, the input range for unipolar signal is 1V. The FPGA is Xlinx Spartan IIE XC2S200E. The clock frequency is 50MHz. The PWM signal with the calculated duty cycle is sent to the switch through a gate driver circuit.

The prototype of Boost PFC controlled by FPGA is shown in Fig. 6. The proposed duty cycle calculation algorithm can be executed in parallel by FPGA implementation. The VHDL implementation of the duty cycle parallel control in FPGA is shown in Fig. 7. The architecture II for current term calculation and architecture III for voltage term calculation are processed in parallel concurrently. In the prototype, the 50MHz FPGA chip was used to implement the proposed control method in AC-DC converter with PFC operating at 400kHz switching frequency. In the FPGA verification, about 15,000 gates are used in the FPGA. This means that a mixed signal ASIC solution based on the proposed duty cycle parallel control can achieve high switching frequency with lower cost, than the other digital solution for PFC implementation.

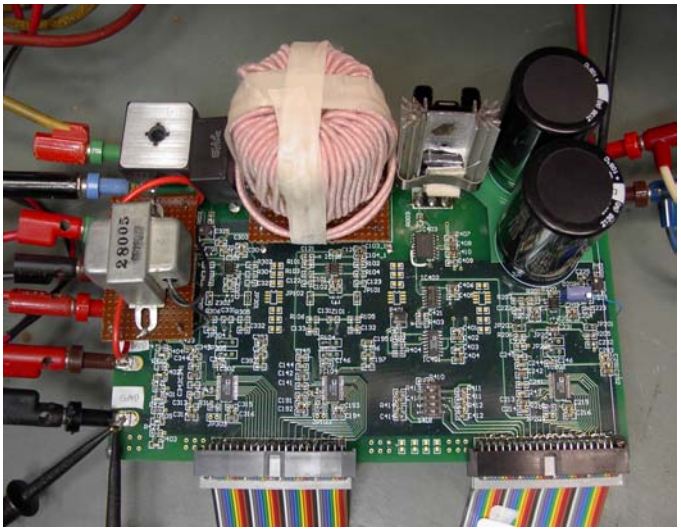

Fig. 6 Prototype of FPGA implementation

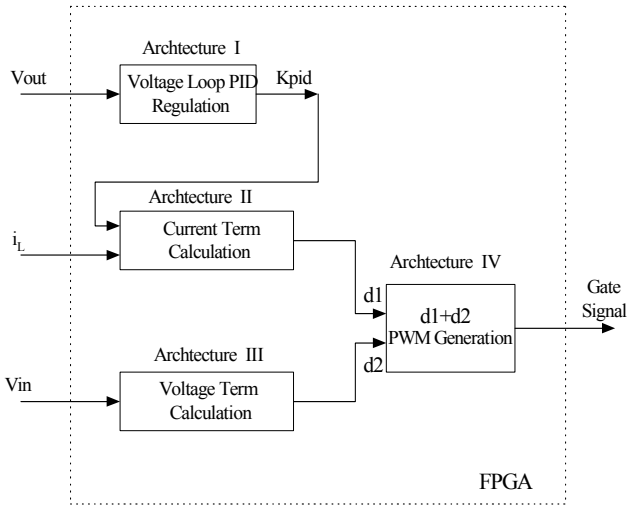

Fig. 7 Diagram of FPGA implementation

IV. EXPERIMENTAL RESULTS

The operating parameters for the prototype of FPGA implementation are chosen as the following: rated input voltage V_{in}=55V(RMS), output voltage V_{out}=100V, rated output power P_{load}=300W, switching frequency f_{sw}=400kHz and line frequency f_{line}=60Hz.

The input current and voltage waveforms for the full load (I_o=3A) under the steady state are shown in Fig. 8. The power factor under this condition is 0.999 and THD is 3.8%. The input current and voltage waveforms for the load current, I_o=2A, is shown in Fig. 9. The power factor under this condition is 0.998 and THD is 5.9%. Test results show that the proposed PFC control method can achieve near unity power factor under the steady state.

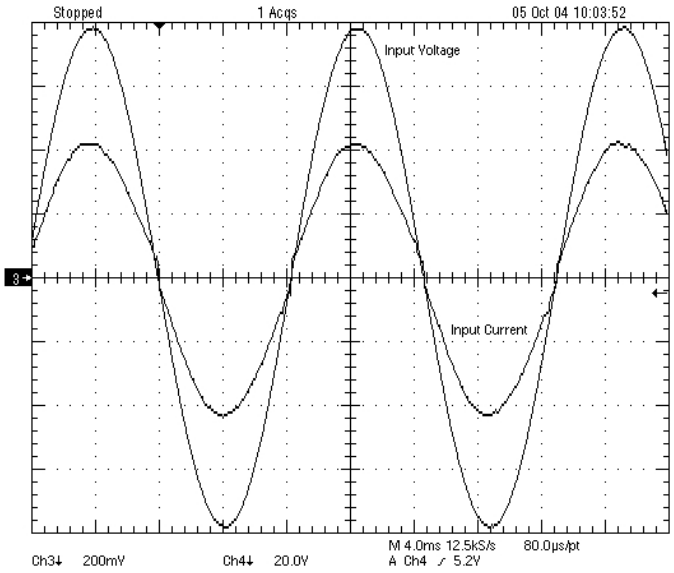

Fig. 8 Input voltage and current waveforms for full load; I_o=3A, THD=3.8%, PF=0.999, Voltage: 20V/div, Current: 4A/div

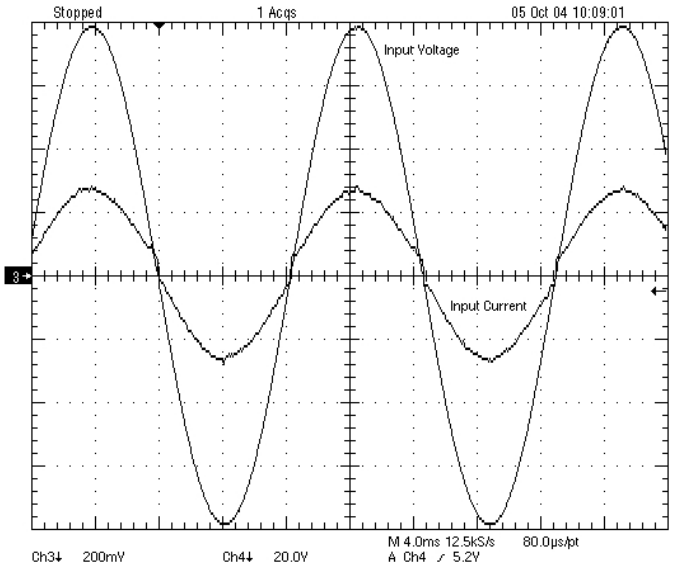

Fig. 9 Input voltage and current waveforms 2A load; I_o=2A, THD=5.9%, PF=0.998, Voltage: 20V/div, Current: 4A/div

The input current waveforms under distorted input voltage condition are shown in Fig. 10. The input voltage is 55V and clipped at 85% peak value. The THD of input voltage is 6.6%. The THD of input current is 4.9% and the power factor is 0.999. Test results show that sinusoidal input current waveform can be achieved under non-sinusoidal input voltage condition.

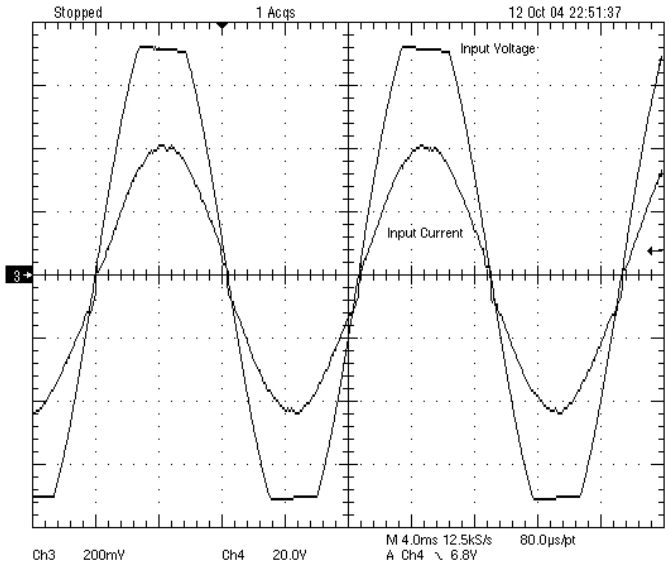

Fig. 10 Input current waveform for distorted input voltage; input current THD=4.9%, Voltage: 20V/div, Current: 4A/div

The dynamic performance under the transient state for step input voltage change is shown in Fig. 11 and Fig. 12, respectively. When the input voltage is changed from 55V to 65V, as shown in Fig. 11, the output voltage overshoot in the transient state is about 1V. When the input voltage is increased from 65V to 55V, as shown in Fig. 12, the output voltage drop in the transient state is about 1V. The input current still maintains sinusoidal waveform under the transient state. The voltage drop or overshoot to the step input change is small.

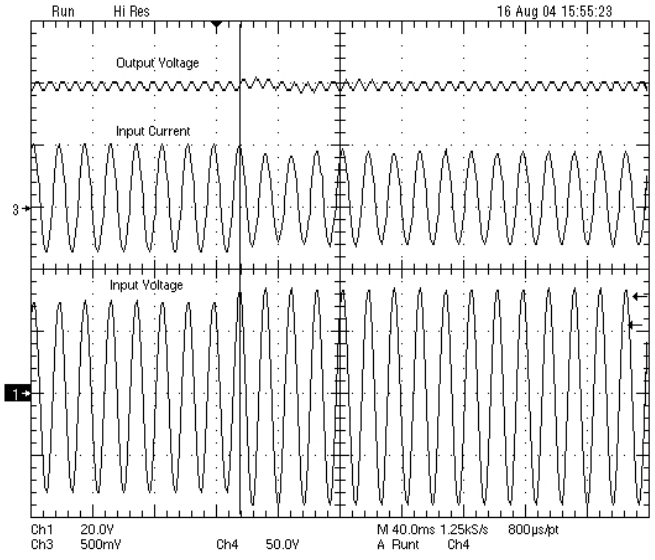

Fig. 11 Input current & output voltage for step input voltage change; V_{in} changed from55V to 65V, output voltage overshoot: 1V, Input voltage: 50V/div, Output voltage: 20V/div, Current: 10A/div

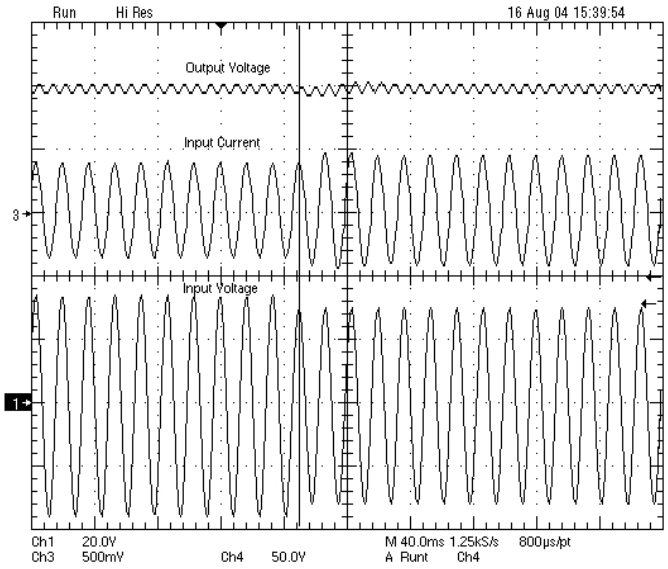

Fig. 12 Input current & output voltage for step input voltage change; V_{in} changed from65V to 55V, output voltage drop: 1V, Input voltage: 50V/div, Output voltage: 20V/div, Current: 10A/div

The dynamic performance under the transient state when the load current is changed from 2A to 3A and from 3A to 2A are shown in Fig. 13 and Fig. 14, respectively. The output voltage drop is 2.3V when the output power changed from 200W to 300W (load current I_o changed from 2A to 3A). The output voltage overshoot is 2.5V when the output power changed from 300W to 200W (load current I_o changed from 3A to 2A). The input current can maintain sinusoidal waveform in the load transient state.

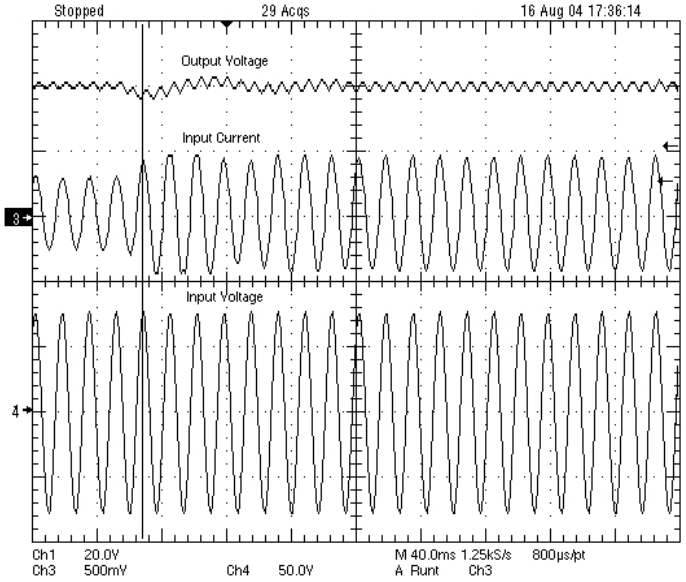

Fig. 13 Input current & output voltage waveforms in load transient state; *Io* changed from 2A to 3A, output voltage drop 2.3V, Input voltage: 50V/div, Output voltage: 20V/div, Current: 10A/div

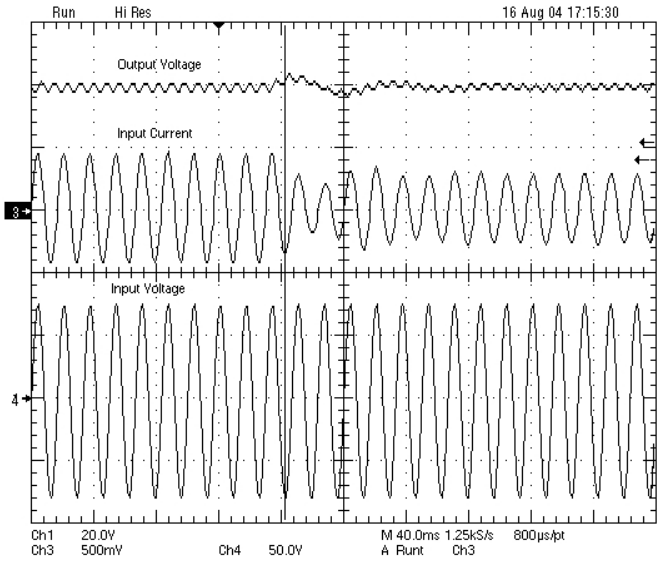

Fig. 14 Input current & output voltage waveforms in load transient state; *Io* changed from 3A to 2A, output voltage overshoot 2.5V, Input voltage: 50V/div, Output voltage: 20V/div, Current: 10A/div

V. CONCLUSION

A new duty cycle parallel control method for AC-DC converter with power factor correction is proposed. The duty cycle required to achieve unity power factor consists of two terms: current term and voltage term. They are calculated directly based on the reference current and sensed inductor current, input voltage and output voltage. It requires only one multiplication and three addition operations for digital implementation so that the proposed PFC control method can be implemented by a low cost DSP, microprocessor, FPGA or an ASIC to achieve high switching frequency. The proposed duty cycle parallel control method is simpler than commonly used average current mode control for PFC implementation.

Test results for a FPGA implementation show that the proposed method can achieve unity power factor under both steady and transient state. Sinusoidal input current can be achieved under non-sinusoidal input voltage condition. The proposed digital PFC control method can achieve good dynamic performance for load and input voltage change.

The switching frequency of FPGA control Boost PFC is 400kHz. The FPGA implementation for the proposed duty cycle parallel control method shows that it can achieve near unity power factor by using low gate number.

The proposed duty cycle parallel control strategy has high potential for the next generation of high switching frequency PFC implementation, due to its lower calculation requirement, lower cost and better performance than average current mode control.

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