A Novel Nonisolated Half Bridge DC-DC Converter

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***Abstract*---The duty cycle of conventional multi-phase buck converters becomes extremely small as the output voltage becomes lower and lower. This is a severe challenge with the switching frequency goes up. This paper introduces a non-isolated half bridge converter which extends duty cycle to a favorable range. Thus, the converter will have symmetrical dynamic response ability. The switching loss will reduce dramatically. The primary current is directly transferred to the output. The energy transferring is more effectively then that of conventional isolated half bridge converter. In addition, the voltage stress of the primary MOSFETs equals to the input voltage, which is much lower than that of non-isolated forward or push-pull topologies. A 12V input, 1V/30A output, 350 kHz prototype was built to demonstrate the advantages.**

I. INTRODUCTION

There is a clear trend that the output voltage of VRMs designed for the future microprocessors will be 1V even lower. In order to reduce the passive component size, and also to meet the stringent transient response requirement, the switching frequency will also move into the MHz range in the next few years. Today's 12V input VRMs usually use multi-phase interleaving synchronous buck topology. Due to the low output voltage and high switching frequency, the duty cycle is very narrow, which reduces the VRMs efficiency and impairs transient response.

To solve above-mentioned problems, transformer based topologies, such as tapped inductor buck converter, active-clamp couple-buck converter, forward converter, push-pull converter are developed.

Tapped – inductor and coupled buck converter extends the converter duty cycle to a favorable range [1]-[4]. However, this topology also generates some other issues such as complicated magnetic implementation. The other drawback is the leakage inductance of the coupled-inductor, which makes the topology almost infeasible without additional snubber.

Nonisolated forward topology is another solution [5]. But since the transformer works in the first quadrant, the size of the transformer will be much bigger than that of double-ended topologies. Therefore, the overall size of the VRM will be bigger than multiphase buck solution. In addition, the voltage stress of the primary MOSFET is twice the input voltage.

Nonisolated push-pull topology is another choice. A smaller core can be used for the same out power comparing with the above forward topology [6][7]. The drawback is there are two windings in primary, which makes the transformer design a little more critical when using planar PCB transformer. Furthermore, it's necessary and important to avoid transformer imbalance. The voltage stress of primary MOSFETs is also twice the input voltage.

This paper presents a novel non-isolated half bridge topology as an alternative solution for future 12V VRMs. A current doubler is adopted for the secondary side, which can reduce the output ripple. This proposed topology has many benefits as compared with the above mentioned topologies. The transformer size is much smaller than that in forward topology. The imbalance of the transformer is not a critical issue. The voltage stress of the primary MOSFETs equals to the input voltage, which is much lower than those in forward or push pull. There are only two switches at the primary side, the control method is simple.

A 12V input, 1V/30A output prototype was built to demonstrate the feasibility and the advantages of this proposed topology.

II. LIMITATIONS OF CURRENT APPROACHES

Most of VRMs today use synchronous rectifier buck topology. As the output voltage goes down and the switching frequency goes up, the duty cycle becomes extreme narrow and the turn - on period of the top switch becomes extreme short. In order to generate this extreme short gate driving signal, a high speed comparator is necessary, this may increase cost. Moreover, the extreme duty cycle may cause

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malfunction at high frequency due to the very short conduction time for the top switch.

Another problem is the asymmetrical transient response. The step - down response is much worse than the step - up response. That's because when the load steps up, the duty cycle can extend much to provide energy to the output and the inductor charging voltage V_{in} – Vo is high, while the duty cycle cannot be much smaller to respond effectively to a load step down and the inductor discharging voltage Vo is unfortunately low as well. This asymmetrical transient response makes the output filter over-designed and makes it very difficult to optimize the design [4].

The most serious problem for the 12V – input buck converter is the large top switch turn – off loss. For the same input average current, the narrower the duty cycle, the higher the peak current goes through the top switch. Furthermore, in order to satisfy the fast transient response requirement, the inductance can't be too large. Small inductance yields large current ripple. Hence, the turn-off current of the top switch becomes very large, as shown in Fig. 1, so the turn-off switching loss and efficiency will suffer.

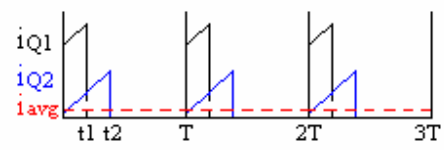


Fig. 1 Peak current comparison of different duty cycle

Multi-phase interleaving synchronous rectifier buck topology is a widely recognized solution today. The major benefits of this topology are the output ripple cancellation and the improved transient response. But the effectiveness of this ripple cancellation is related to the duty cycle. This topology can't extend the duty cycle so the duty cycle is still extremely narrow when the output voltage goes down further. Thus, the ripple cancellation is actually very poor.

Transformer based topologies can help extend the duty cycle to a favorable range. Tapped inductor buck converter, coupled buck converter, nonisolated forward converter and push-pull converter are developed for above reason. But those solutions cause some other issues at the same time. Reducing or eliminating the effect of leakage inductance is a severe challenge for tapped-inductor and coupled inductor topologies. Big transformer makes forward topology not so attractive. A common drawback of those topologies is that the voltage stress of the primary switches is much higher than the input voltage, even twice. For 12V input VRM, it's reasonable that the input voltage maybe up to 14V, so the voltage stress of primary switches is 28V plus spike. Obviously, 30V MOSFET, which is widely used in 12V - input VRM application, is not available again. Thus, the efficiency and performance of the converter will suffer.

Topologies with extended duty cycle and low voltage stress are expected.

III. THE PROPOSED NONISOLATED HALF-BRIDGE TOPOLOGY

Fig.2 is a conventional half bridge topology. Current doubler is adopted at the secondary side, which can provide ripple cancellation. When isolation is not needed, the primary ground can be connected with secondary ground. By selecting proper transformer turns ratio, a duty cycle around 50% can be achieved for 12V input and 1V output.

It is observed that with the conventional half bridge converter, all the output electrical energy is converted into magnetic energy and back into electrical energy through the transformer. It is also observed that the primary ground shall be at a stable voltage potential so that the half bridge can operate well.

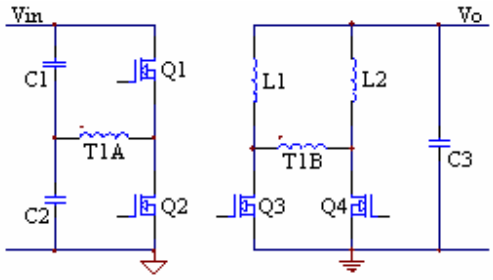


Fig. 2 Conventional half bridge topology

A new topology is developed by connecting the primary ground of the conventional half bridge converter to the output voltage point instead of connecting it to the secondary ground, as shown in Fig.3.

Comparing with the conventional half bridge topology, the major advantage of this proposed circuit is that part of the output energy is transferred from the input to the load directly. Therefore, the secondary winding current and inductor current is reduced, and the converter operates more efficiently. Duty cycle can be extended and optimized by selecting appropriate turns ratio of the transformer. The turn - off time of Q2 can also be reduced significantly because the gate is reversely biased by the output voltage during off time.

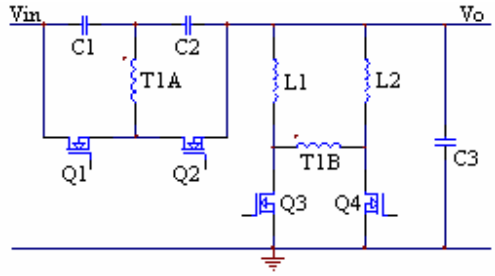


Fig.3 Proposed nonisolated half bridge topology

It is understandable that the nonisolated half bridge converter has similar basic operation principle and waveforms with the conventional half bridge converter. Fig.4 gives the key waveforms of the proposed topology. Q1, Q2 turn on alternatively as within the conventional half bridge converter. Q1 and Q4 turn on complementarily, and Q2 and Q3 turn on complementarily as well. The input current in the proposed converter is directly transferred to the output in addition to the secondary current. This is a more effective way to deliver energy than the conventional half bridge converter. Control of the nonisolated half bridge converter is the same as the control of a conventional half bridge converter.

The nonisolated half bridge converter operation can be briefly described by five operation modes as shown in Fig. 5 as follows:

Mode 1 (t < t1): Initially, Q1 and Q2 are off. Q3 and Q4 are on. The inductors L1 and L2 are both freewheeling.

Mode 2 (t1 < t < t2): Q1 turns on and Q4 turns off at t1 simultaneously. The energy starts delivering from input to the load. The inductor L1 is still freewheeling through Q3, while the inductor L2 is charged through Q3 as well. In addition to the current of inductor L1 and L2, the input current also goes through C3 and load resistor. Part of required energy delivers to output directly.

Mode 3 (t2 < t < t3): Q1 turns off and Q4 turns on at t2 simultaneously. The inductors L1 and L2 are both freewheeling.

Mode 4 (t3 < t < t4): Q2 turns on and Q3 turns off at t3 simultaneously. The inductor L1 is charged while L2 is still freewheeling through Q4. In addition to the current of inductor L1 and L2, the input current also goes through C3 and load resistor. Part of required energy delivers to output directly.

Mode 5 (t4 < t < t5): Q2 turns off and Q3 turns on at t4 simultaneously. The inductors L1 and L2 are both freewheeling. At t5, Q1 turns on and Q4 turns off again. Next cycle starts.

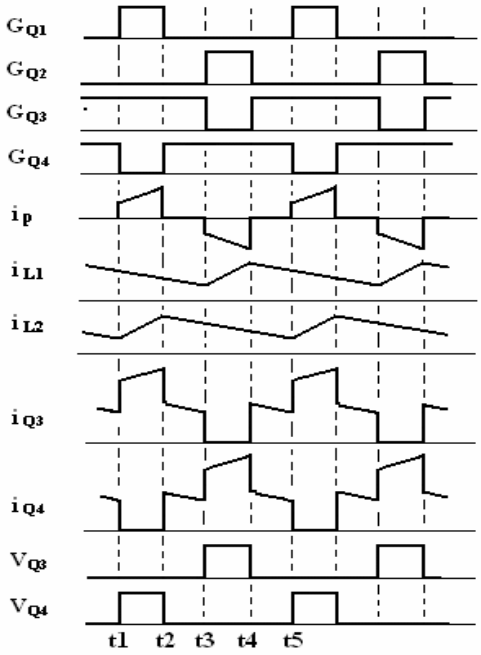
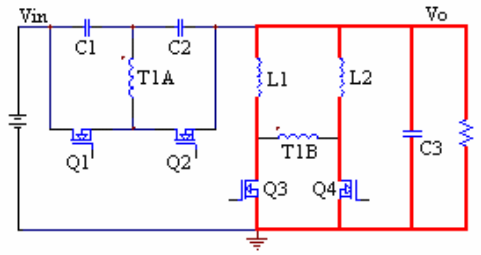
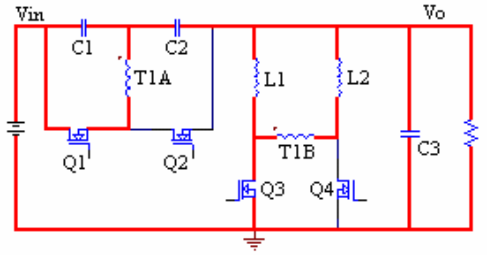


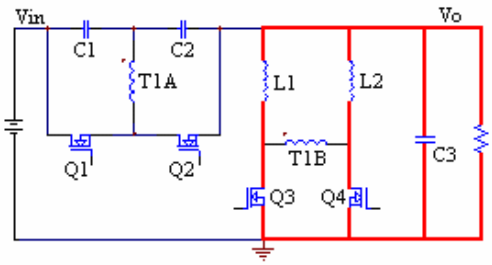
Fig.4 Key waveforms of the proposed topology



Mode 1



Mode 2



Mode 3

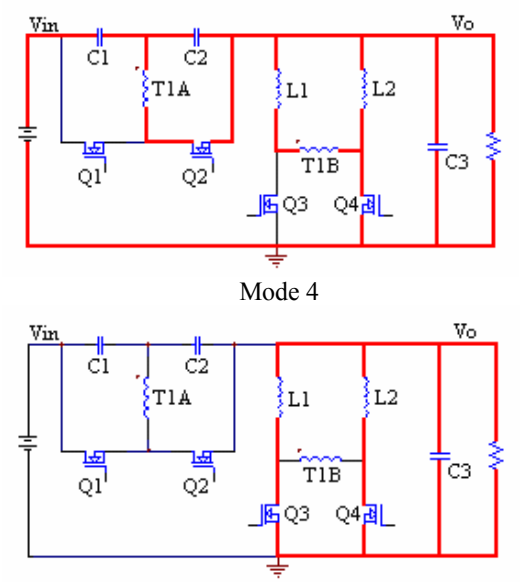


Fig. 5 Equivalent circuits in 5 operation modes

IV. ANALYSIS OF THE PROPOSED TOPOLOGY

The major advantages of this proposed topology are the duty cycle is extended and the overall efficiency is improved comparing with a buck converter. The dynamic performance of the converter will also benefit from the extended duty cycle. Detailed analysis will be engaged below.

The operating principle of this nonisolated converter is similar to a conventional half bridge converter, but there is still some difference.

For conventional half bridge converter, the steady-state conversion ratio is:

$$M = \frac{V_o}{V_{in}} = \frac{D}{2n} \qquad (1)$$

For the proposed converter, the primary voltage amplitude of the transformer is:

$$V_p = \frac{V_{in} - V_o}{2} \qquad (2)$$

The voltage - second of the secondary inductor L1 or L2 must keep balance in steady-state. Considering the voltage - second of L1 over a whole switching cycle:

At t1 ~ t2, t = D * Ts / 2, V_L = - Vo

At t2 ~ t3, t = (1 – D) * Ts / 2, V_L = - Vo

At t3 ~ t4, t = D * Ts / 2, $V_L = V_p / n - Vo$

At t4 ~ t5, t = (1 – D) * Ts / 2, V_L = - Vo

The amount of voltage – second over one switching cycle should be zero, so we can get:

$$-V_o \cdot \frac{D}{2} \cdot T_s - V_o \cdot \frac{1-D}{2} \cdot T_s + \left(\frac{V_p}{n} - V_o \right) \cdot \frac{D}{2} \cdot T_s - V_o \cdot \frac{1-D}{2} \cdot T_s = 0$$

Thus the conversion ratio of the proposed converter can be solved as:

$$M = \frac{V_o}{V_{in}} = \frac{D}{4 \cdot n + D} \qquad (3)$$

Meanwhile, the duty cycle can be derived as:

$$D = \frac{4 \cdot V_o \cdot n}{V_{in} - V_o} \qquad (4)$$

Where, D is the converter duty cycle. V_{in} is the input voltage. Vo is the output voltage. n is the transformer turns ratio (Np / Ns). Ts is the switching period. V_L is the voltage across inductor L1.

If the input voltage Vin is 12V and output voltage Vo is 1V, the duty cycle is 0.083 when buck topology is adopted. Instead, the duty cycle will be 0.545 (assume n=1.5) when the proposed topology is adopted. The duty cycle is extended significantly.

With the duty cycle extended to an appropriate range from extreme narrow level, the converter will have symmetrical dynamic response ability. High performance comparator will be not necessary for the pulse width modulator again. The possibility of malfunction will decrease. The most attractive benefit is that the switching loss will reduce dramatically.

The ideal voltage stress of the primary MOSFETs, V_{in} – Vo, is less than the input voltage. While on the contrary, the voltage stress of the primary MOSFETs is two times of the input voltage in forward and push pull topologies. That means the proposed topology can get higher reliability or lower conduction loss by using lower voltage rate MOSFETs, such as 30V even 20V MOSFETs. Another benefit of low voltage stress is that the miller effect of MOSFETs reduces, so the gate driving loss even switching loss can be reduced.

The major benefits of the proposed nonisolated half bridge converter can be summarized as:

1. Switching loss will reduce dramatically with the extended duty cycle.

2. The energy transferring is more effectively then that of conventional half bridge converter.
3. The voltage stress of the primary MOSFETs is less than the input voltage.

V. LOSS COMPARISON

Detailed loss analysis for a 12V - input, 1V/30A output converter was done. A two - phase synchronous buck converter was also designed for same requirement and used as a benchmark for this analysis.

Roughly, the total power loss of a buck converter and the proposed nonisolated half bridge converter can be divided into four parts:

1. Switching loss of the MOSFETs
2. Conduction loss of the MOSFETs
3. Gate driving loss of the MOSFETs
4. Loss of Magnetic components

Turn – off loss is the dominant loss for the primary MOSFETs and top MOSFETs. In the proposed nonisolated half bridge converter, the duty cycle is extended, so the peak current flows through the primary MOSFETs decreases dramatically for the same output power. Thus the turn - off loss of the primary MOSFETs, which is proportional to the peak current, will be significantly reduced as compared with that of the top MOSFETs in a two-phase buck converter. For a 12V - input, 1V/30A output two - phase buck converter, assuming current ripple is 20A, the peak current flowing through each top MOSFET will be 25A when it turns off. On the contrary, if the nonisolated half bridge converter (NHB) is adopted, the primary current ripple is only 7.27A by using the same inductor as buck converter, so the peak current flowing through each primary MOSFET will be 10.5A when it turns off. Fig. 6 illustrates the difference.

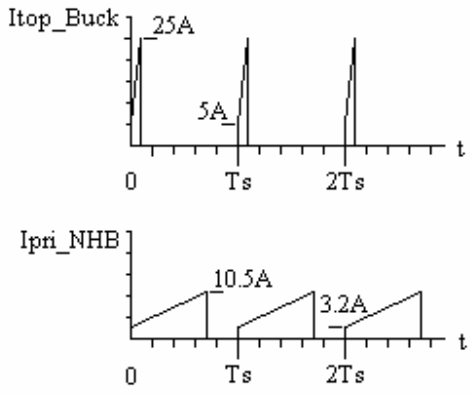


Fig. 6 Peak current difference in buck converter and proposed converter

Assuming turn – off time is 20ns, switching frequency is 350 kHz, the turn – off switching loss of two top MOSFETs in buck converter will be:

$$P_{off} = V_{in} * I_p * t_{off} * f_s = 12 * 25 * 20n * 350k$$

$$= 2.1W$$

The turn – off switching loss of two primary MOSFETs in nonisolated half bridge converter is:

$$P_{off} = V_{in}/2 * I_p * t_{off} * f_s = 6 * 10.5 * 20n * 350k$$

$$= 0.44W$$

Obviously, turn – off switching loss of nonisolated half bridge converter is much less than that of two – phase buck converter, 1.66W loss is saved.

Actually, the proposed converter can also save some turn – on switching loss, but the turn – on switching loss is usually less than 20% of the turn – off switching loss, and it is hard to precisely evaluate as the effect of reverse recovery of the body diode in the synchronous MOSFET.

On the other side, conduction loss is the dominant loss for the secondary side MOSFETs and bottom MOSFETs. In a two - phase synchronous buck converter, the RMS value of each bottom MOSFET roughly equals to:

$$I_{Q\_rms} = \frac{I_o}{2} \cdot \sqrt{1 - D} \qquad (5)$$

In the proposed nonisolated half bridge converter, the secondary side MOSFET's current waveforms was shown in Fig. 4. The RMS value of each secondary MOSFET roughly equals to:

$$I_{Q\_rms} = \frac{I_o}{2} \cdot \sqrt{1 + D} \qquad (6)$$

Duty cycle is extended in the proposed topology. Obviously, RMS value of the current flowing through the secondary side MOSFETs increased. Hence, the conduction loss in nonisolated half bridge converter increases as compared with that in the two – phase synchronous buck converter.

Since there is an extra transformer in the proposed converter and the transformer will dissipate some energy, the magnetic losses of the proposed converter, which included inductor losses and transformer losses, will increase too.

The overall efficiency of the proposed converter is still improved since the switching loss is reduced so dramatically.

An example was taken for this loss analysis. The

input voltage is 12V, output voltage and current is 1V/30A. IRF7821 was selected as primary and top MOSFETs, and FDS7088N7 was selected as secondary side and bottom MOSFETs, the secondary inductor is 250nH. The calculation results indicate that the efficiency is improved about 2% ~ 3%. Figure 7 illustrates the breakdown of the losses in the proposed nonisolated half bridge converter (NHB) and a two-phase buck converter (Buck).

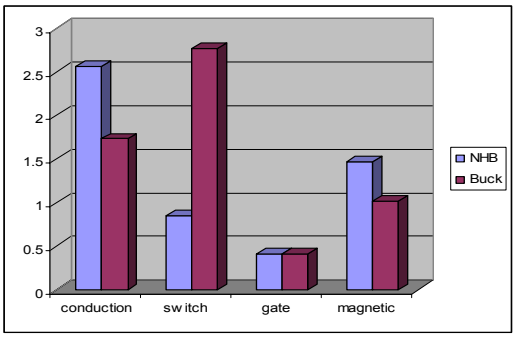


Fig. 7 Loss comparisons between proposed converter and two-phase buck converter

VI. VERIFICATION

A 12V - input, 1V/30A output prototype was built. For comparison, a two - phase interleaving buck was also built with same specification. The switching frequency is 350 kHz. MOSFET IRF7821 (R_{dson} = 9 mΩ, Q_g = 15.3 nC) was selected as the primary switches and top switches; MOSFET FDS7088N7 (R_{dson} = 3 mΩ, Q_g = 37 nC) was selected as the secondary side switches and bottom switches. RM4 planar cores and PCB windings are employed to build a transformer with 2:1 turns ratio and two 250 nH inductors. 12 layers PCB was designed and built.

The prototype and typical waveforms are illustrated in Fig. 8 and Fig. 9 respectively. Fig. 9(b) indicates that the gate - source of the primary low side MOSFET is negative biased when it is turned off. This negative voltage can turn off the MOSFET faster, so the turn – off switching loss can be reduced.

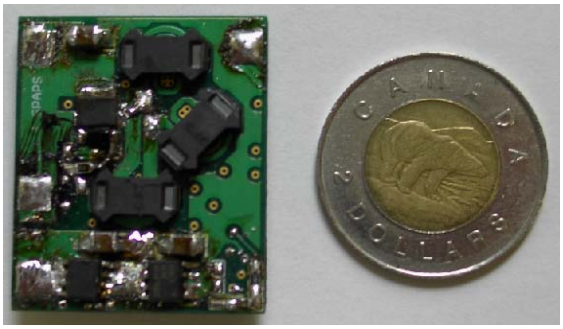
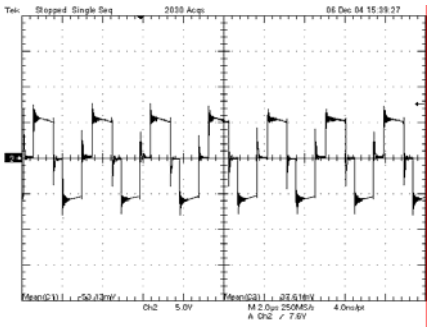
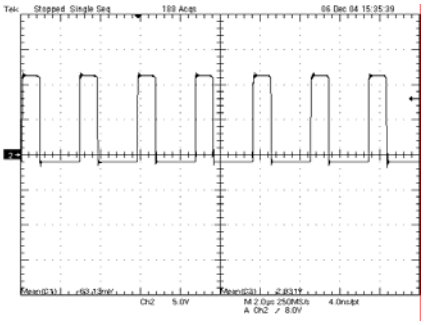


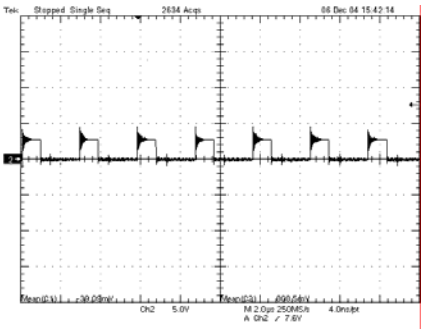
Fig. 8 Prototype of nonisolated half bridge converter



(a) Voltage across primary winding of the transformer



(b) Gate-source voltage of primary low side MOSFET



(c) Drain-Source voltage of synchronous MOSFET

Fig. 9 typical waveforms

Fig. 10 shows their measured efficiency. It is shown that the proposed nonisolated half bridge converter has more than 2% higher efficiency than the synchronous buck converter.

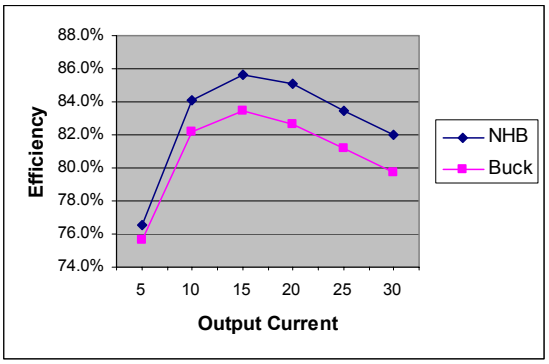


Fig. 10 Measured prototypes' efficiency

VII. CONCLUSIONS

Synchronous buck converter is a widely adopted solution for today's high current low voltage telecom and microprocessor power supplies. When the switching frequency goes up and the output voltage goes down, this topology faces severe challenges as its duty cycle becomes extremely small. A novel nonisolated half bridge topology is proposed in this paper. It can extend the converter duty cycle, so the dynamic performance can benefit from it. The overall efficiency of the converter also improved. The voltage stress of the primary switches is lower than the input voltage, so the low voltage rate MOSFETs can be used and the converter performance may benefit from this. A 12V input, 1V/30A output converter was built to illustrate the above advantages.

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