A new resonant gate drive circuit with centre-tapped transformer

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***Abstract* – This paper presents a new resonant gate drive circuit for a pair of low side switches with 50% duty cycle or less, which is suitable for variable frequency resonant converter, push-pull converter and so on. A centre-tapped transformer is utilized to boost switches' gate voltage twice high as Vcc voltage. Charging and discharging the gate input capacitance by a constant current source increases MOSFETs switching transition speed. The theoretical analysis and simulation waveforms are provided. A prototype board working at 1MHz is built and experimental results are also given.**

I. INTRODUCTION

With the development of computing and telecom technologies in recent years, high power density is increasingly required in switching power supply design. It has been a trend that switching frequency is moving up to above Megahertz region. Along with benefits from higher operating switching frequency in power supply, such as compact size and faster loop respond, it also brings several drawbacks. Increasing gate drive loss is one of them since it is frequency related loss. A conventional gate driver circuit shown in Fig. 1 is widely used in current power converters, including a totem-pole pair of driving mosfets, Q1 and Q2, and optional resistor that is omitted in some applications between the driving mosfets and Power MOSFET, M. Triggered by PWM signal, driving mosfets, Q1 and Q2 are switched to provide the paths to charge and discharge effective capacitance, C_g of Power MOSFET. The total gate capacitive loss can be defined as:

$$P_g = C_g \cdot (V_{CC})^2 \cdot f_S \qquad (1)$$

Where C_g is effective capacitance of power MOSFET, f_S is the switching frequency. V_{CC} is the voltage of power source.

The equation (1) shows that total charge stored in effective capacitance is proportional to the switching frequency and is completely dissipated by the gate driver. With higher frequency application, it may cause gate driver itself destroyed by overheat. Also, the gate loss takes a considerable share in total power dissipation. In some case, gate loss is compatible to the conduction loss [1]. Efficiency of converters is degraded significantly. Moreover, the conventional gate driver cannot meet the requirement of switch speed in high frequency application. Fast switching transition is crucial for performance of power converters, especially for low voltage, high current output converters. It can reduce switching loss and conduction loss as well. However, the conventional gate driver operation is based on R-C charge and discharge. Turn-off transition takes quite longer time as the voltage on gate capacitance is discharged down and discharging current becomes much smaller than its peak value. Consequently, longer turn-off transition occurs, which is not desire to reduce the switching loss and conduction loss. In order to increase the speed of switching transition paralleled gate drivers are employed in some cases. But this results in component cost increased.

The issues of the conventional gate driver are posing to the power designers and researches. Many attempts have been made to recover gate loss energy [1]-[8]. But most efforts only focused on single circuit to drive single MOSFET. Also, some of control signals are difficult to generate.

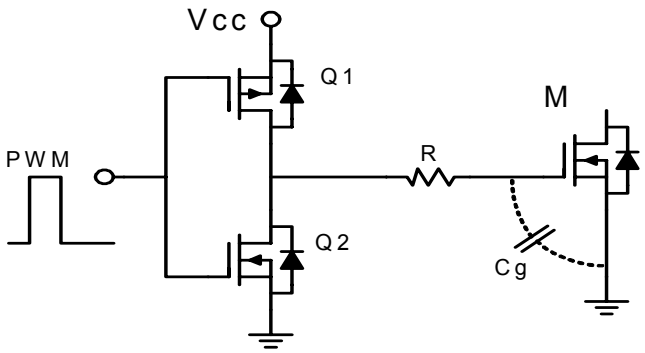

Fig. 1 Conventional gate driver

In this paper, a new resonant gate drive circuit is proposed and its operating principle is described in section II. Section III covers the loss analysis. Design guideline is also introduced. Simulation and experimental results are given in section IV. Finally, conclusion is drawn in section V.

II. PROPOSED RESONANT GATE DRIVE CIRCUIT

Fig. 2 shows the proposed resonant gate drive circuit. It consists of three driving mosfets, S1-S3 and a centre-tapped transformer. Centre of transformer is connected to power source, V_{CC} through S3. M1 and M2 are power MOSFETs. C_g represents effective capacitance of power MOSFETs.

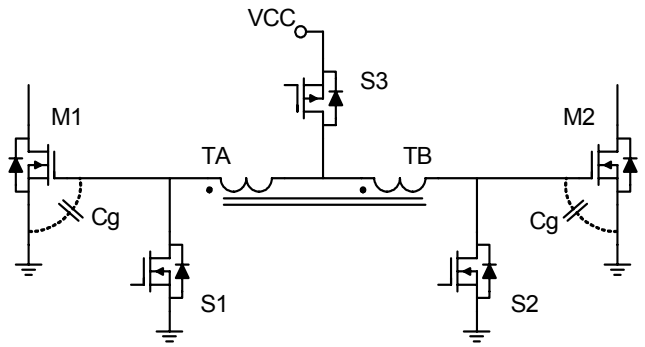

Fig. 2 Proposed resonant gate drive circuit

In Fig. 2, S1 and S2 are N-channel mosfets. S3 is a P-channel mosfet. Turn's ratio of two windings TA and TB of transformer is 1:1. Fig. 3 shows the key operating

waveforms. Fig. 4 illustrates the circuit operation in each stage.

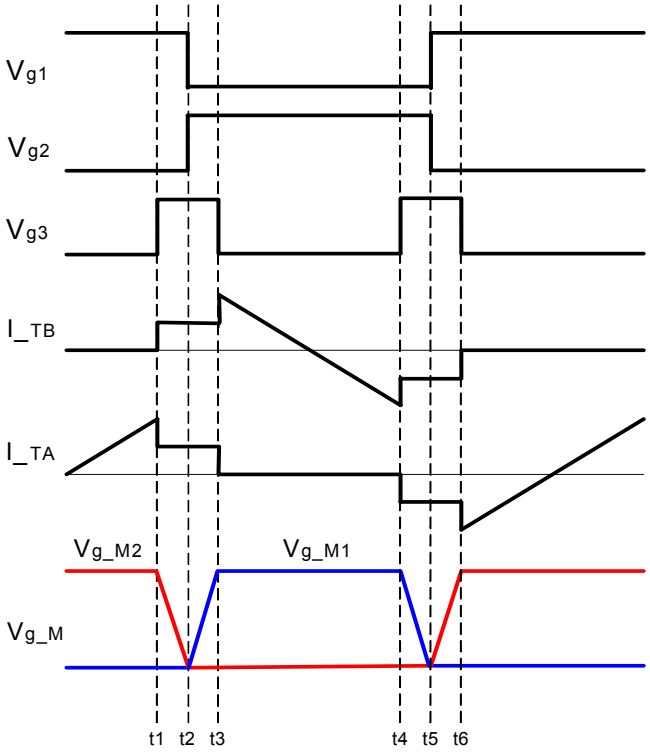

Fig. 3 Operating waveforms

Assume initially, before t1, S1 and S3 stay on. Power MOSFET M1 is off, whereas M2 is on. Winding TA of transformer is linearly charged. A voltage is induced in winding TB, which is piled up with the voltage of winding TA to drive gate voltage of M2 up to twice of Vcc voltage.

At t1, M2 switch off signal arrives. S3 is turned off. Magnetizing current keeps same direction flowing; half of amount of current circulates into the winding TA, which induces the current in winding TB. The other half amount of current keeps same direction flowing through S1, Cg of M2, TB, and then returns TA. Cg of M2 is discharged by an approximate current source at the amount of half of peak magnetizing inductance current. As long as the voltage on Cg of M2 is discharged below the threshold, M2 is turned off. Voltage on Cg of M2 continues to be discharged to zero, body diode of S1 conducts the current and S2 can be turned on at ZVS.

At t2, S2 is turned on at ZVS and S1 is turned off. Magnetizing current continues to flow, now, to charge the Cg of M1. The voltage across each winding of transformer keeps increasing as Cg is charged up until the voltage on winding TB climb over Vcc voltage. At the moment, body diode of S3 starts conducting current, centre voltage of transformer is clamped at Vcc + body diode drop on S3. The maximum voltage on gate voltage of M is consequently clamped at two times of centre voltage, Vcc + body diode drop on S3. Since body diode of S3 is conducted, switch S3 can be turned at ZVS.

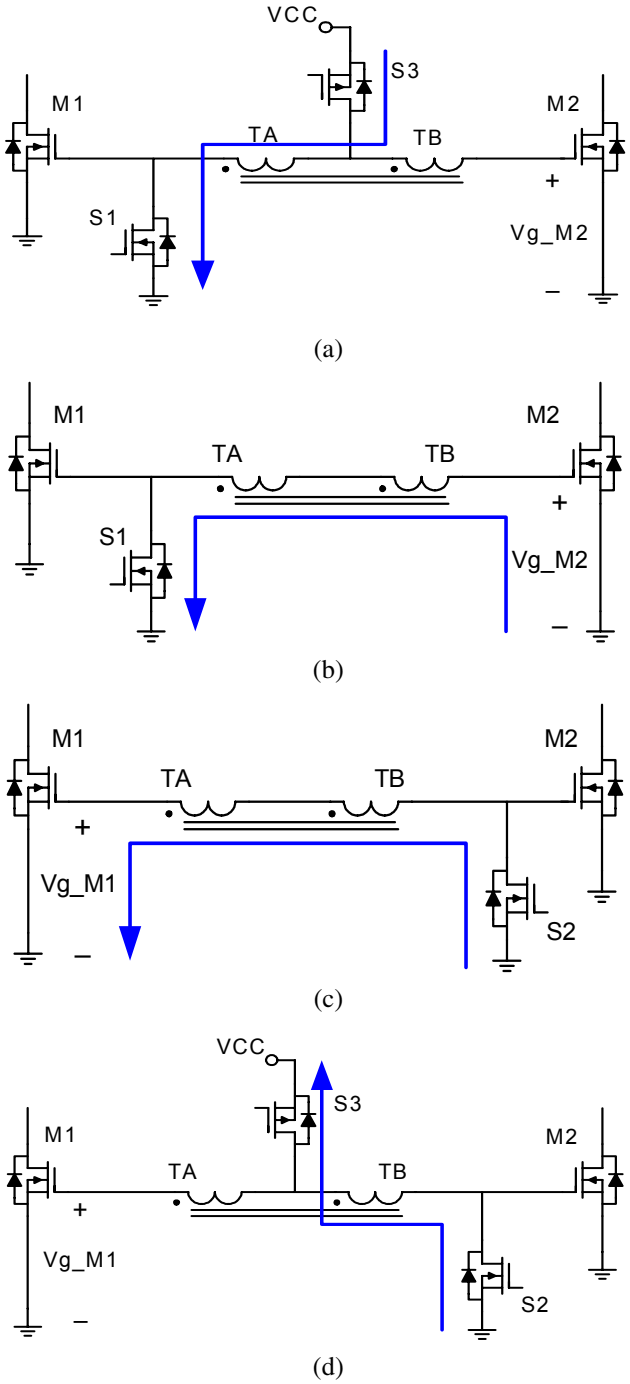

Fig. 4 Operation stages: (a) M1 turned off and M2 turned on (before t1), (b) M2 turning off (t1~t2), (c) M1 turning on (t2~t3), (d) M2 turned off and M1 turned on (after t3).

At t3, with an appropriate time delay from t2, S3 is turned on at ZVS. Then winding TB is linearly charged. Gate voltage of M1 is boosted to twice of Vcc voltage.

Operating principle in the other half switching period (from t4 to t6) works the same as from t1 to t3 except that the direction is reversed.

By controlling the timing of S1 and S2, gate voltages of a pair of power MOSFETs can be arranged as overlap mode, critical mode and delay mode to satisfy different kinds of application. Operation mode shown in Fig. 3 is critical mode

where one power MOSFET is turned on right after the other one is turned off.

In this paper, a new resonant gate drive circuit is proposed. Effective capacitances of power MOSFETs are charged and discharged by a constant current source to recover gate charge energy. The constant current source also speeds up switching transition, especially for the turn-off transition. A centre-tapped transformer is utilized to obtain gate voltage as high as twice of source voltage. This advantage allows gate voltage to reach a decent voltage level even power source voltage locates at logic voltage level, 2.5V for example. For some telecom applications in which no 12V intermediate bus and output rail sets at 2.5V or 3.3V, by using this gate driver, gate voltage of MOSFET in the circuit powered by output rail can reach relatively high level without an extra circuit. Also control logic signals of proposed circuit are simple and very easy to design and implement.

III. ANALYSIS AND DESIGN GUIDELINE

(1) Loss distribution

The total losses of proposed resonant gate drive circuit are distributed to conduction loss, driving loss and transformer core loss. That is:

$$Pgr = P_{rms} + P_{drive} + P_{core} \quad (2)$$

Among the total losses, conduction loss, P_{rms} is the major loss. As stated in section II, a triangle shaped current flows through R_{ds_on} of driving mosfets and winding resistance of transformer during steady state (S3 on and either S1 or S2 on), whereas an approximately constant current that charges and discharges effective capacitance of power MOSFETs flows through both transformer windings and gate resistance, R_g during the transit time. The power dissipation on those resistances when currents flow can be described as following:

$$P_{rms} = I_{ss\_rms}^2 \cdot (2R_{ds\_on} + R_L) + 2 \cdot I_{t\_rms}^2 \cdot (R_g + 2R_L + R_{ds\_on}) \quad (3)$$

Where I_{ss_rms} is the RMS current that flows through transformer during steady state, I_{t_rms} is the RMS current flowing through transformer during transit state. R_L is the winding resistance of transformer. Here assuming S1, S2 and S3 have same R_{ds_on} value. I_{ss_rms} and I_{t_rms} can be derived in (4) and (5):

$$I_{ss\_rms} = \frac{I_{pk}}{\sqrt{3}} \quad (4)$$

$$I_{t\_rms} = \frac{I_{pk}}{2} \cdot \sqrt{\frac{T_t}{T_s}} \quad (5)$$

Where I_{pk} is the peak current of magnetizing inductance current of transformer; T_t is the total transition time during the pair of MOSFETs switching; T_s is the switching period of converter.

In the total conduction losses, Rg loss is main contributor. At range of 1-2 Ω for standard gate resistance of power MOSFET, even the MOSFETs transition period is normally short, the loss on internal gate resistance of power MOSFETs still takes large of share of conduction loss, which gives a significant impact on the efficiency of resonant gate driver. Fig. 5 shows the calculation of gate resistance's impact on loss saving of resonant gate driver.

Since the total gate charge of driving switches is small, driving losses just occupy small part of total loss. Besides, the driving mosfets realize the ZVS, switching loss of those driving mosfets can be neglected. By choosing high frequency core material and optimal turns of transformer windings, the core loss of transformer can be minimized.

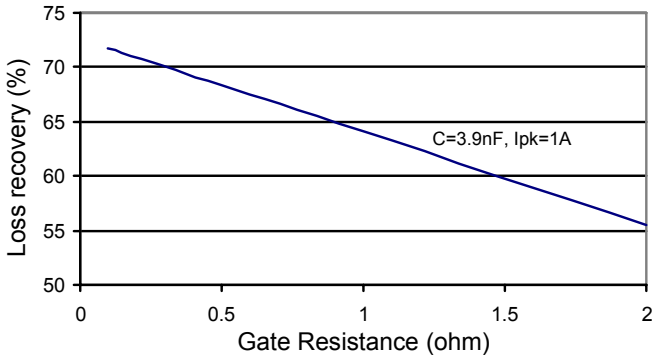

Fig. 5 Calculated gate resistance impact on loss saving

(2) Design guideline

Resonant gate driver is designed not only to recover much of gate energy to improve the driving efficiency, but also to realize the faster driver as well. Faster driver will benefit reducing the switching loss. In this proposed resonant gate drive circuit, the input capacitance of power MOSFETs, Cg is charged and discharged by an approximately constant current during the transit time between two switches, shown in Fig. 3, from t1 to t3. Using a current source to Drive MOSFET can provide much faster driving speed comparing with conventional driver at same current level. It will overcome the drawback of slow turn-off of conventional driver. However, faster driving speed requires higher driving current that may cause conduction loss increase dramatically because of power dissipation on the internal resistance of power MOSFET, Rg. To design this resonant gate driver, the driving speed and driving current are the main parameters to be determined. As discussion above, the trade-off between driving speed and driving current need to be considered. The relationship between speed and driving current is expressed in (6):

$$I_{ped} = \frac{2 \cdot V_{CC} \cdot C_g}{T_t}, \quad I_{ped} = \frac{I_{pk}}{2} \quad (6)$$

Where I_{ped} is pedestal current that charges and discharges effective capacitance of power MOSFET, Cg.

Another consideration to determine the constant driving current is that the setting current may be limited at certain value because voltage across the internal resistance, Rg prevents power MOSFET from turning off. Shown in Fig. 6, S1 is turned off, a constant current, I_{dcg} discharges Cg. It is obvious that when discharge current is high enough, actual gate voltage, Vg of M could be higher than threshold of power MOSFET. Power MOSFET cannot be properly turned off. Shoot-through of a pair of MOSFETs and consequent component failure may occur. For the power MOSFET with

1-2 Ω internal gate resistance and 1.8V threshold voltage, limited driving current is set at 1A to 1.5A. Paralleled mosfets may relax this limitation.

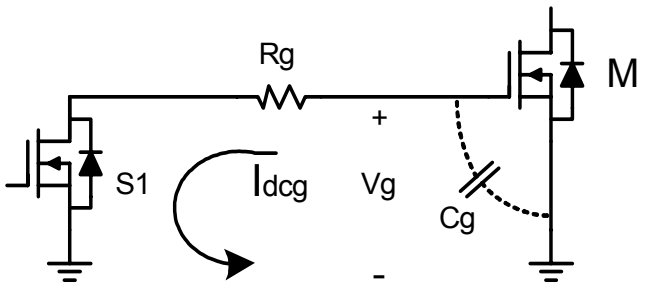

Fig. 6 Equivalent discharge circuit

When the pedestal current is determined, the magnetizing inductance can be obtained in the equation (7):

$$L_m = \frac{V_{CC} \cdot \left(\frac{T_S - T_t}{2} \right)}{2 \cdot I_{pk}} \qquad (7)$$

Where L_m is magnetizing inductance of transformer.

In high frequency application (greater than 1MHz), magnetizing inductance is normally small at range of a few hundred nano-henries. Air coil could be an option, which eliminates core loss of transformer. The centre-tapped transformer also can be made as a coupled inductor to get comparatively lower leakage inductance by a bifilar wire winding construction.

IV. SIMULATION AND EXPERIMENTAL RESULTS

A computer simulation has been done to verify the proposed resonant gate driver circuit. Fig. 7 gives logic circuit block used in simulation and experiment. The simulation results shown in Fig. 8 and Fig. 9 show the simulation result at switching frequency of 1MHz and 2MHz respectively. Simulation condition is listed as following:

Source voltage is 5V. Switching frequencies are set at 1MHz and 2MHz and corresponding magnetizing inductances are 900nH and 250nH respectively. 3.9nF capacitor is used to simulate equivalent gate capacitance of MOSFET. It is assumed no leakage inductance in the simulation.

A prototype was built. The voltage of power source is 5V and clock frequency is set at 1MHz. All the logic circuit was using discrete gate components. A toroid core (T44-15) from Micrometals is used for centre-tapped transformer in which a bifilar wire winding construction is employed to minimize the leakage inductance of transformer. Magnetizing inductance is 900nH. Mosfets with small total gate charge are chosen for S1 to S3, where FDN335N from Fairchild is selected for S1, S2 and FDN308P is selected for S3.

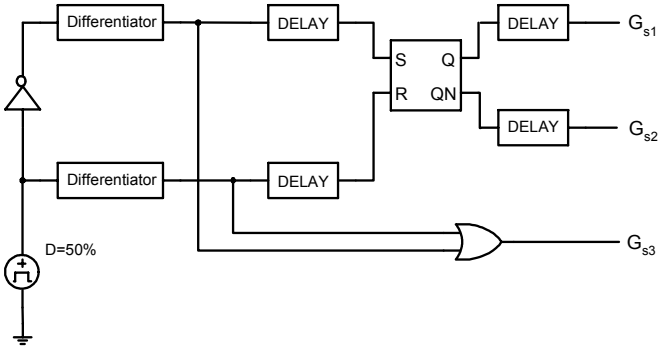

Fig. 7 Logic control block for resonant gate driver

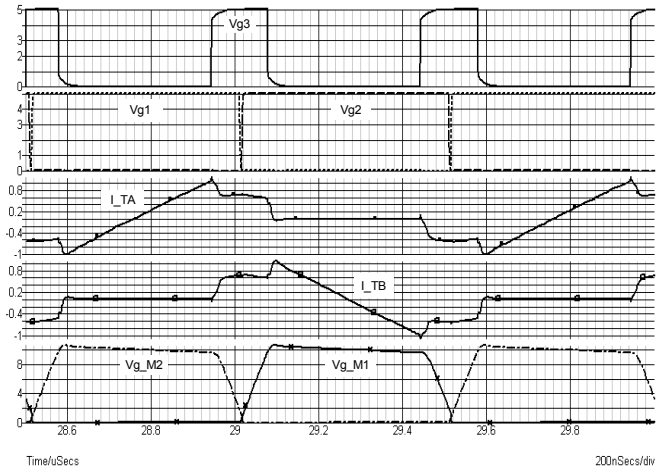

Fig. 8 Simulation results (fs = 1MHz)

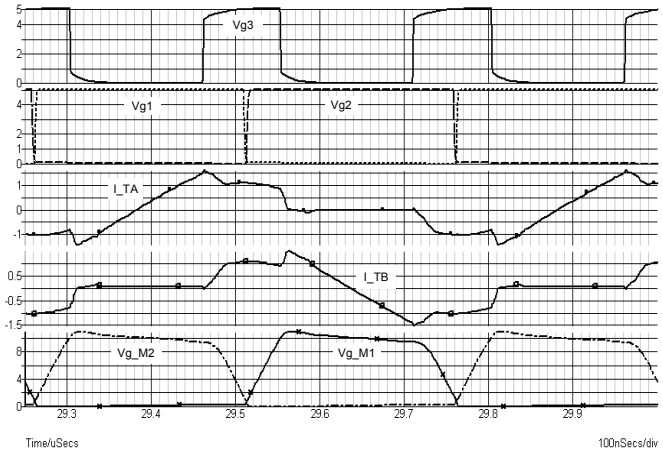

Fig. 9 Simulation results (fs = 2MHz)

Two conditions are tested. One is using 3.9nF ceramic capacitor as circuit load with a resistor in series to simulate internal resistance of MOSFET, R_g; the other is resonant gate driver circuit drives two paralleled mosfets on each side. FDS4410 is selected as Power MOSFET. Fig. 10 and Fig. 11 show the result waveforms for two cases respectively. Both cases are working as overlap mode. The ringing on gate voltage, V_{g_M} is cause by the leakage inductance of transformer. The gate voltages are boosted to about 10V, twice of source voltage, 5V.

For the case of capacitor load, a resistor is connected to capacitor in series to represent internal gate resistance of

Mosfet. Also the resistor damps the circuit to obtain the steady value. For Fig. 10, the series resistance is 0.22Ω and actually measured loss of circuit is 255mW. The total loss for conventional driver is 712mW. Then the loss saving is 64%. Loss saving under different series resistor is also measured. Fig. 12 characterizes energy saving of the resonant gate driver with different series resistor that presents the gate resistance. The measured loss saving for capacitor load matches the calculation result shown in Fig. 5. There is about 7% error between the calculation and the measured results.

For the case of MOSFETs load, typical gate capacitance obtained from curve in datasheet is used to calculate the circuit loss saving that is 48%, where total gate loss is 514mW and circuit loss is 267mW.

From experimental results, it can be observed that the internal gate resistance of MOSFET has a great impact on the performance of resonant gate driver.

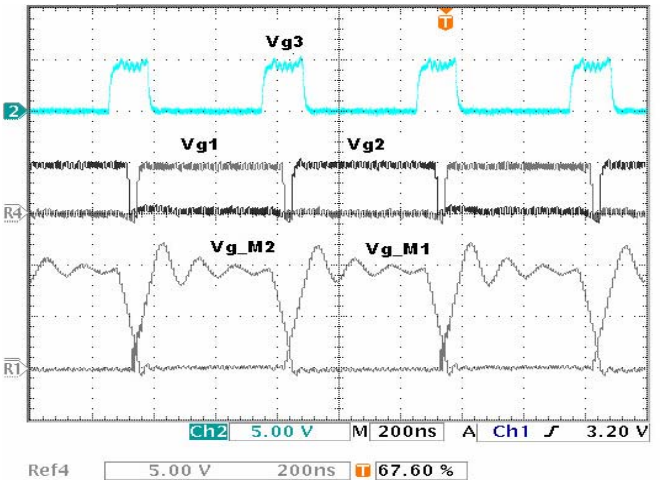

Fig. 10 Experiment 1: using capacitor as load

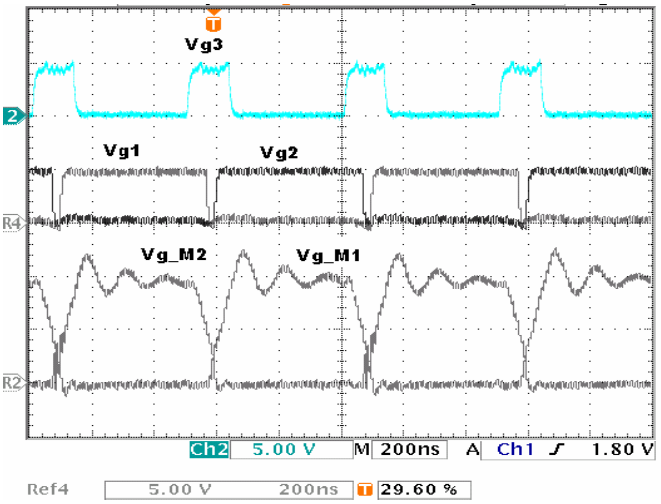

Fig. 11 Experiment 2: using MOSFETs as load

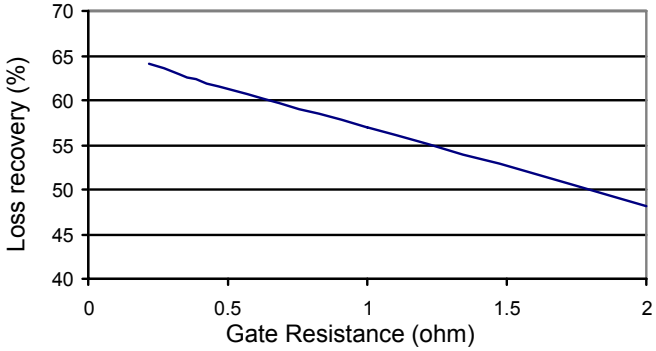

Fig. 12 Measured loss recovery with different gate resistances

V. CONCLUSION

This paper presents a new resonant gate drive circuit that is suitable for a pair of low side MOSFETs with 50% duty cycle or less. A centre-tapped transformer is utilized to obtain gate voltage as high as twice of source voltage. This advantage allows gate voltage to reach a decent voltage level when power source voltage is at lower logic voltage level. An approximate constant current is utilized to drive the MOSFET to achieve higher driving speed and also recover gate drive energy while the conventional driver loses all of them. From the experimental result, the internal gate resistance has significant impact on the resonant gate driver's performance. With improvement of gate resistance of MOSFET, resonant gate driver will benefit from it, saving more gate drive energy.

Since the transformer is used, by adding two more winding, the application can be extended to drive high side MOSFETs in full bridge or half bridge for variable frequency resonant converter. Further research will be conducted.

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