A New Digital Control Algorithm to Achieve Optimal Dynamic Performance in DC-to-DC Converters

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Abstract - **In this paper, a new optimal control algorithm is proposed to achieve the best possible dynamic performance for DC-to-DC converters under load changes and input voltage changes. Using the concept of capacitor charge balance, the proposed algorithm predicts the optimal transient response for a DC-to-DC converter during the large signal load current change, or input voltage change. The equations used to calculate the optimized transient time and the optimized duty cycle series are presented. By using the proposed algorithm, the best possible transient performance, including the smallest output voltage overshoot/undershoot and the shortest recovery time, is achieved. In addition, since the large signal dynamic response of power converters is successfully predicted, the large signal stability is guaranteed. Experimental results show that the proposed method produces much better dynamic performance than a conventional current mode PID controller.**

I. INTRODUCTION

Recently, there has been an increasing demand for high dynamic performance power converters. Among the many criteria of dynamic performance, output voltage overshoot and recovery time are often considered the most important. In general, the output voltage deviates under load change, or input voltage change. The value of output voltage deviation depends on the filter inductor and capacitor values in the powertrain, and the switching frequency and control algorithm. If the inductor, capacitor and switching frequency are fixed, different control algorithms achieve different dynamic performance. Some work has been done to improve the dynamic performance of power converters [1]-[3]. However, these methods cannot guarantee the best possible dynamic performance.

In theory, for any specific power converter and its related parameters, there exists a best possible dynamic performance (minimum overshoot and/or minimum recovery time) under a load current change, or input voltage change. If we can determine the best possible transient response and a method to realize it, the dynamic performance can be greatly improved. Therefore, it is not only necessary but also practical to explore the best possible dynamic performance for power converters.

In this paper, a new digital optimal control algorithm is proposed to achieve the best possible dynamic performance for DC-to-DC converters. The proposed method uses the principle of capacitor charge balance to predict the necessary minimum number of switching cycles and their appropriate duty cycles to drive the output voltage back to its nominal value during a transient condition. In section II, the transient response of a buck converter under voltage mode control is analyzed in order to outline the deficiencies of conventional linear control techniques. In section III, the optimal transient response algorithm is proposed. This is followed by the derivation of the equations to implement the proposed method in section IV. Experimental results are presented in section V and the conclusions are presented in section VI.

II. LIMITATIONS OF CONVENTIONAL CONTROL METHODS DURING A LOAD TRANSIENT

Since the dynamic performance under a load current change is one of the most important issues in power converter design, the transient response of a power converter under a large signal positive load current change will be fully discussed. In this section, the transient response of a buck converter (Fig. 1) under voltage mode control is analyzed.

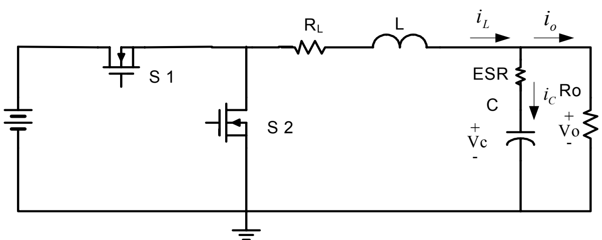


Fig. 1 Synchronous buck converter

The dynamic response waveforms of a voltage mode controlled buck converter under positive load current step change are illustrated in Fig. 2. In the beginning, the load current steps from i_{o1} to i_{o2} at point 0. It is assumed that before point 1, the output voltage drop has not been sensed by the control circuit. Therefore, the duty cycle remains constant. As a result, the inductor current remains unchanged during the period t_0. Then, since the load current is greater than the inductor current, the capacitor discharges to provide the required load current. As a result, the capacitor and output voltages decrease. At point 1, the output voltage drop is sensed by the control circuit. Then, with voltage mode control, the duty cycle increases, which causes the inductor current to increase. However, before point 2, the inductor current is lower than the load current. As a result, the capacitor voltage continues to decrease. At point 2, the inductor current is equal to the load current, so then the capacitor stops discharging. At this point, the capacitor voltage drop is at its maximum.

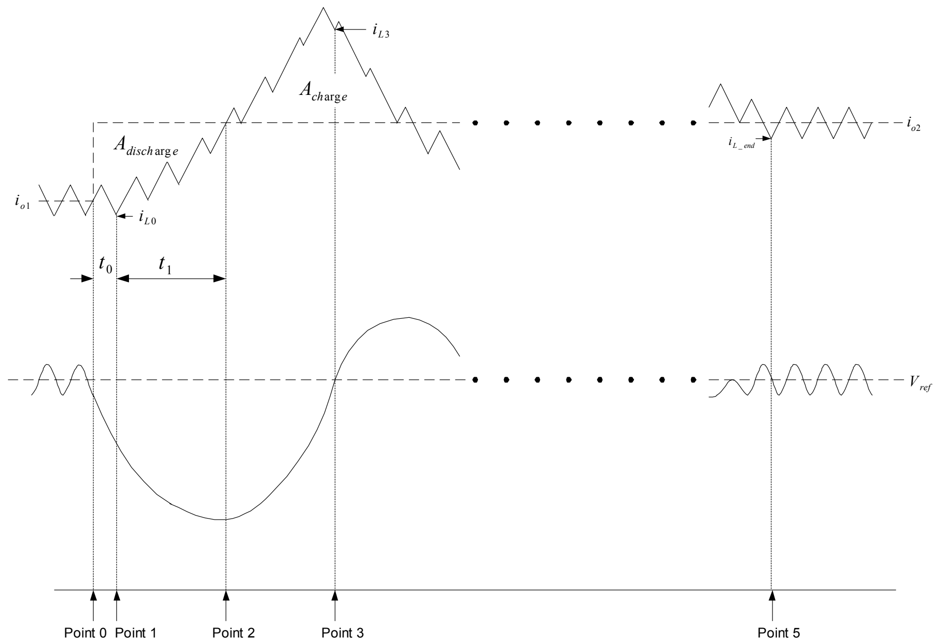


Fig. 2 Transient response of a voltage mode controlled buck converter under positive load current step change (top: inductor current, bottom: capacitor voltage)

It can be observed from Fig. 2 that under voltage mode control, the duty cycle is not 100% during t_1. As a result, the inductor current cannot increase at its maximum slew rate. Therefore, the time period, t_1, for the inductor current to rise above the load current is not minimized. It can be clearly observed from Fig. 2 that the discharge area, $A_{discharge}$, is not minimized. Since the value of $A_{discharge}$ determines the maximum capacitor voltage drop during the transient, the maximum capacitor voltage drop is not minimized.

After point 2, the inductor current continues to increase and becomes greater than the load current. As a consequence, the capacitor is recharged and the capacitor voltage rises up towards the nominal value V_{ref}. When the value of capacitor charge, A_{charge}, is equal to the capacitor discharge, $A_{discharge}$, the capacitor voltage reaches its nominal value, V_{ref}, shown as point 3. However, using voltage mode control or other conventional linear control methods, the inductor current is usually not equal to the new steady state inductor current value at this point. Therefore, in the switching period after point 3, the capacitor current is non-zero. Therefore, the output voltage is not equal to the nominal value, V_{ref}. Furthermore, since the capacitor current is non-zero, the capacitor continues to charge or discharge. As a result, the capacitor and output voltages continue to change and the converter remains in the transient state. If the voltage mode controller is designed to make the system stable, the converter will enter the new steady state several switching cycles later at point 5. This analysis indicates that voltage mode control cannot achieve the best possible dynamic performance.

Generally speaking, the design objectives for voltage mode control, or other conventional linear control methods are to make the steady state error converge to zero and to achieve wide bandwidth with sufficient phase margin. However, these objectives cannot guarantee minimum overshoot and transient time for load current changes or input voltage changes. Therefore, to achieve the best possible dynamic response, a new advanced control algorithm is needed.

III. PROPOSED OPTIMAL TRANSIENT RESPONSE ALGORITHM

When load current changes, different control methods generate different duty cycle series allowing the output voltage to recover. As a consequence, their transient performances are different. However, for a given set of power converter parameters, there exists a control method to generate an optimized duty cycle series, which can drive the power converter system to achieve the minimum overshoot and/or minimum transient time under a large signal load current change.

From the analysis presented in section II, it can be clearly seen that if the following necessary and sufficient conditions are satisfied, the best possible dynamic performance will be achieved:

1) At the beginning of the transient, the inductor current should rise at its maximum slew rate. When the inductor current reaches its peak value, it should drop at its maximum slew rate.
2) When the charge delivered to the capacitor is equal to the charge delivered by the capacitor, the inductor current reaches its new steady state value and the transient ends.
3) When the transient ends, the duty cycle for the next

switching cycle will be set to its new steady state value.

Fig. 3 illustrates the waveforms of the inductor current and capacitor voltage under a positive load current change when the best possible transient response satisfies the above conditions. In the beginning, the load current changes from i_{o1} to i_{o2} at point 0. In a digitally controlled buck converter, the output voltage is sensed each switching cycle. Assuming that at point 1, the output voltage deviation exceeds a predefined level, the control system judges that the buck converter has entered a large signal response period, so then, the optimal control algorithm is activated. Under the optimal control algorithm, the inductor current is forced to follow the proposed optimal transient waveforms. Specifically, the proposed best possible transient under positive load current change consists of two periods, the optimized inductor current rising period, t_{up}, and the optimized inductor current falling period, t_{down}.

During t_{up}, the duty cycle is set at 100%, so that the inductor current increases at its maximum slew rate. t_{up} is composed of two intervals t_1 and t_2. During t_1, the inductor current is lower than the load current. During t_2, the inductor current is higher than the load current. At the end of interval t_{up}, the inductor current reaches its peak value, i_{L3}, at point 3.

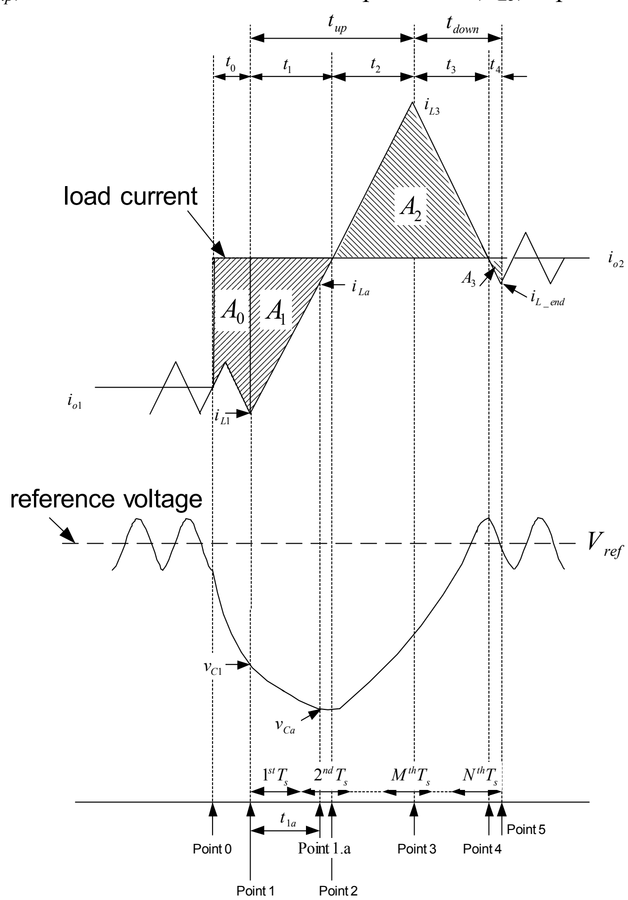


Fig. 3 Optimal inductor current transient for load current positive change when $t_{opt} = NT_s$ (top: inductor current, bottom: capacitor voltage)

After point 3, the transient process enters the optimized inductor current falling period, t_{down}. During this interval, the duty cycle is set at 0%, so that the inductor current drops at its maximum slew rate. t_{down} is composed of two intervals t_3 and t_4. During t_3, the inductor current is greater than the load current. During t_4, the inductor current is lower than the load current. At point 5, the inductor current reaches its new steady state value, i_{L_end}, and at the same time, the charge delivered to capacitor is equal to the charge delivered by the capacitor, so the transient ends.

If the inductor current and capacitor voltage follow this path, the best possible dynamic performance including minimum undershoot and transient time is achieved.

IV. Derivation of the Optimal Control Algorithm for Practical Implementation

The dynamic equations of the synchronous buck converter can be expressed by (1)-(3).

$$\frac{di_L}{dt} = \frac{v_{in} - v_o'}{L} \quad (1)$$

Equation (1) is applicable when S1 is on and S2 is off.

$$\frac{di_L}{dt} = \frac{-v_o'}{L} \quad (2)$$

Equation (2) is applicable when S1 is off and S2 is on.

$$C\frac{dv_C}{dt} = i_c = i_L - i_o \quad (3)$$

In (1)-(3), v_{in} represents the input voltage, v_c represents the capacitor voltage, i_c represents the capacitor current, i_L represents the inductor current, i_o represents the load current and v_o' represents the equivalent output voltage including the system losses. v_o' is given by (4), which includes the output voltage, v_o, and system loss, r_{loss}.

$$v_o' = v_o + i_o r_{loss} \quad (4)$$

The output voltage is given by (5), where *ESR* represents the equivalent series resistance of the filter capacitor.

$$v_o = v_C + i_C ESR \quad (5)$$

r_{loss} is expressed as (6), where R_L represents the winding resistance of the filter inductor, R_{on} represents the MOSFET on resistance and $R_{switching}$ represents the MOSFET switching loss.

$$r_{loss} = R_L + R_{on} + R_{switching} \quad (6)$$

The key point to achieve the optimal transient response is to precisely predict the rising and falling periods of the transient, t_{up} and t_{down}. Calculating t_{up} and t_{down} requires values for i_L, v_o and i_o. In real time implementation i_L and v_o can be directly measured, however i_o must be estimated.

In the proposed optimal control algorithm, the optimized transient time can be calculated in six steps:

1) Estimating the new load current i_{o2}
2) Calculating the inductor current rising and falling slew rates
3) Calculating the capacitor discharge portion A_0
4) Calculating t_1 and the capacitor discharge portion A_1
5) Calculating t_4 and the capacitor discharge portion A_3

6) Calculating the capacitor charge A_2 and the time periods t_2 and t_3

In order to simplify the calculations, three assumptions are made:

1) During the transient, the output voltage variation is small, so it can be assumed that the output voltage is approximately equal to V_{ref}.
2) After point 1, the load current remains constant at i_{o2}.
3) The input voltage remains constant during the transient.

These assumptions are usually true in real applications. Using these assumptions, the equations to calculate the optimized transient time are given as follows:

Step 1: Estimating the new load current i_{o2}

To estimate the new load current value, the output voltage, v_{o1}, the inductor current i_{L1} at point 1, the output voltage, v_{oa}, and the inductor current, i_{La} at point 1.a are sensed. During the time interval, t_{1a}, the change of output capacitor charge can be written as (7), and re-written as (8)

$$C\Delta v_C = C(\Delta v_0 - \Delta i_C ESR) \tag{7}$$

$$\begin{aligned} C\cdot\Delta v_C &= C\cdot[(v_{0a}-v_{o1})-(i_{Ca}-i_{C1})\cdot ESR] \\ &= \int_{po\text{ int }1}^{po\text{ int }1.a}(i_L - i_{o2})\cdot dt \end{aligned} \tag{8}$$

In (8), i_{Ca} and i_{C1} are the capacitor current at point 1 and point 1.a. Since i_{C1}=i_{L1}-i_{o2}, i_{Ca}=i_{La}-i_{o2}, and i_{C2}-i_{C1}=i_{La}-i_{L1}, then, (8) can be rewritten as (9).

$$C\cdot(v_{0a}-v_{o1}) = \frac{1}{2}(i_{L1}+i_{La})\cdot t_{1a} - i_{o2}\cdot t_{1a} + (i_{La}-i_{L1})\cdot C\cdot ESR \tag{9}$$

From (9), the new load current i_{o2} can be estimated using (10).

$$i_{o2} = \frac{1}{2}(i_{L1}+i_{La}) - \frac{C\cdot(v_{0a}-v_{o1}) - C\cdot(i_{La}-i_{L1})\cdot ESR}{t_{1a}} \tag{10}$$

Step 2: Calculating the inductor current rising and falling slew rates

Considering the losses of the power stage, the inductor current rising and falling slew rate can be obtained from (1) and (2) respectively. Here, for simplicity, an approximation is made that during the transient, so (11) is obtained.

$$v_o' \approx V_{ref} + i_{o2}\cdot r_{loss} \tag{11}$$

Step 3: Calculating the capacitor discharge portion A_0

The capacitor discharge A_0 can be estimated by using the change of the capacitor voltage during the time period t_0. Assuming that the capacitor voltage ripple is very small, the capacitor discharge A_0 can be obtained using (12).

$$\begin{aligned} A_0 &= C\cdot(v_{C0}-v_{C1}) \approx C\cdot(V_{ref}-v_{C1}) = C\cdot(V_{ref}-v_{o1}+i_{C1}\cdot ESR) \\ &= C\cdot(V_{ref}-v_{o1}+(i_{L1}-i_{o2})\cdot ESR) \end{aligned} \tag{12}$$

Step 4: Calculating t_1 and the capacitor discharge portion A_1

Based on the estimated load current i_{o2} and the inductor current rising slew rate given by (1), the interval t_1 and the capacitor discharge A_1 can be obtained by using (13) and (14).

$$t_1 = \frac{i_{o2} - i_{L1}}{(v_{in} - v_o')/L} \tag{13}$$

$$A_1 = \frac{1}{2}t_1(i_{02} - i_{L1}) \tag{14}$$

Step 5: Calculating t_4 and the capacitor discharge portion A_3

When the transient ends, the new steady state duty cycle can be obtained using (15).

$$D_{new} = \frac{v_o'}{v_{in}} \tag{15}$$

Then, the value of the new steady state inductor current ripple can be expressed as (16).

$$I_{ripple} = (1 - D_{new})\cdot T_s\cdot\frac{v_o'}{L} \tag{16}$$

Therefore, the new steady state inductor current valley value i_{L_end} is given by (17).

$$i_{L\_end} = i_{o2} - \frac{1}{2}I_{ripple} = i_{o2} - \frac{1}{2}(1-\frac{v_o'}{v_{in}})\cdot T_s\cdot\frac{v_o'}{L} \tag{17}$$

Based on the estimated load current, i_{o2}, the inductor current falling slew rate given by (2) and the new steady state inductor current valley value given by (17), the interval t_4 and the capacitor discharge area A_3 can be obtained using (18) and (19).

$$t_4 = \frac{i_{o2} - i_{L\_end}}{v_o'/L} \tag{18}$$

$$A_3 = \frac{1}{2}t_4\cdot(i_{02} - i_{L\_end}) \tag{19}$$

Step 6: Calculating the capacitor charge A_2 and the time periods t_2 and t_3

In the proposed method, the charge delivered by the capacitor is equal to the charge delivered to the capacitor so (20) is obtained.

$$A_0 + A_1 + A_3 = A_2 \tag{20}$$

In addition, during the time period t_2, the inductor current slew rate is given by (1). During the time period t_3, the inductor current slew rate is given by (2). Then, the capacitor charge area A_2 can be rewritten as (21), where i_{L3} is given by (22).

$$A_2 = \frac{1}{2}(t_2 + t_3)\cdot(i_{L3} - i_{02}) \tag{21}$$

$$i_{L3} = i_{o2} + \frac{v_0'}{L}\cdot t_3 = i_{o2} + \frac{v_{in} - v_0'}{L}\cdot t_2 \tag{22}$$

Using (22), the ratio t_2/t_3 can be derived as (23).

$$t_2/t_3 = \frac{v_o'}{v_{in} - v_o'} \tag{23}$$

Then, using (7), (14), (19) and (21)–(23), the optimal transient time t_2 and t_3 can be derived using (24) and (25).

$$t_2 = \sqrt{\frac{A_0 + A_1 + A_3}{\frac{1}{2}\frac{v_{in}}{v_o'}\frac{v_{in} - v_o'}{L}}} \tag{24}$$

$$t_3 = \frac{v_{in} - v_o'}{v_o'} t_2 \quad (25)$$

By using (13), (18), (24) and (25), the optimal transient time is expressed as (26).

$$t_{opt} = t_1 + t_2 + t_3 + t_4 \quad (26)$$

From the above equations, it can be observed that the proposed optimal transient response method mainly uses division and square root operations to calculate t_1 through t_4. If these two calculation operations are saved and implemented by look-up tables, then the desired optimum control algorithm can be easily implemented using ASICs.

Using the values of t_1, t_2, t_3 and t_4, the minimum number of switching cycles and the duty cycles of each switching cycle can be easily predicted. However, there are two cases for t_{opt}:

1) t_{opt} is an integer multiple of T_s, where T_s is the switching period, which is also the sampling period
2) t_{opt} is not an integer multiple of T_s

In the first case, it is assumed that $t_{opt}=NT_s$, and t_{up} is greater than $(M-1)T_s$ and less than MT_s, where M, N are integers. To achieve the best possible transient response, for the 1st to $(M-1)^{th}$ switching cycle, the duty cycle is 100%. For the M^{th} switching cycle, the duty cycle is given by (27). For the $(M+1)^{th}$ to N^{th} switching cycle, the duty cycle is zero.

$$d = \frac{t_{up} - (M-1)T_s}{T_s} \quad (27)$$

In the second case, t_{opt} is not an integer multiple of T_s. Instead, t_{opt} can be expressed as $t_{opt}=NT_s+t_{residual}$, where $t_{residual}<T_s$ and t_{up} is greater than $(M-1)T_s$ and less than MT_s as shown in Fig. 4. In this situation, the duty cycle values for the 1^{st} to N^{th} switching cycle are the same as that when $t_{opt}=NT_s$. However, for the last $(N+1)^{th}$, switching cycle, an approximate method is used. As shown in Fig. 4, the duty cycle is set to d_{N+1} given by (28), where i_{LN} is the inductor current at the end of switching cycle N. Therefore, the inductor current can still reach its new steady state valley value, i_{L_end}, at the end of the optimized transient response (shown as the solid line shown in Fig. 4). The voltage error caused by this approximation method is very small compared to the output voltage drop during the load current step change. Therefore, its influence can be neglected.

$$d_{N+1} = \frac{v_o T_s + (i_{L\_end} - i_{LN})L}{v_{in} T_s} \quad (28)$$

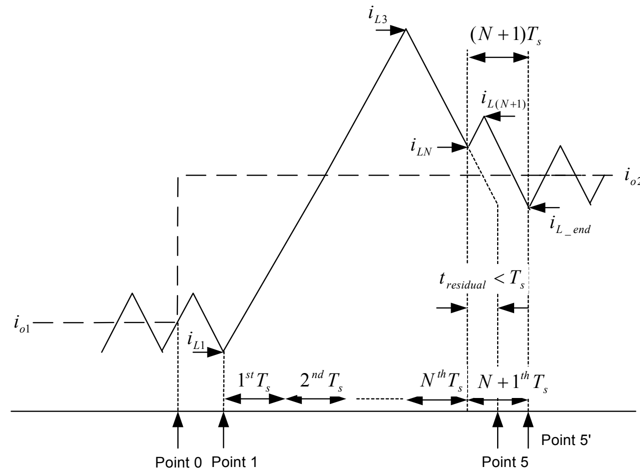


Fig. 4 Optimal inductor current transient for load current positive change when $T_{opt}=NT_s+T_{residual}$

In the proposed control system implemented with a buck converter, a small signal PID controller is used to regulate the power converter during the steady state and any small signal transient response periods. During a large transient, when the large signal optimal transient response algorithm ends at point 5, the control algorithm is switched back to the PID controller. Before the control algorithm is switched back to the PID controller, the optimal control algorithm calculates the new steady state values I_{Lnew} (if current mode control is used) and D_{new} for the PID controller, and resets the outputs of the PID controller to these values.

The value of D_{new} is obtained using (15). Since, in the steady state, the inductor current is sensed $0.3T_s$ before the switch is turned on and the slew rate during MOSFET turn-off period is $-v_o'/L$, the steady state reference inductor current value I_{Lnew} for a current mode PID controller can be obtained using (29).

$$I_{Lnew} = i_{L\_end} + 0.3 \cdot v_o' \cdot \frac{T_s}{L} \quad (29)$$

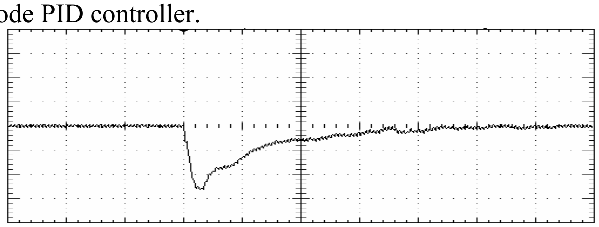
In this section, the equations of the proposed optimal control algorithm were derived for a positive load current change. In order to apply the optimal control algorithm for a negative load current change, or input voltage change, the operation principles and equations are similar to those for a positive load current change.

V. Experimental Results

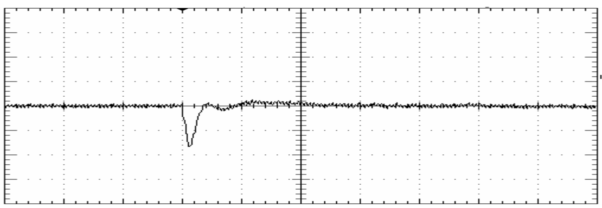
A field programmable gate array (FPGA) was used to implement the proposed optimal control algorithm in a synchronous buck converter. The parameters of the buck converter are listed as follows: $V_{in}=5V$, $V_o=2.5V$, rated load power=25 W, $L=1\mu H$, $C=235\mu F$, ESR=1mΩ and RL=2mΩ and fs=400khz.

A comparison of experimental results for the proposed optimal algorithm and a current mode PID controller is shown in Fig. 5-Fig. 7. The parameters of current mode PID controller were optimized in the frequency domain to maximize the bandwidth at a phase margin of 50º.

It is shown in Fig. 5 that using the proposed optimal control algorithm, the overshoot due to a positive load current step change is decreased by 40% compared with that of the current mode PID controller. The recovery time is significantly reduced to almost 1/10 of that of the current mode PID controller.



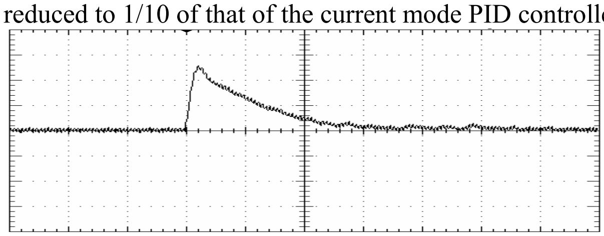
(a) Current mode PID controller



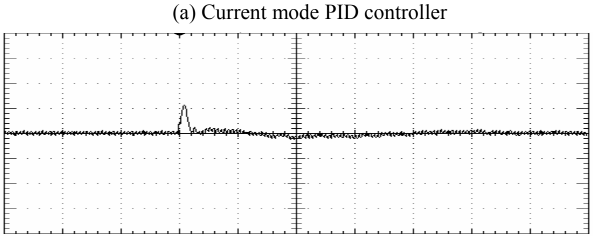
(b) The proposed optimal control algorithm

Fig. 5 Experimental result of output voltage response to load current change from 0A to 5A (X axis: 40us/div; Y axis: 50mv/div)

During a negative load current step change, shown in Fig. 6, using the proposed optimal control algorithm, the overshoot is decreased by 55% compared with that of the current mode PID controller. In addition, the recovery time is reduced to 1/10 of that of the current mode PID controller.



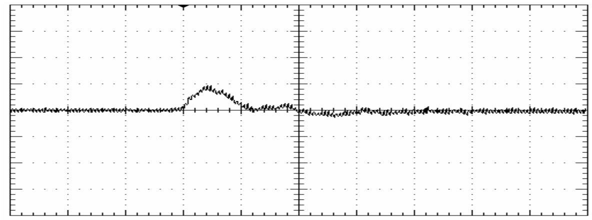
(a) Current mode PID controller



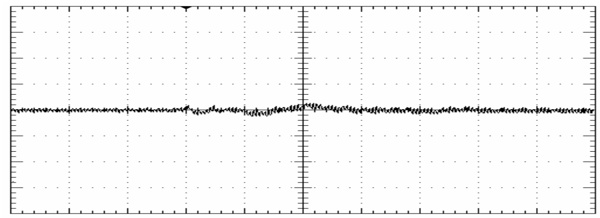
(b) The proposed optimal control algorithm

Fig. 6 Experimental result of output voltage response to load current change from 5A to 0A (X axis: 40us/div; Y axis: 50mv/div)

Under an input voltage step change of 2.5V, shown in Fig. 7, the overshoot of the output voltage is about 45mv with a recovery time of 50μs for the current mode PID controller. By using the optimal algorithm, the overshoot/undershoot during the transient is less than 10mv.



(a) Current mode PID controller



(b) The proposed optimal control algorithm

Fig. 7 Experimental result of output voltage response to input voltage change from 5V to 7.5V (X axis: 40us/div; Y axis: 50mv/div)

It should be noted that if the inductor and capacitor values are not accurate, it will influence the performance of the proposed optimal control algorithm. However, fortunately using +/-20% tolerance for the inductor and capacitor, the dynamic performance of the converter is still very good.

VI. CONCLUSIONS

In this paper, a new optimal control algorithm to improve the dynamic performance of DC-to-DC converters was proposed. Using the principle of capacitor charge balance, the optimal number of switching cycles and their respective duty cycles are predicted in order to drive the output voltage back to its nominal value during the transient. Therefore, the best possible transient performance with minimum overshoot and recovery time is achieved.

Experimental results show that the proposed optimal control algorithm produces much better dynamic performance under load current step changes and input voltage step changes. These results indicate that the proposed algorithm can be an attractive alternative to classic controllers in power converter applications where high dynamic performance is required. Furthermore, the proposed algorithm can be easily applied to other topologies such as the boost and buck-boost converters.

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