A New Non-Isolated Full Bridge Topology for Low Voltage High Current VRM Applications

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***Abstract* - In this paper a new non-isolated full bridge topology is introduced. The primary side of this topology is a full bridge; however, the input voltage ground of the conventional full bridge is connected directly to the positive point of the output and not connected to the input ground. In this arrangement, the input current flows directly to the load without going through the transformer. The secondary side rectifier stage is a current doubler. The primary side can operate in either phase shift soft switching mode or hard switching mode. The advantages of this topology, include soft switching and reduced conduction loss. A 1.41 by 1.41 inch power module has been built and tested to verify the analysis.**

I. INTRODUCTION

With the continued development of integrated circuit technology, next generation CPUs will operate at much higher speeds, and consume more power. According to the Voltage Regulation Module (VRM) road maps [1],[2] next generation CPUs will operate at supply voltages below 1V, with tight voltage tolerance, large current demand (above 100A), and fast dynamic response (above 100A/μs). Therefore, it will be very difficult for conventional buck type topologies to meet all of these requirements.

In this paper, a new non-isolated full bridge topology is proposed, which has significant advantages over conventional buck type topologies, including soft-switching and reduced synchronous rectifier conduction loss. To verify the analysis and demonstrate the advantages of the new topology, a prototype has been built. An efficiency of 84.8% has been achieved at 1V/30A.

II. LIMITATIONS OF THE BUCK TOPOLOGY

In order to minimize power consumption of CPUs, the input voltage of VRMs has increased from 5V to 12V, while their output voltages are presently decreasing to 1V and lower. In traditional designs, a multi-phase buck topology is widely used for VRMs since it has a simple structure and low component cost. By paralleling multiple modules together and phase shifting each module, the output current ripple can be dramatically reduced, so a small inductor can be used and faster dynamic response can be achieved. However, when the output voltage is reduced to 1V or lower, the duty cycle of the buck becomes extremely narrow at approximately 10%.

Small duty cycles have several drawbacks. Small duty cycles cause high peak current through the high side MOSFETs, which dramatically increases switching loss. In addition, small duty cycles degrade the dynamic response, since the available range for the duty cycle to adjust to load, or input voltage change is very narrow. The final disadvantage of small duty cycles is that they reduce the effectiveness of the ripple current cancellation of the interleaved phase shift method.

When buck topologies operate at high switching frequencies, the turn on and turn off times of the high side MOSFETs must be very short to minimize switching loss. This limits its application at high switching frequencies because short turn on and turn off times require high driving current, which makes the driving circuits expensive and difficult to design.

The final disadvantage of the phase shift buck method is that sensing the current of the high side MOSFET with very short conduction time is difficult. This makes controlling several modules to evenly share the output current difficult.

From the preceding analysis, it is clear that the buck topology has many limitations when used in VRM applications. Therefore, topologies with extended duty cycles must be developed in order to solve the limitations of the buck topology. In the next section a new topology will be introduced to solve the aforementioned limitations.

III. ANALYSIS OF THE PROPOSED TOPOLOGY

A new non-isolated full bridge VRM topology is shown in Fig 1. The primary side of this topology is a full bridge, however the bottom point of the conventional full bridge is connected directly to the positive point of the output. In this arrangement, the input current flows directly to the load without going through the secondary side of the transformer. With this arrangement, the current stress of the synchronous rectifiers can be reduced. The secondary side rectifier stage is a current doubler. The primary side can operate in either phase shift soft switching mode, or hard switching mode. For the prototype in this paper, the control method is phase shift.

A. Current and Voltage Stress

In this section the current and voltage stress of this topology is analyzed. All calculation examples are based on a 1V/30A 500KHz application.

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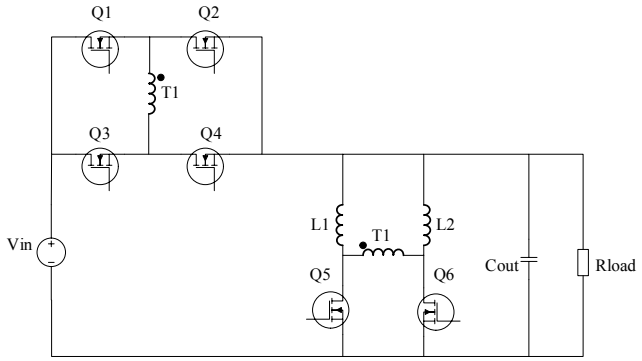

Fig. 1 New non-isolated full bridge topology

If we assume the efficiency is 100% and the current ripple through the inductors is very small, then the voltage transfer ratio of the proposed topology is defined using (1), where $N=Np/Ns$ is the turns ratio. D is the duty cycle, Ns is the secondary turns and Np is the primary turns.

$$V_o = V_{in}\frac{D}{2N+D} \tag{1}$$

The RMS current through the primary MOSFET is given by (2), where I_{in} is the average input current.

$$I_{PMOSFET\_RMS} = \frac{I_{in}}{\sqrt{D}}\frac{\sqrt{2}}{2} \tag{2}$$

Equation (3) can be used to calculate the peak current through the primary MOSFETs.

$$I_{PMOSFET\_PK} = \frac{I_{in}}{D} \tag{3}$$

The best ripple current cancellation and dynamic performance is achieved at 50% duty cycle. Therefore, the transformer turns ratio should be selected so that the VRM operates at 50% duty cycle in the steady state. Using (1), when the input voltage is 12V and output 1V, if the duty cycle is 50%, the turns ratio is 2.5. If the turns ratio is 2, the duty cycle is 36.3%. If the turns ratio is 3, the duty cycle is 54.5%. Since when the turns ratio is 3 the duty cycle is closer to 50%, a turns ratio of N=3 is used for the prototype.

An interleaved buck Using (2) and (3), at 12V input and 1V/30A output, the RMS current through the four primary side MOSFETs are 2.39A, and the peak current is 4.58A. The proposed topology has four primary side switches and two synchronous rectifiers. When a two phase interleaved buck converter is used, it has two switches and two synchronous rectifiers. For the buck, with the same operating conditions including a 12V input and 1V/15A load per phase, its RMS current through the high side MOSFETs will be 4.33A and the peak current will be 15A for each of the two high side switches. Using the previous assumptions, at the high side the total switching losses for the two buck phases, neglecting the synchronous rectifiers, are 1.64 times that of primary side switches for the non-isolated full bridge [(15A*2 buck switches)/(4.58A*4 bull bridge switches)]. Furthermore, the high side conduction losses for the buck converter are also 1.64 times that of the primary side switches for the non-isolated full bridge [(4.33A^2*2 buck switches)/(2.39A^2*4 bull bridge switches)]. Therefore, the switching losses and conduction losses for the buck are both much higher than the proposed non-isolated full bridge.

Equations (4) and (5) can be used to calculate the RMS current through the synchronous rectifiers if the ripple of the inductor current is small.

$$I_{Lavg} = \frac{I_o - I_{in}}{2} \tag{4}$$

$$I_{syn\_RMS} = \sqrt{(1+D)}I_{Lavg} \tag{5}$$

From (4) it can be observed that the current stress on the synchronous rectifiers is reduced because the input current goes directly to the load side. Using (4) and (5), the average current through the synchronous rectifiers is 13.75A and the RMS current is 17.09A.

B. Principals of Operation

In this section, the detailed operation states of the non-isolated full bridge in phase mode are analyzed. Key waveforms are shown in Fig. 2.

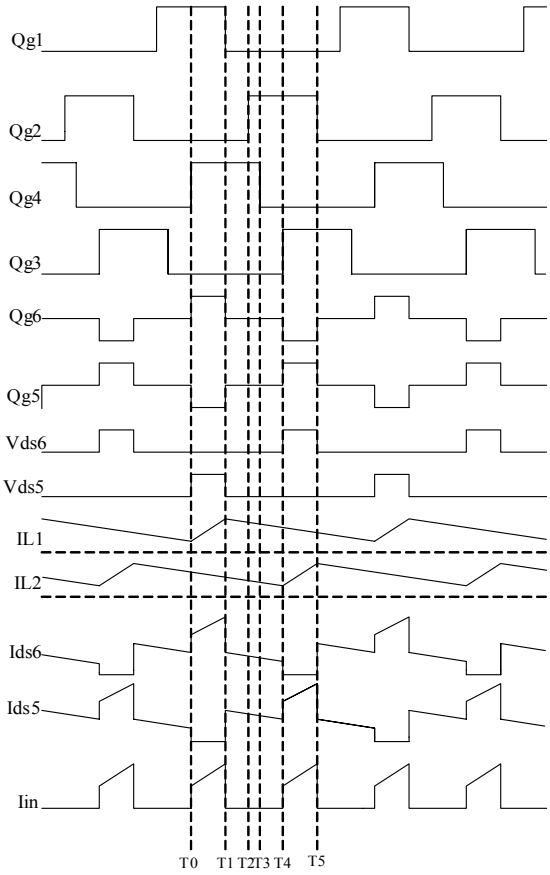

Fig. 2 Waveforms during the five states of operation

The first state is illustrated in Fig 3. From time T0 to T1, Q1, Q4 and Q6 are on. The current in L1 decreases and the current in L2 increases. Energy flows from the input to the

load.

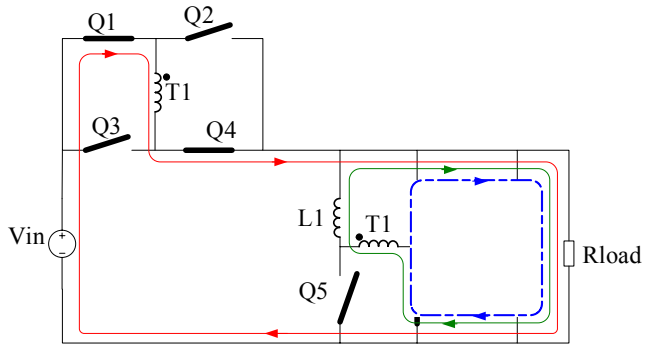

Fig. 3 Circuit operation during time interval T0-T1

The second state is illustrated in Fig 4. From time T1 to T2, Q1 turns off first to allow the zero voltage turn on of Q2. The current reflected from secondary side charges C1 and discharges C2. The current in L1 and L2 both decrease.

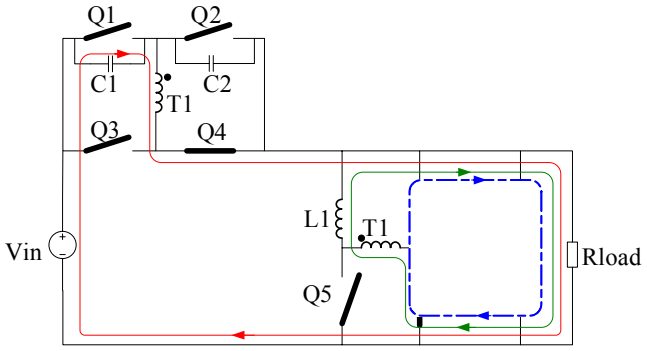

Fig. 4 Circuit operation during time interval T1-T2

The third state is illustrated in Fig 5. From time T2 to T3 after the voltage across Q2 reaches zero, Q2 turns on at zero volts. Both Q5 and Q6 are on. Since the secondary side of the transformer is shorted, the primary and secondary sides of the transformer are decoupled.

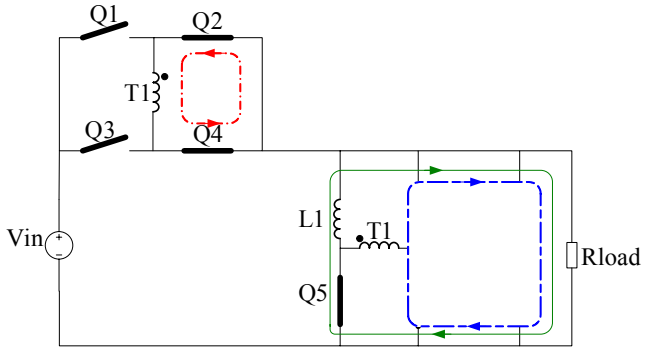

Fig. 5 Circuit operation during time interval T2-T3

The fourth state is illustrated in Fig 6. From time T3 to T4, Q4 turns off to prepare for the zero voltage turn on of Q3. The energy stored in the leakage inductance of the transformer charges C4 and discharges C3.

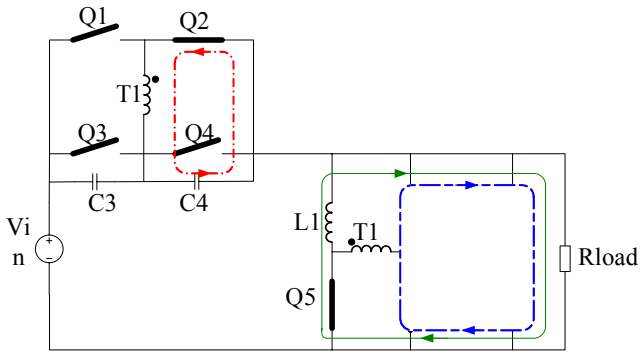

Fig. 6 Circuit operation during time interval T3-T4

The fifth and final state is illustrated in Fig 7. From time T4 to T5 after the voltage across Q3 is zero, Q3 turns on at zero volts and Q6 turns off. At this time one switching period is complete.

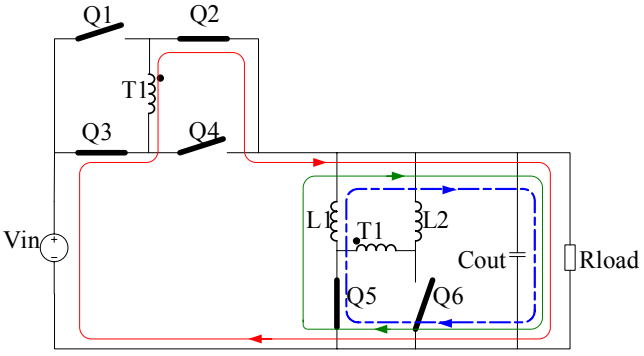

Fig. 7 Circuit operation during time interval T4-T5

C. *Design Comparison*

In order to verify the proposed topology, a 12V input 1V/30A output VRM has been designed to operate at a 500kHz switching frequency. The turns ratio of primary to secondary is 3:1. In the steady state the duty cycle is 0.545. Phase shift control is used to reduce the switching losses in the primary side. In order to demonstrate the advantages of this topology, the key parameters of the new topology and a buck topology operating at 12V input and 1V/30A output are compared in Table1. The inductor current ripple is included in the calculations.

From the data shown in Table 1 and the previous analysis, it is clear that the new full bridge topology has significant advantages over the traditional phase shift buck:

1. The peak primary current of the proposed topology is much less than buck. In addition, since zero voltage switching can be achieved with phase shift control, switching losses of primary side are significantly reduced.
2. The duty cycle of the proposed topology can be optimized for dynamic response and efficiency.
3. The primary side input current is sent to the load side so that the current stress of the synchronous rectifiers can be reduced.

4. Since the duty cycle of the proposed topology is near 50%, it can provide better ripple cancellation compared to a conventional buck.

TABLE 1 PARAMETERS COMPARISON OF BUCK AND NEW FULL BRIDGE OPERATE AT 12V INPUT

Topology	Duty Cycle	Peak Primary Current	Synchronos Rectifier RMS Current
New Non-Isolated Full Bridge	0.545	4.88A	17A
2 Phase Buck	0.083	18A	14.3A
	Output	**Filter Inductor**	**Filter Inductor Peak Current**
New Non-Isolated Full Bridge	1V/30A	300nH	14.9A
2 Phase Buck	1V/15A/Phase	300nH	18A

IV. EXPERIMENTAL RESULTS

A prototype has been built for a 12V input and 1V/30A load on a 1.41 by 1.41 inch 12 layer, 2oz copper printed circuit board. A photo of the prototype is shown in Fig. 8.

In the design three RM4 core pairs are used. One pair is used for transformer and the other two pairs are used for the current doubler.

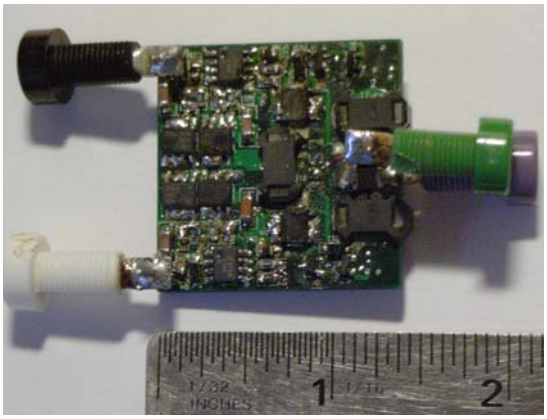

Fig. 8 Photo of the prototype; size 1.41"x1.41"(3.6x3.6cm)

In the proposed topology, the transformer design is very important - if the leakage inductance is too large, the performance of the VRM will be very poor. Large leakage inductance on the synchronous rectifier driving windings causes ringing for the drive voltage, which detrimentally affects the performance of the synchronous rectifiers. Large leakage inductance on the secondary windings causes poor current sharing of the two synchronous rectifiers and increases conduction losses. The layers of the transformer are shown in Fig. 9. The leakage inductance of the transformer windings was measured and the measurement results are shown in Fig. 10.

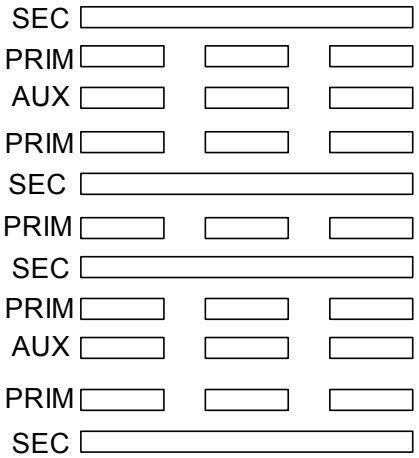

Fig. 9 Transformer layers

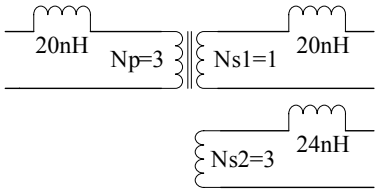

Fig. 10 Leakage inductance measurement results of the transformer.

The high side MOSFETs used in the design are IRF7821, since they have very low gate charge to minimize switching loss. The low side MOSFETs used are FDS7788, since they have very low on state resistance to minimize conduction loss. Experimental waveforms of the self-driven gate drive signals of the synchronous rectifiers and drain-to-source voltages are shown in Fig. 11 and Fig. 12, respectively. An efficiency of 84.8% has been achieved at full load.

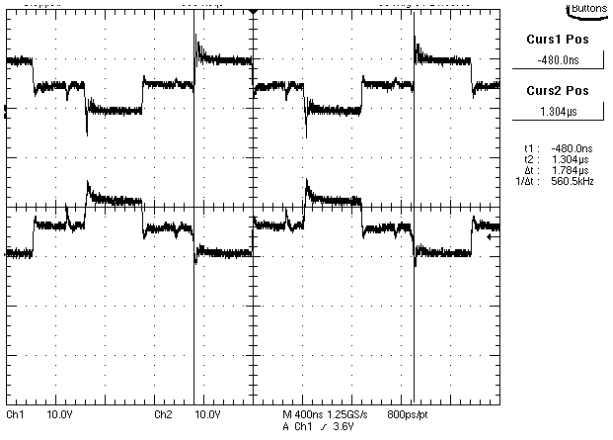

Fig. 11 Gate drive signals of the synchronous rectifiers

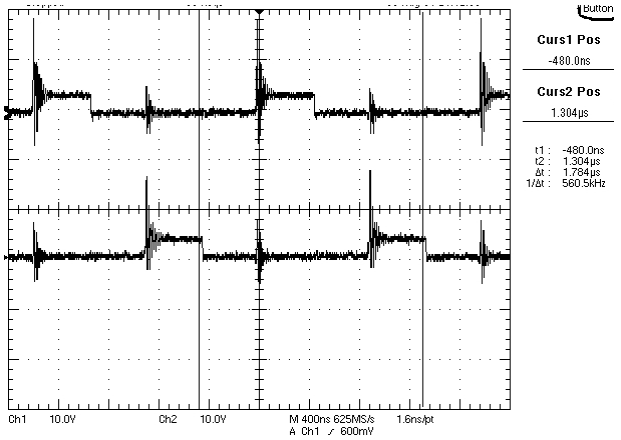

Fig. 12 Drain-to-source voltage waveforms of the SRs

V. CONCLUSIONS

In this paper, a new non-isolated full bridge topology has been proposed. The primary side of this topology is a full bridge, however the input voltage ground of the conventional full bridge is connected directly to the output. In this arrangement, the input current flows directly to the load without going through the transformer. The secondary side rectifier stage is a current doubler. The primary side can operate in either phase shift soft switching mode or hard switching mode, so zero voltage switching can be achieved, thereby dramatically reducing switching losses in comparison to traditional multi-phase buck VRM topologies. The secondary side of the proposed topology is the current doubler. A transformer is utilized in the proposed topology so that the duty cycle of the VRM can be optimized to maximize current ripple cancellation, efficiency and dynamic response.

To demonstrate the advantages of this topology a VRM module has been built and tested. From the analysis presented and experimental results it is clear that this new topology can achieve much better efficiency than conventional multi-phase buck VRM topologies.

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