A New Transformer-Based Non-isolated Topology Optimized for VRM Application

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***Abstract*---The duty cycle of conventional multi-phase buck converters becomes extremely small as the output voltage becomes lower and lower. This is a severe challenge with the switching frequency goes up. This paper introduces a non-isolated half bridge converter which can extend the duty cycle to a favorable range. Thus, the converter will have symmetrical dynamic response ability. The switching loss will reduce dramatically. The primary current is directly transferred to the output. The energy transferring is more effectively then that of conventional isolated half bridge converter. In addition, the voltage stress of the primary MOSFETs equals to the input voltage, which is much lower than that of non-isolated forward or push-pull topologies. A 12V input, 0.8V/30A output, 500 kHz prototype was built to demonstrate the advantages.**

I. INTRODUCTION

There is a clear trend that the output voltage of VRMs designed for the future microprocessors will be 1V even lower. In order to reduce the passive component size, and also to meet the stringent transient response requirement, the switching frequency will also move into the MHz range in the next few years.

Most of today's 12V VRMs use synchronous buck topology. As the output voltage goes down and the switching frequency goes up, the duty cycle becomes extremely narrow and the turn-on period of the top switch becomes extremely short. In order to generate this extremely short gate driving signal, a high speed comparator is necessary, this may increase cost. Moreover, the extreme duty cycle may cause malfunction at high frequency due to the very short conduction time for the top switch.

Another problem caused by this narrow duty cycle is the asymmetrical transient response. The step-down response is much worse than the step-up response. That's because when the load steps up, the duty cycle can extend much to provide energy to the output. On the other side, the duty cycle cannot be much smaller to respond effectively to a load step-down as there is no space to decrease the duty cycle further. This asymmetrical transient response makes the output filter over-designed and makes it very difficult to optimize the design [1].

The most serious problem for 12V input buck converter is the large top switch turn-off loss. For the same input average current, the narrower the duty cycle, the higher the peak current goes through the top switch. Furthermore, in order to satisfy the fast transient response requirement, the output inductor can't be too large. Small inductance yields large current ripple. Hence, the turn-off current of the top switch becomes very large, so the turn-off switching loss is increased and efficiency will suffer.

To solve the above mentioned problems, transformer based topologies, such as tapped-inductor buck converter, forward converter, push-pull converter are developed.

Tapped-inductor buck converter extends the converter duty cycle to a favorable range [1]-[4]. However, this topology also generates some other issues such as complicated magnetic implementation. The major drawback is the leakage inductance of the tapped inductor, which makes the topology almost infeasible without additional snubber.

Non-isolated forward topology is another solution [5]. But since the transformer works in the first quadrant, the size of the transformer will be much bigger than that of double-ended topologies. In addition, a reset winding is needed for forward converter. This makes the transformer design more complicated. Therefore, the overall size of the VRM will be bigger than multiphase buck solution. Furthermore, the voltage stress of the primary MOSFET is twice the input voltage.

Non-isolated push-pull topology is another choice. A smaller core can be used for the same out power comparing with the above forward topology [6][7]. The drawback is that there are two windings in primary, which makes the transformer design a little more critical when using planar PCB transformer. Furthermore, it's necessary and important to avoid transformer imbalance. The voltage stress of primary MOSFETs is also twice the input voltage.

A common drawback of those topologies is that the voltage stress of the primary switches is much higher than the input voltage, even twice. For 12V input VRM, its input voltage will be up to 14V, so the voltage stress of primary switches is 28V plus spike. Obviously, 30V MOSFET, which is widely used in 12V input VRM applications, can not be used reliably in this case. Thus, the efficiency and performance of the converter will suffer. Therefore, topologies with extended duty cycle and low voltage stress

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are expected.

This paper presents a novel non-isolated half bridge topology as an alternative solution for future 12V VRMs, as given in section 2. This proposed topology has many benefits as compared with the above mentioned topologies. Section III the steady state analysis which shows that it can extend the duty cycle and keep the voltage stress as low as that of buck converter. Section IV provides the loss comparison between the proposed topology and Buck converter. Section V summarizes the advantages of the new converter and section VI provides the experimental results for a 12V input, 0.8V/30A output, 500 kHz prototype. Section VII is the conclusion.

II. PROPOSED NON-ISOLATED HALF-BRIDGE TOPOLOGY

Fig.1 is a conventional half bridge topology. Current doubler is adopted at the secondary side, which can provide ripple cancellation. When isolation is not needed, the primary ground can be connected with secondary ground. By selecting proper transformer turns ratio, a duty cycle around 50% can be achieved for 12V input and 1V or 0.8V output.

It is observed that with the conventional half bridge converter, all the output electrical energy is converted into magnetic energy and back into electrical energy through the transformer. It is also observed that the primary ground shall be at a stable voltage potential so that the half bridge can operate properly.

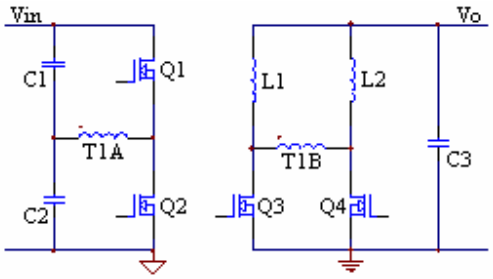


Fig. 1 Conventional half bridge topology

A new topology can be developed by connecting the primary ground of the conventional half bridge converter to the output voltage point instead of connecting it to the secondary ground, as shown in Fig.2.

Comparing with the conventional half bridge topology, the major advantage of this proposed circuit is that part of the output energy is transferred from the input to the load directly without going through the filter inductor. Therefore, the transformer secondary winding current, consequently the inductor current are reduced, and the converter operates more efficiently. Duty cycle can be extended and optimized by selecting appropriate turns ratio of the transformer. The turn-off time of Q2 can also be reduced significantly because the gate is reversely biased by the output voltage during off time.

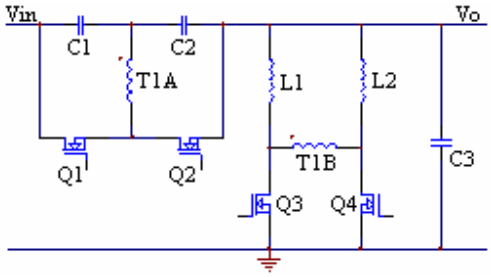


Fig. 2 Proposed Non-isolated Half Bridge topology

It can be expected that this non-isolated half bridge converter will have similar operation and waveforms as the conventional half bridge converter. Fig.3 gives the key waveforms of the proposed topology.

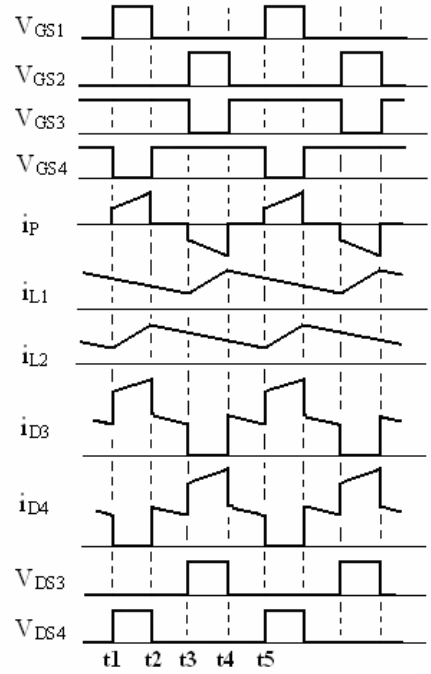


Fig. 3 Key waveforms of the proposed topology

The operation of this non-isolated half bridge converter can be briefly described by five operation modes as shown in Fig.4 as follows:

Mode 1 ($t < t1$): Initially, Q1 and Q2 are off. Q3 and Q4 are on. The inductors L1 and L2 are both freewheeling.

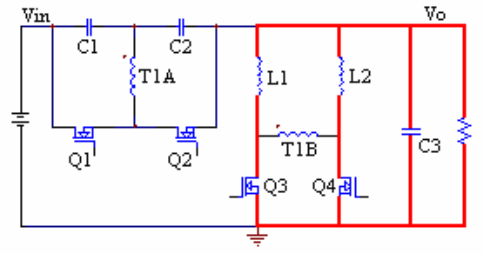
Mode 2 ($t1 < t < t2$): Q1 turns on and Q4 turns off at t1 simultaneously. The energy starts delivering from input to the load. The inductor L1 is still freewheeling through Q3, while the inductor L2 is charged through Q3 as well. In addition to the current of inductor L1 and L2, the input current also goes through C3 and load resistor. Part of required energy delivers to output directly.

Mode 3 ($t2 < t < t3$): Q1 turns off and Q4 turns on at t2 simultaneously. The inductors L1 and L2 are both freewheeling.

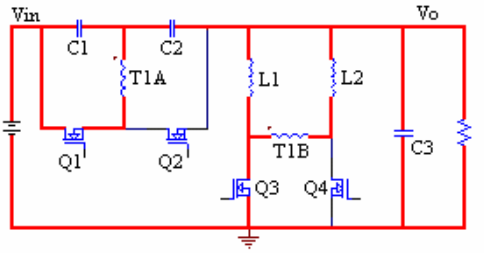
Mode 4 (t3 < t < t4): Q2 turns on and Q3 turns off at t3 simultaneously. The inductor L1 is charged while L2 is still freewheeling through Q4. In addition to the current of inductor L1 and L2, the input current also goes through C3 and load resistor. Part of required energy delivers to output directly.

Mode 5 (t4 < t < t5): Q2 turns off and Q3 turns on at t4 simultaneously. The inductors L1 and L2 are both freewheeling. At t5, Q1 turns on and Q4 turns off again. Next cycle starts.

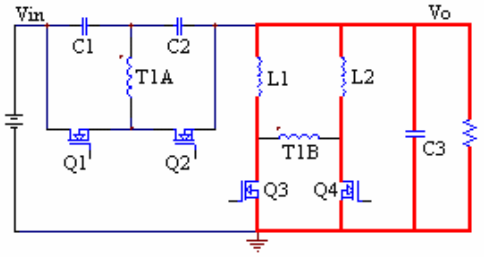
Essentially, Q1 and Q2 turn on alternatively as within the conventional half bridge converter. Q1 and Q4 turn on complementarily, and Q2 and Q3 turn on complementarily as well. The input current in the proposed converter is directly transferred to the output in addition to the secondary current. This is a more effective way to deliver energy than the conventional half bridge converter. Control of the non-isolated half bridge converter is the same as the control of a conventional half bridge converter.



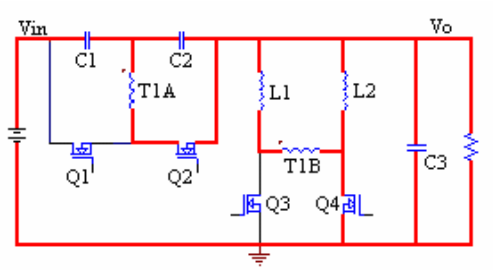
(a) Mode 1 (t < t1)



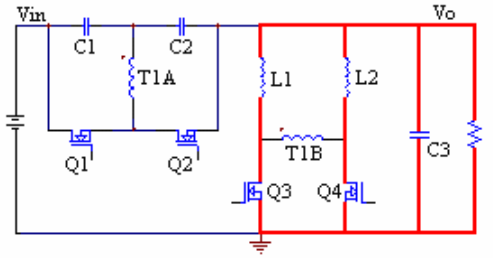
(b) Mode 2 (t1 < t < t2)



(c) Mode 3 (t2 < t < t3)



(d) Mode 4 (t3 < t < t4)



(e) Mode 5 (t4 < t < t5)

Fig. 4 Equivalent circuits in five operation modes

III. STEADY-STATE ANALYSIS OF NHB

The operating principle of this non-isolated converter is similar to a conventional half bridge converter, but there are still some differences.

For conventional half bridge converter, the steady-state conversion ratio is:

$$M = \frac{V_o}{V_{in}} = \frac{D}{2n} \qquad (1)$$

Where, D is the turn-on time of each MOSFET over one switching cycle divided by half of the period. n is the transformer turns ratio Np / Ns.

For the proposed converter, the primary voltage amplitude of the transformer is:

$$V_p = \frac{V_{in} - V_o}{2} \qquad (2)$$

The volt-second of the output inductor L1 or L2 must keep balance in steady-state. Considering the voltage across L1 over a whole switching cycle:

At t1 ~ t2, $t = D * T_s / 2$, $V_L = - V_o$

At t2 ~ t3, $t = (1 - D) * T_s / 2$, $V_L = - V_o$

At t3 ~ t4, $t = D * T_s / 2$, $V_L = V_p / n - V_o$

At t4 ~ t5, $t = (1 - D) * T_s / 2$, $V_L = - V_o$

Where, T_s is the switching period. V_L is the voltage across inductor L1.

The volt-second over a switching cycle should be zero,

therefore:

$$-V_o\cdot\frac{D}{2}\cdot T_s - V_o\cdot\frac{1-D}{2}\cdot T_s + \left(\frac{V_p}{n} - V_o\right)\cdot\frac{D}{2}\cdot T_s - V_o\cdot\frac{1-D}{2}\cdot T_s = 0$$

Thus the conversion ratio of the proposed converter can be solved as:

$$M = \frac{V_o}{V_{in}} = \frac{D}{4\cdot n + D} \quad (3)$$

Meanwhile, the duty cycle can be derived as:

$$D = \frac{4\cdot V_o\cdot n}{V_{in} - V_o} \quad (4)$$

Where, D is the converter duty cycle, which equals to turn-on time of each MOSFET over a switching cycle divided by half of the switching period. V_{in} is the input voltage. V_o is the output voltage. n is the transformer turns ratio (Np / Ns).

If the input voltage V_{in} is 12V and output voltage V_o is 0.8V, the duty cycle is 0.067 when buck topology is adopted. Instead, the duty cycle will be 0.57 (assume n=2) when the proposed topology is adopted. The duty cycle is extended to a favorable value.

With the duty cycle extended to an appropriate range from extremely narrow level, the converter will have symmetrical dynamic response ability. High performance comparator will be not necessary for the pulse width modulator. The possibility of malfunction can be significantly reduced.

The voltage stress of primary MOSFETs Q1 and Q2 is:

$$V_{stress} = V_{in} - V_o \quad (5)$$

The voltage stress equals to around 14V for 12V input (10-14V).

The voltage stress of secondary synchronous MOSFETs equals to the voltage amplitude across the secondary winding of the transformer, which is V_p / n. V_p is decided by equation (2). So the voltage stress is around 3V when n equals to 2 in 12V input condition.

These are smaller than those in buck converter. While on the contrary, the voltage stress of the primary MOSFETs is two times of the input voltage in forward and push-pull topologies. That means the proposed topology can get higher reliability or lower conduction loss by using lower voltage rate MOSFETs, such as 20V MOSFETs. Another benefit of low voltage stress is that the miller effect of MOSFETs reduces, so the gate driving loss even switching loss can be reduced.

The waveforms of the current flowing through bottom MOSFETs Q3 and Q4 are of trapezoid, which is illustrated in Fig.3 as i_{D3} and i_{D4}. The RMS value of this waveform is:

$$I_{Q\_rms} = \frac{I_o}{2}\cdot\sqrt{1 + D} \quad (6)$$

Where, I_o is the output current. Obviously, the RMS value of the current flowing through bottom MOSFET increases when the duty cycle is extended.

The current waveform of the primary MOSFETs in NHB is similar to that of conventional half bridge converter.

IV. LOSS COMPARISON

Detailed loss analysis for a 12V input, 0.8V/30A output converter was done. A two phase synchronous buck converter was also designed for same requirement and used as a benchmark for this analysis.

Roughly, the total power loss of a buck converter and the proposed non-isolated half bridge converter can be divided into four major parts:

1. Switching loss of the MOSFETs
2. Conduction loss of the MOSFETs
3. Gate driving loss of the MOSFETs
4. Loss of Magnetic components

Turn-off loss is the dominant loss for the primary/top MOSFETs. In the proposed non-isolated half bridge converter, the duty cycle is extended, so the peak current flows through the primary MOSFETs decreases dramatically for the same output power. Thus the turn-off loss of the primary MOSFETs, which is proportional to the peak current, will be significantly reduced as compared with that of the top MOSFETs in a two-phase buck converter. For a 12V input, 0.8V/30A output two-phase buck converter, assuming current ripple is 20A, the peak current flowing through each top MOSFET will be 25A when it turns off. On the contrary, if the non-isolated half bridge converter (NHB) is adopted, the primary current ripple is only 6.2A by using the same inductor as buck converter, so the peak current flowing through each primary MOSFET will be 10.1A when it turns off. Fig. 5 illustrates the difference.

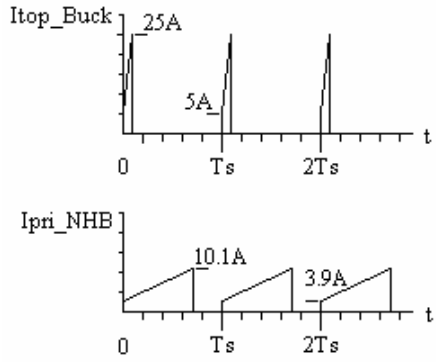


Fig. 5 Peak current difference in buck converter and proposed converter

Assuming turn-off time is 15ns, switching frequency is

500 kHz. The turn-off switching loss of two top MOSFETs in buck converter will be:

$$P_{off} = 2 * 1/2 * V_{in} * I_p * t_{off} * f_s = 12*25*15n*500k$$

$$= 2.25W$$

The turn-off switching loss of two primary MOSFETs in non-isolated half bridge converter is:

$$P_{off} = 2 * 1/2 * V_{in}/2 * I_p * t_{off} * f_s = 6*10.1*15n*500k$$

$$= 0.45W$$

Obviously, turn-off switching loss of non-isolated half bridge converter is much less than that of two-phase buck converter, 1.8W loss is saved.

Actually, the proposed converter can also save some turn-on switching loss, but the turn-on switching loss is usually less than 20% of the turn-off switching loss, and it is hard to precisely evaluate as the effect of reverse recovery of the body diode in the synchronous MOSFET.

On the other side, conduction loss is the dominant loss for the secondary side MOSFETs and bottom MOSFETs. In a two-phase synchronous buck converter, the RMS value of the current in each bottom MOSFET roughly equals to:

$$I_{Q\_rms} = \frac{I_o}{2}\cdot\sqrt{1-D} \qquad (7)$$

In the proposed non-isolated half bridge converter, the secondary side MOSFET's current waveforms were shown in Fig.3. The RMS value of the current flowing in each secondary MOSFET was roughly expressed in equation (6). Duty cycle is extended in the proposed topology. Obviously, RMS value of the current flowing through the secondary side MOSFETs increased. Hence, the conduction loss in non-isolated half bridge converter increases as compared with that in the two-phase synchronous buck converter.

Since there is an extra transformer in the proposed converter and the transformer will dissipate some energy, the magnetic losses of the proposed converter, which included inductor losses and transformer losses, will increase too.

An example was taken for this loss analysis. The input voltage is 12V, output voltage and current is 0.8V/30A. Switching frequency is 500 kHz. IRF7821 was selected as primary and top MOSFETs, and FDS7088N7 was selected as secondary side and bottom MOSFETs, the secondary inductor is 250nH.

Fig.6 illustrates the breakdown of the losses in the proposed non-isolated half bridge converter (NHB) and a two-phase synchronous buck converter (Buck).

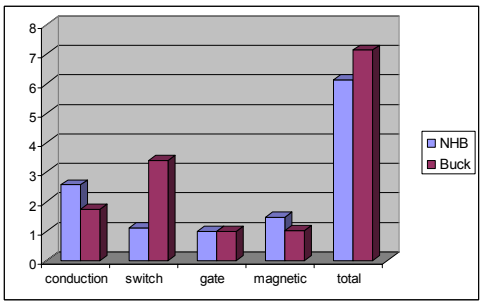


Fig. 6 Loss comparison between proposed converter and two-phase buck converter

It is noticed that the overall efficiency of the proposed converter is still improved since the switching loss is reduced so dramatically. The calculation results indicate that the efficiency is improved about 2% ~ 3%.

This non-isolated half bridge converter can also be further extended to multi-phase configuration (as show in Fig.7). With respect to multi-phase buck converter, there is an advantage for the proposed topology in this kind of configuration. In multi-phase buck converter, in order to realize current sharing, either input current or output current of each phase need to be sensed. It's difficult to sense the current with good noise immunity and low power dissipation. In NHB, the current sensing is much easier than buck converter. In stead of sensing four current in a 4 phase buck converter, only two currents need to be sensed in this proposed topology. As shown in Fig.7, R1 and R2 are used to sense the input current of each phase. It is observed that one terminal of R1 and R2 is at a fixed low voltage. This makes the signal processing much easier.

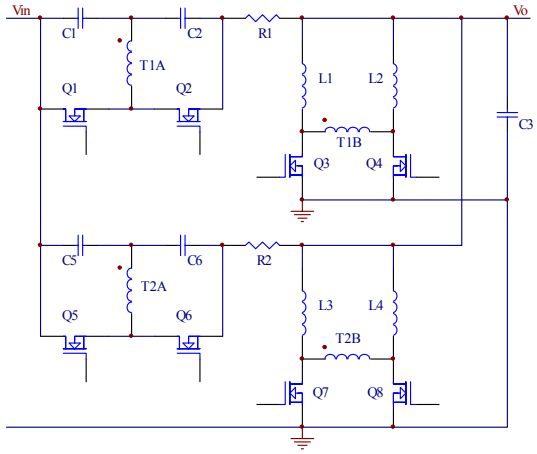


Fig. 7 Multi-phase non-isolated half bridge converter

V. ADVANTAGES

The major advantages of this proposed topology are the duty cycle is extended and the overall efficiency is improved comparing with a buck converter. The dynamic performance of the converter will also benefit from the extended duty cycle.

The transformer size is much smaller than that in forward topology. There is only one primary winding, so the transformer design is simple. The voltage stress of the primary MOSFETs equals to the input voltage, which is much lower than those in forward or push pull converter.

The benefits of proposed NHB topology can be summarized as:

1. Duty cycle can be extended to a favorable value.
2. Improved Efficiency with respect to synchronous buck converter and conventional half bridge converter.
3. Voltage stress of the primary MOSFETs is less than the input voltage.
4. Symmetrical transient response ability.
5. Easier implementation for multi-phase configuration and better ripple cancellation performance.

VI. EXPERIMENTAL VERIFICATION

A 12V input, 0.8V/30A output prototype was built. For comparison, a two-phase interleaving buck converter was also built with same specification. The switching frequency is 500 kHz.

MOSFET IRF7821 was selected as the primary switches and top switches; MOSFET FDS7088N7 was selected as the secondary side switches and bottom switches. The main schematic is shown in Fig.2. Where C1 and C2 are two 10 uF ceramic capacitors, and C3 is a 100 uF ceramic capacitor. A PWM controller UCC3806 from TI was selected to generate the PWM signal and regulate the output voltage. 12 layer 2ounce PCB was designed and built.

RM4 planar cores and PCB windings are employed to build a transformer and two 250 nH inductors. The transformer has 2 turns in primary winding and 1 turn in secondary winding,

Coupling of the winding strongly affects the operation of the synchronous MOSFETs. Interleaved structure was used to ensure that the driving winding and the primary winding are well coupled. The transformer structure is illustrated in Fig.8 as below.

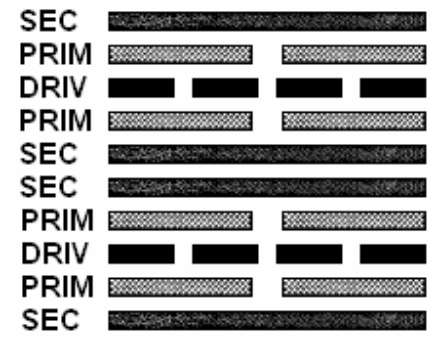


Fig. 8 Structure of the transformer

Self-driven was adopted for two synchronous MOSFETs Q3 and Q4. A driving winding was designed in the planar transformer to generate the driving signals for Q3 and Q4. A new simple drive scheme, which was presented in [8], was used to maintain the synchronous MOSFETs on even when the voltage in the transformer is zero. The driving winding has 4 turns.

Dual channel driver LM5100 from National Semiconductor was used as the driver chip for two primary MOSFETs Q1 and Q2.

Fig.9 shows the picture of the prototype. Fig.10 shows the measured waveforms.

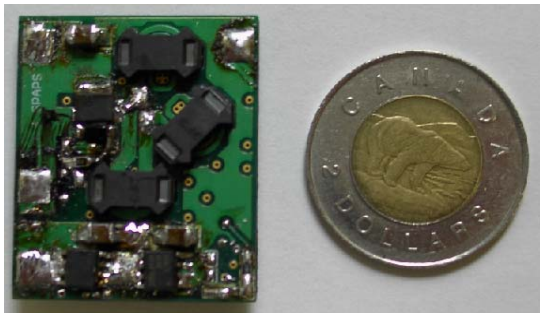
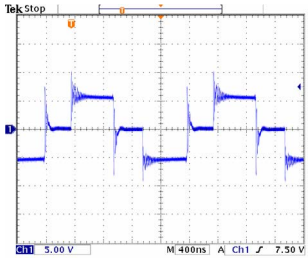


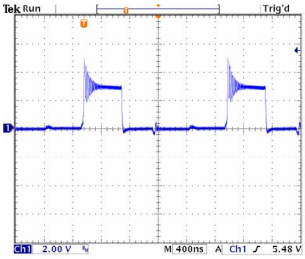
Fig. 9 Prototype of Non-isolated half bridge converter

Fig.10(a), (b) indicate that the operation waveforms are quite similar with conventional half bridge converter. Fig.10(c) indicates that the gate-source of the primary low side MOSFET is negative biased when it is turned off. This negative voltage can turn off the MOSFET faster, so its turn-off switching loss can be reduced. Fig.10(d) indicates the drive signal of the synchronous MOSFET. The drive voltage is around 6V even while the transformer voltage is zero.

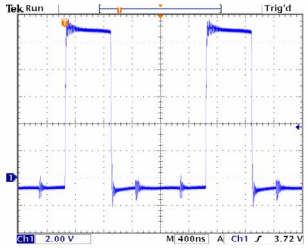
As the input voltage is connected to output terminal by two capacitors C1 and C2, in theory, the input voltage step will be coupled to output side. However, in reality, the impact is very small because the output capacitor, C3, is much larger than the voltage divider capacitors (C1, C2). Fig. 11 shows the response of the output voltage when at start up. Fig.11(a) shows the output voltage trajectory at start up, when the output capacitor C3 is 100uF. Fig.11(b) shows the output voltage trajectory at start up, when the output capacitor C3 is 500uF. It is noted that initially the output voltage has a very small jump and then the output voltage rises to its steady state value. In addition, the jump when C3 is 500uF is much smaller than that when C3 is 100uF. This step is caused by voltage divider formed by C1, C2 and C3. The bigger the capacitor C3 is, the lower the output voltage jump at start up is. It is noted that in actual condition, the output capacitor is much larger than 500uF and therefore, the voltage jump is even less. It is also noted that no soft start is designed in the prototype (UCC3806 does not have soft start function). If the soft start is used, the start up trajectory will be more desirable.



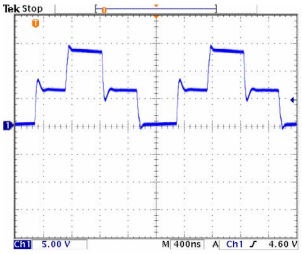
(a) Voltage across primary winding of the transformer (5 V/div, 400 ns/div)



(b) Drain-Source voltage of synchronous MOSFET (2 V/div, 400 ns/div)

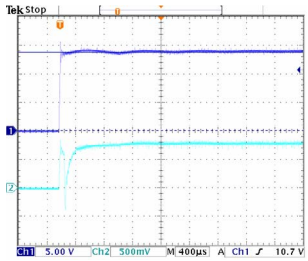


(c) Gate-source voltage MOSFET Q2 (2 V/div, 400 ns/div)

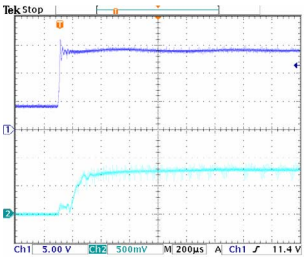


(d) Drive signal of the synchronous MOSFET (5 V/div, 400 ns/div)

Fig. 10 Typical waveforms of the prototype



(a) Output voltage at start-up, 100uF capacitor (5 V/div, 400 us/div)



(b) Output voltage at start up, 500uF capacitor (5 V/div, 200 us/div)

Fig.11 Start up trajectory

Fig.12 shows the measured efficiency at 0.8V, as well as the Buck converter. It is noticed that the proposed converter has more than 2% higher efficiency than the synchronous buck converter. The peak efficiency of the proposed converter at 0.8V is 83.8% at 15A. The full load efficiency at 30A is 79%.

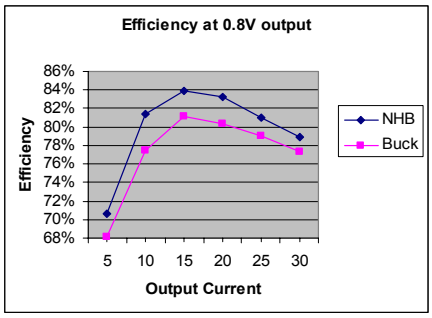


Fig. 12 Measured prototypes' efficiency

VI. CONCLUSIONS

Synchronous buck converter is a widely adopted solution for today's VRM application. When the switching frequency goes up and the output voltage goes down, this topology faces severe challenges as its duty cycle becomes extremely small. A novel non-isolated half bridge topology was proposed in this paper. It can extend the converter duty cycle, so the dynamic performance can benefit from it. The overall efficiency of the converter also improved. The voltage stress of the primary switches is lower than the input voltage, so that 20V low voltage rate MOSFETs can be used and the converter performance may benefit from this. A 12V input, 0.8V/30A output, 500 kHz converter was built to demonstrate its advantages.

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