A Digital Control Algorithm for DC-DC Converters Under Input Voltage Changes

Guang Feng (*Member IEEE*) [1], Wilson Eberle (*Student Member IEEE*), Yan-Fei Liu (*Senior Member IEEE*)
Queen's Power Group, www.queenspowergroup.com
Department of Electrical and Computer Engineering, Queen's University, Kingston, Ontario, Canada, K7L 3N6
gfeng@aps.anl.gov, wilsoneberle@wilsoneberle.com, yanfei.liu@queensu.ca

***Abstract* - In this paper, a new optimal two-switching cycle compensation algorithm is proposed to achieve optimal transient performance for DC-DC converters under an input voltage change. Using the principle of capacitor charge balance, the proposed algorithm predicts the optimized two-switching cycle duty cycle series to drive the output voltage back to the steady state when the input voltage changes. Experiments are performed in a 2.5V, 10A, synchronous Buck converter to verify the effectiveness of the proposed algorithm. The results show that using the proposed algorithm, good dynamic performance, including as small overshoot/undershoot and short recovery time is achieved.**

I. INTRODUCTION

Recently, there has been an increased demand for power converters with high dynamic performance [1],[2]. Among the many criteria of dynamic performance, output voltage overshoot and recovery time are often considered the most important. By improving the dynamic response of a DC-DC converter, the size of the output capacitor can be decreased to meet the same dynamic performance requirements. Thus, the cost of the converter is significantly reduced. Therefore, it is not only necessary but also practical to explore dynamic performance improvements for power converters.

In DC-DC converter control system design, good dynamic performance should be maintained during load current changes and input voltage changes. Reference [3] proposes an optimal control algorithm to achieve the best possible dynamic performance for DC-DC converters under a load current change.

In this paper, a new two-switching cycle compensation algorithm is proposed to optimize the transient performance for DC-DC converters under input voltage changes. Using the principle of capacitor charge balance, the proposed algorithm predicts the optimized two-switching cycle duty cycle series to drive the converter back to steady state when the input voltage changes. The proposed algorithm is well suited to be implemented digitally either using a field programmable gate array (FPGA) or a low-cost application specific integrated circuit (ASIC).

1. Dr. Guang Feng now is working as an assistant power electronics engineer at Argonne National Lab, Illinois, USA.

II. OPERATION PRINCIPLE OF THE PROPOSED TWO-SWITCHING CYCLE COMPENSATION ALGORITHM

The principle of capacitor charge balance states that, in the steady state, the average of the capacitor current over one switching period must be equal to zero. Equation (1) represents the principle of capacitor charge balance.

$$v_c(T_s) - v_c(0) = \tfrac{1}{C} \cdot i_{c\,avg} = 0 \rightarrow \frac{1}{T_s}\int_0^{T_s} i_c(t)dt = 0 \quad (1)$$

By recognizing that the integral period of (1) may be extended over the total transient time of a DC-DC converter, (2) is obtained.

$$v_c(t_b) - v_c(t_a) = \tfrac{1}{C} \cdot i_{c\,avg} = 0 \rightarrow \frac{1}{t_b - t_a}\int_0^{t_b - t_a} i_c(t)dt = 0 \quad (2)$$

In (2), t_a represents the time of the beginning of the transient period and t_b represents the end of the transient period. Thus, if at t_b the inductor current i_L and the duty d have reached their new steady state values and (2) has been satisfied, the converter will immediately enter its new steady state without any switchover between the new steady state and the transient.

Using the principle of capacitor charge balance, a new optimal two-switching cycle compensation algorithm for the input voltage changes is proposed. In this paper, the Buck converter, shown as Fig. 1, is used as the design example. The proposed optimal algorithm can also be applied to other converter topologies, including the Boost and Buck-Boost.

The transient response of the Buck converter under the control of the optimal algorithm is proposed as shown in Fig. 2. It is assumed that before point 0, the input voltage remains constant at v_{in0}. During switching cycle T_0, the input voltage increases from v_{in0} to v_{in1}. Since before point 1, the input voltage change has not been sensed by the control system, the duty cycle remains unchanged. As a result, the inductor current increases, which causes the output voltage to increase.

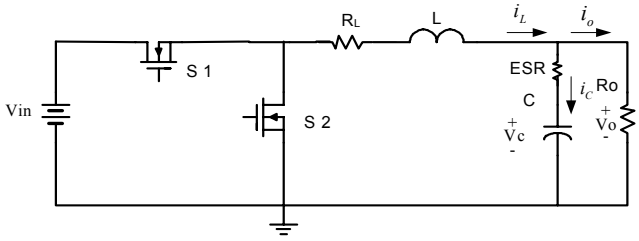


Fig. 1 Synchronous Buck converter

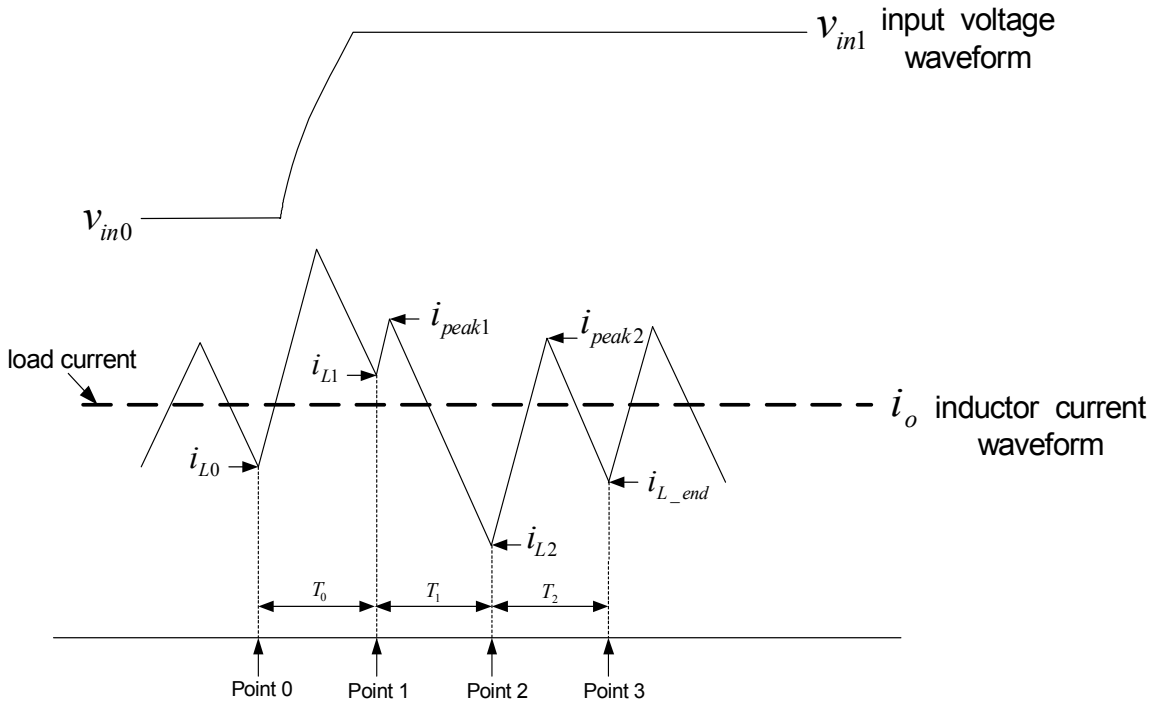


Fig. 2 The proposed two-switching cycle transient response for the positive input voltage change

In the proposed method, the input voltage is sampled each switching cycle. If at point 1, the sensed input voltage deviation exceeds a predefined level, the optimal two-switching cycle compensation algorithm is activated.

After the proposed algorithm is activated, the duty cycles for two-switching cycles are predicted for the cycles following point 1. The duty cycle values for switching cycle T_1 and T_2 are d_1 and d_2, respectively. Under the proposed algorithm, when the transient ends at the end of the second switching cycle at point 3, the following three conditions are satisfied,

1 The charge delivered to the capacitor is equal to the charge delivered by the capacitor at the end of the second switching cycle T_2.
2 At the end of the second switching cycle, the inductor current is equal to its new steady state peak minimum value, i_{L_end}.
3 At the end of the second switching cycle, the duty cycle is set to the new steady state value D_{new} for the new input voltage condition.

As a result, the converter immediately enters the new steady state without any switchover between the transient and the steady state. i.e. the output voltage, inductor current and duty cycle are at their steady state values. In addition, at the end of the transient, the control system is switched back to the current mode PID controller, which is used to control the steady state and small signal conditions. Before the control algorithm is switched back to the current mode PID controller, the optimal algorithm calculates the new steady state values i_{L_new} and D_{new}, and resets the outputs of the current mode PID controller to these calculated values. In the proposed compensation algorithm, at least two switching cycles are needed to compensate for the input voltage change. The explanation is given as follows.

It is assumed that at point 1, the output voltage error is Δv_o and the error between the inductor current and the new steady state inductor current value for the new input voltage condition is Δi_L. The relationship between the duty cycle d and the variation of output voltage, inductor current in one switching cycle can be expressed as (3).

$$\begin{cases} \Delta v_o = f_1(d) \\ \Delta i_L = f_2(d) \end{cases} \tag{3}$$

In (3), $f_1(d)$ and $f_2(d)$ are the functions for the DC-DC converter.

In order to drive the output voltage and the inductor current to their new steady state values in one switching cycle, (4) must be satisfied.

$$\begin{cases} \Delta v_o = f_1(d_1) \\ \Delta i_L = f_2(d_1) \end{cases} \tag{4}$$

However, (4) usually has no solution mathematically, since the number of unknowns is fewer than the number of equations. Therefore, at least two switching cycles are needed, so that the solution is obtained using (5).

$$\begin{cases} \Delta v_o = f_1(d_1) + f_1(d_2) \\ \Delta i_L = f_2(d_1) + f_2(d_2) \end{cases} \tag{5}$$

III. Equations Used to Calculate The Two-Switching Cycle Duty Cycle Series

The analysis in Section II shows that the key point to achieve the two-switching cycle transient response under an input voltage change is to precisely predict the duty cycle series d_1, d_2 and the new steady state duty cycle value D_{new} for the new input voltage condition. Using these predicted duty cycle values, the Buck converter enters the new steady state in two switching cycles without any switchover between the transient and steady state. As a result, small overshoot/undershoot and short recovery time can be achieved.

It is assumed that (a) the Buck converter system operates at the fixed frequency; (b) inductor value L, capacitor value C and switching frequency f_s are known; (c) the inductor current i_L, input voltage v_{in} and output voltage v_o can be directly measured. The following assumptions are also made in order to simplify the calculations:

1. Using the proposed compensation algorithm, the output voltage variation during the transient is very small, so that in the algorithm calculation, the output voltage is approximately equal to its nominal value, V_{ref}.
2. The load current i_o is constant during the transient. Therefore, its value can be obtained from the average inductor current value before the transient.
3. The input voltage v_{in1} remains unchanged during switching cycles T_1 and T_2.

If the input voltage variation is slow so that assumption (3) is not satisfied, or if the calculated duty cycle value d_1 or d_2 is higher than 100% or lower than 0%, an improved compensation algorithm proposed in Section IV is utilized.

The derivation of duty cycle values d_1 and d_2 is as follows. In order to achieve the condition (2) described in Section II, the duty cycle values d_1 and d_2 must be satisfy (6).

$$i_{L\_end} - i_{L1} = (d_1 v_{in1} - v_o')\frac{T_s}{L} + (d_2 v_{in1} - v_o')\frac{T_s}{L} \quad (6)$$

In (6), i_{L1} is the inductor current measured at point 1. The equivalent output voltage v_o' and the new steady state inductor current valley value, i_{L_end}, are given by (7) and (8).

$$v_o' \approx V_{ref} + i_o \cdot r_{loss} \quad (7)$$

$$i_{L\_end} = i_o - \frac{1}{2}\frac{v_o'}{L} \cdot T_S \frac{v_{in1} - v_o'}{v_{in1}} \quad (8)$$

In (7) and (8) i_o is the load current and r_{loss} is given by (9).

$$r_{loss} = R_L + R_{on} + R_{switching} \quad (9)$$

In (9), R_L is the winding resistance of the inductor, R_{on} is the MOSFET on resistance, and $R_{switching}$ is the MOSFET switching loss equivalent resistance.

The relationship between d_1 and d_2 can be derived from (6) and is given by (10).

$$d_1 + d_2 = \frac{(i_{L\_end} - i_{L1}) \cdot \frac{L}{T_s} + 2 \cdot v_o'}{v_{in1}} = k \quad (10)$$

Under the proposed algorithm, the charge delivered to the capacitor is equal to the charge delivered by the capacitor by the end of the transient (point 3). Therefore, (11) is obtained.

$$A_{charge0} + A_{charge1} + A_{charge2} = 0 \quad (11)$$

In (11), $A_{charge0}$ is the change of capacitor charge at point 1, $A_{charge1}$ and $A_{charge2}$ are the capacitor charge variation during the switching cycles T_1 and T_2.

Assuming that the capacitor voltage ripple is very small, then $A_{charge0}$ can be calculated from (12) using the output voltage v_{o1} measured at point 1 of Fig. 2 and (13), (14).

$$\begin{aligned} A_{charge0} &= C \cdot (v_{C1} - v_{C0}) \approx C \cdot (v_{C1} - V_{ref}) = C \cdot (v_{o1} - i_{C1} \cdot ESR - V_{ref}) \\ &= C \cdot (v_{o1} - (i_{L1} - i_o) \cdot ESR - V_{ref}) \end{aligned} \quad (12)$$

where

$$C\frac{dv_C}{dt} = i_c = i_L - i_o \quad (13)$$

$$v_o = v_C + i_C \cdot ESR \quad (14)$$

In (14), *ESR* is the equivalent series resistance of output capacitor.

The capacitor charge variation $A_{charge1}$ during the switching cycle T_1 can be expressed by (15).

$$\begin{aligned} A_{charge1} &= \frac{1}{2} d_1 T_s \cdot \left[(i_{L1} - i_{L2}) + (i_{peak1} - i_{L2})\right] \\ &\quad + \frac{1}{2}(1 - d_1) T_s \cdot (i_{peak1} - i_{L2}) - (i_o - i_{L2}) T_S \end{aligned} \quad (15)$$

In (15), i_{L2} is the inductor current value at point 2 and i_{peak1} is the peak inductor current value during the switching cycle T_1. i_{peak1} and i_{L2} can be derived as (16) and (17).

$$i_{peak1} = i_{L1} + d_1 T_s \frac{(v_{in1} - v_o')}{L} \quad (16)$$

$$i_{L2} = i_{L1} + (d_1 v_{in1} - v_o')\frac{T_s}{L} \quad (17)$$

The capacitor charge variation $A_{charge2}$ during the switching cycle T_2 can be expressed as (18)

$$\begin{aligned} A_{charge2} &= \frac{1}{2} d_2 T_s \cdot (i_{peak2} - i_{L2}) \\ &\quad + \frac{1}{2}(1 - d_2) T_s \cdot \left[(i_{peak2} - i_{L2}) + (i_{L\_end} - i_{L2})\right] - (i_o - i_{L2}) T_S \end{aligned} \quad (18)$$

In (18), i_{peak2} is the peak inductor current value during switching cycle T_2. It can be obtained using (19).

$$i_{peak2} = i_{L2} + d_2 \cdot T_s \cdot \frac{(v_{in1} - v_o')}{L} \quad (19)$$

Substituting (6), (7), (11)-(19) into (10), the duty cycle values d_1 and d_2 are given by (20) and (21).

$$d_1 = \frac{1}{2}\left[(1+k) - \sqrt{(1+k)^2 + \frac{4L}{v_{in1} \cdot T_s}(i_{L1} - 2i_o + i_{L\_end} - \frac{1}{2}k^2 v_{in1}\frac{T_s}{L} + \frac{A_{charge0}}{T_s})}\right] \quad (20)$$

$$d_2 = k - d_1 \quad (21)$$

When the two-switching cycle transient response ends, the control algorithm is switched back to the current mode PID controller, which is used to control the steady state and small signal variations. In order to make the Buck converter enter the new steady state smoothly, the compensation algorithm calculates the new steady state values i_{Lnew} and D_{new} for the current mode PID controller, and resets the outputs of the current mode PID controller to these calculated values. The new steady state duty cycle value D_{new} for the new input voltage v_{in1} is given by (22).

$$D_{new} = v_o' / v_{in1} \quad (22)$$

Since the new steady state inductor current peak minimum value is i_{L_end}, and the inductor current is sampled 0.3 T_s before the switch is turned on when the Buck converter system is operating in the steady state, the new steady state inductor current reference value i_{Lnew} is obtained using (23).

$$i_{Lnew} = i_{L\_end} + 0.3 \cdot v_o' \cdot T_s / L \quad (23)$$

IV. Improved Optimal Compensation Algorithm

In Fig. 2, the input voltage step change is assumed to be finished before point 1. However, in a real implementation, the input voltage variation is slower due to the input filter capacitor. It may take several switching cycles for the input voltage to reach its new steady state value. To resolve this problem, an improved optimal two-switching cycle compensation algorithm is proposed as shown in Fig. 3.

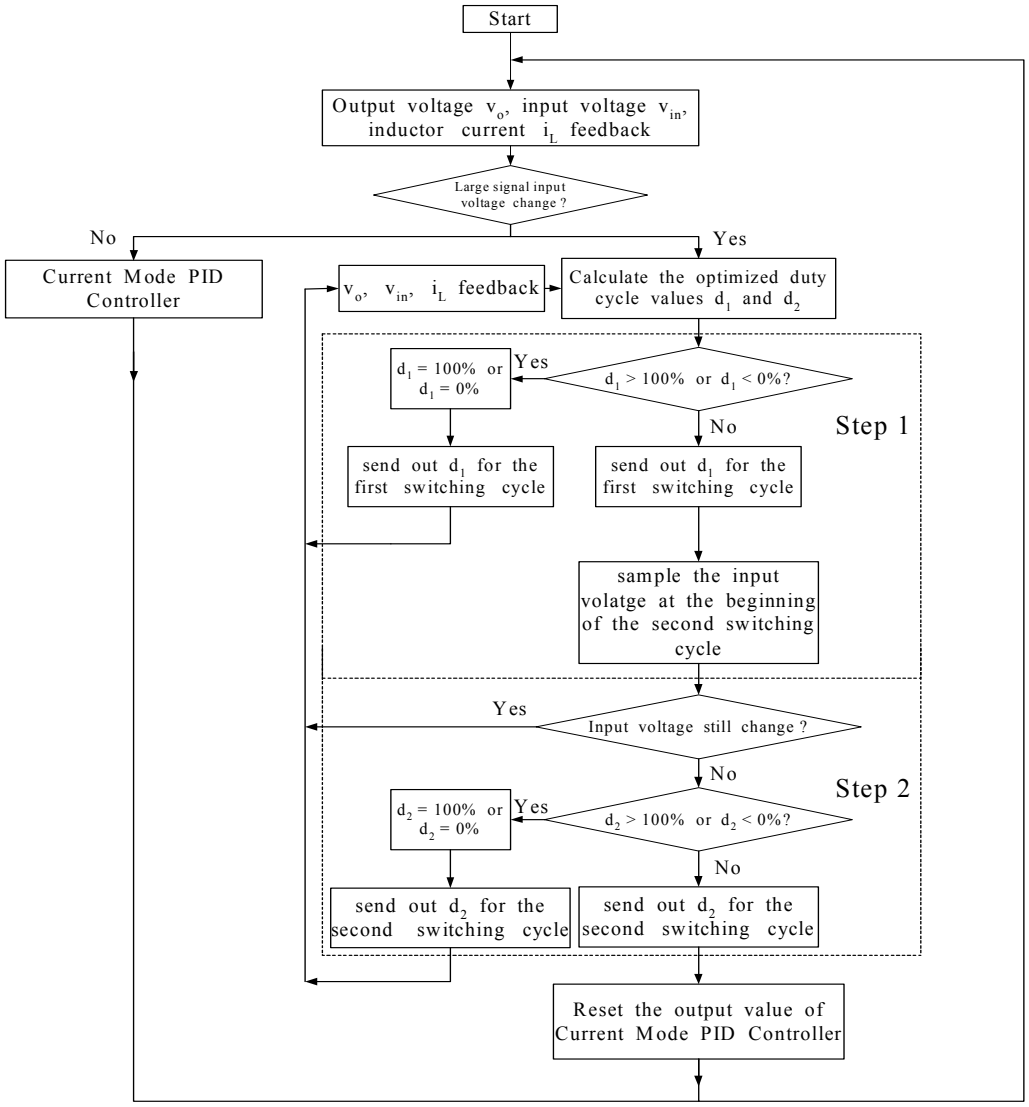


Fig. 3 Flowchart of the improved two-switching cycle compensation algorithm for the input voltage change

In the improved algorithm, the input voltage is sensed each switching cycle. If the large signal input voltage change is sensed, the compensation algorithm is activated. A two-switching cycle duty cycle series is predicted for the given transient response. If the input voltage sampled at the beginning of second switching cycle (point 2) is different from that sampled at the beginning of the first switching cycle (point 1), the compensation algorithm is reset and a new two-switching cycle compensation process is started. This compensation algorithm continues to restart until, the input voltage stops changing. Then, the proposed two-switching cycle transient response enters the second switching period (step 2 in Fig. 3). The transient period ends one switching cycle later. When the transient ends, the control system is switched back to the current mode PID controller, which is used to control the steady state and small signal condition. The compensation algorithm calculates the new steady state values i_{Lnew} and D_{new} for the current mode PID controller, and resets the outputs of the current mode PID controller to these calculated values.

It is possible that one or both of the calculated duty cycle values d_1 or d_2 can be higher than 100% or less than 0% if the input voltage step change or the inductor value is very large. This means it needs 3 or more switching cycles for the DC-DC converter to enter the new steady state. In this case, at the beginning of step 1 or step 2 of the improved compensation algorithm, the duty cycle is set to 100% if it is higher than 100%, or set to 0% if it is lower than 0%. In addition, a new two-switching cycle compensation process will be restarted to regulate the converter (shown in Fig. 3).

V. Simulation Results

Using the switching model for DC-DC converters, simulation is performed using MATLAB to verify the effectiveness of the proposed algorithm. The parameters of the Buck converter are as follows: V_{in}=5V, V_o=2.5V, rated power=25W, L=1uH, C=235uF, and f_s=400khz. The proposed algorithm was compared to a current mode PID controller. The parameters of current mode PID controller were optimized in the frequency domain to maximize the bandwidth at a phase margin of 50 degrees.

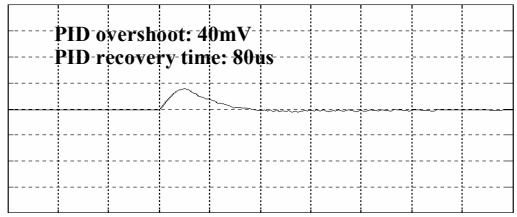
To test the proposed compensation algorithm, input voltage changes of 5V to 7.5V and 7.5V to 5V were used.

Fig. 4 illustrates the output voltage response of the Buck converter when the input voltage changes from 5V to 7.5V in 20us at 5A load current. It is shown in Fig. 4(a) that using the current mode PID controller, the overshoot of the output voltage is 40mv and the recovery time is 80us.

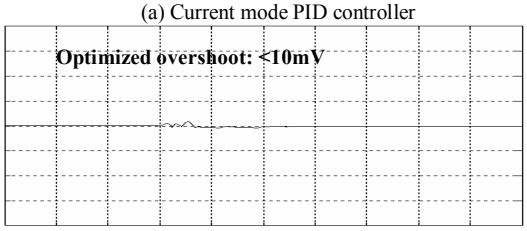
Fig. 5 shows the output voltage response of the Buck converter when the input voltage changes from 5V to 7.5V in 20us at no load. It can be observed from Fig. 5(a) that, using the current mode PID controller, the overshoot of the output voltage is 62mv and the recovery time is 128us.

Fig. 6 illustrates the output voltage response of the Buck converter when the input voltage changes from 7.5V to 5V in 40us at 5A load current. It is shown in Fig. 6(a) that using the current mode PID controller, the undershoot is 32mv and the recovery time is 90us.

However, using the proposed optimal two-switching cycle compensation algorithm, the overshoot/undershoot during the whole transient time is always less than 10mv (shown in Fig. 4 (b), Fig. 5(b) and Fig. 6(b) respectively).

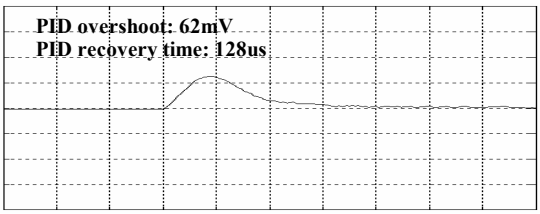


(a) Current mode PID controller

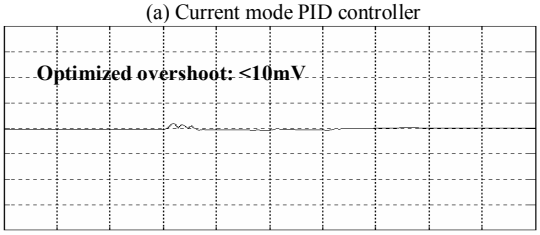


(b) Proposed optimal control algorithm

Fig. 4 Output voltage response to input voltage change from 5V to 7.5V when load current is 5A (X axis: 40us/div; Y axis: 50mv/div)

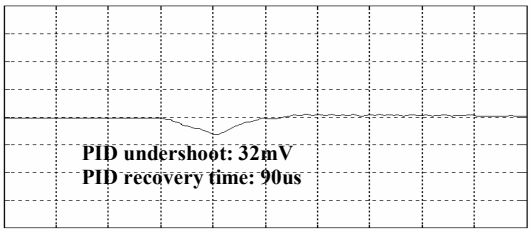


(a) Current mode PID controller

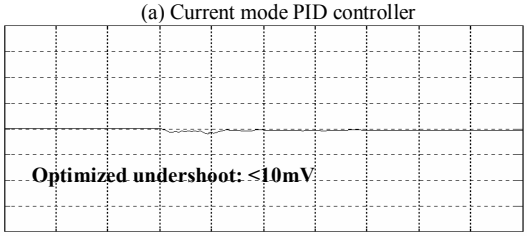


(b) Proposed optimal control algorithm

Fig. 5 Output voltage response to an input voltage change from 5V to 7.5V at no load (X axis: 40us/div; Y axis: 50mv/div)



(a) Current mode PID controller



(b) Proposed optimal control algorithm

Fig. 6 Output voltage response to input voltage change from 7.5V to 5V when load current is 5A (X axis: 40us/div; Y axis: 50mv/div)

VI. Experimental Results

A field programmable gate array (FPGA) was used to

implement the proposed optimal control algorithm in a synchronous Buck converter. The Buck parameters were the same as that used in the simulation. Fig. 7 shows the circuit block diagram of FPGA controlled Buck converter. The FPGA was a Spartan-2E from Xilinx. The clock frequency of the FPGA is 100MHz. In this system, the inductor current is measured using a sensing resistor in series with switch S_1.

Fig. 8 illustrates the output voltage response when the input voltage changes from 5V to 7.5V in 20us at 5A load current. Using the proposed optimal control algorithm, the overshoot is reduced to 11mV from 45mV with the current mode PID controller. It is noted that 11mV is almost buried with the ripple voltage (8mV in the experimental prototype). The recovery time is also reduced to 12us from 72us with current mode PID controller.

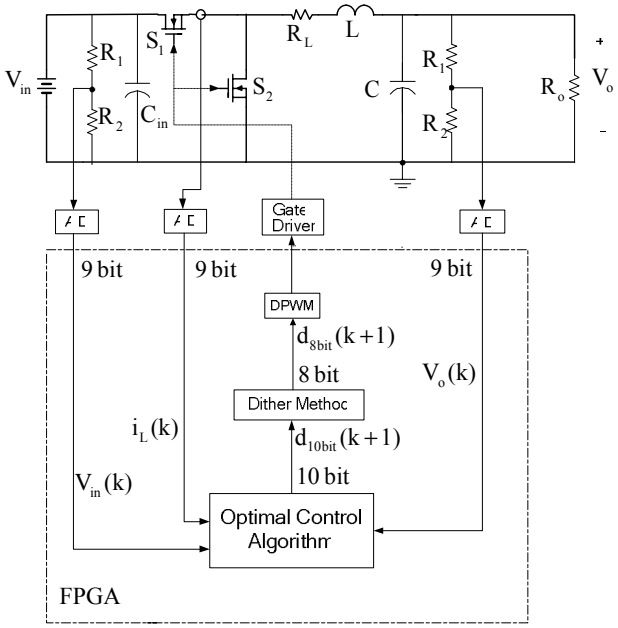
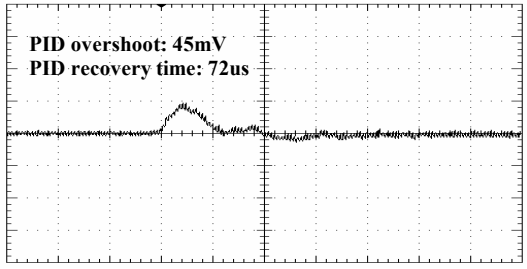
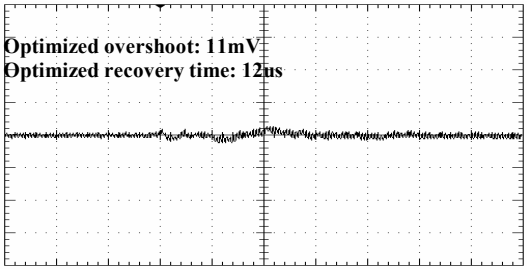


Fig. 7 Diagram of experimental Buck converter test bench using the proposed optimal control algorithms



(a) Current mode PID controller

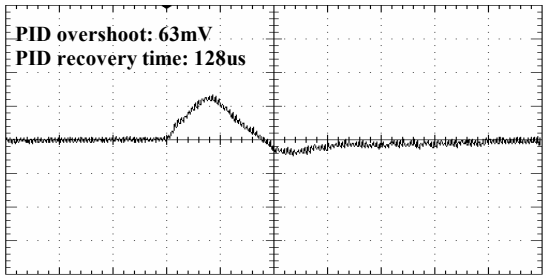


(b) Proposed optimal control algorithm

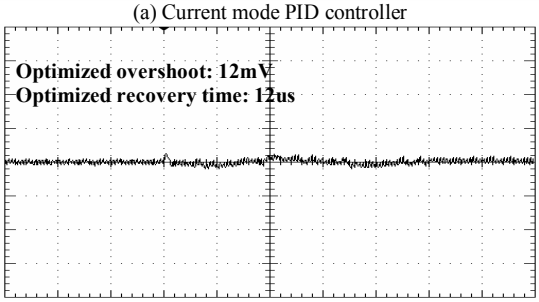
Fig. 8 Output voltage response to an input voltage change from 5V to 7.5V at 5A load (X axis: 40us/div; Y axis: 50mv/div)

Fig. 9 shows the output voltage response when the input voltage changes from 5V to 7.5V in 20us at no load. Again, with the proposed optimal control algorithm, the overshoot is reduced 12mV from 63mV with that of the current mode PID controller. The recovery time is also reduced to 12us from 128us with current mode PID controller.

Fig. 10 demonstrates the output voltage response when the input voltage changes from 7.5V to 5V in 40us at 5A load current. Using the proposed optimal control algorithm, the voltage dip is decreased to 12mV from 38mV with the current mode PID controller. The recovery time is significantly reduced to 12us from 82us with the current mode PID controller.

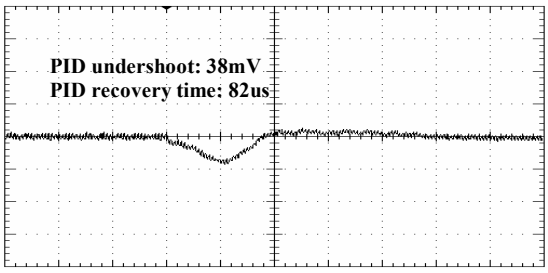


(a) Current mode PID controller

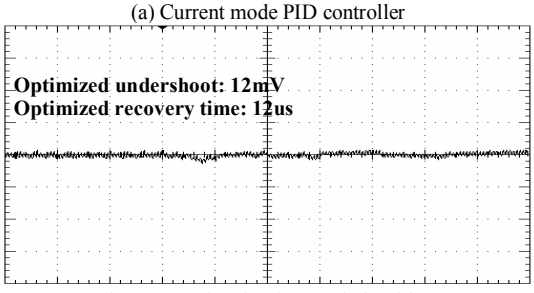


(b) Proposed optimal control algorithm

Fig. 9 Output voltage response to input voltage change from 5V to 7.5V when load current is 0A (X axis: 40us/div; Y axis: 50mv/div)



(a) Current mode PID controller



(b) Proposed optimal control algorithm

Fig. 10 Output voltage response to input voltage change from 7.5V to 5V when load current is 5A (X axis: 40us/div; Y axis: 50mv/div)

The proposed compensation algorithm is insensitive to tolerances of the filter capacitor and inductor. Fig. 11 illustrates the output voltage response to the input voltage change from 5V to 7.5V under different L, C values (+/- 20%). It can be observed from Fig. 11 that the proposed two-switching cycle compensation algorithm can still achieve excellent dynamic performance even when the parameters of the Buck converter are changed. The maximum overshoot/undershoot during the input voltage change is less than 15mv.

VII. CONCLUSIONS

A new two-switching cycle compensation algorithm has been proposed to achieve optimal dynamic performance for the Buck converter under an input voltage change. Using the principle of capacitor charge balance, two duty cycle values after the transient happens are predicted to drive the converter to the new steady state after the input voltage change. As a result, good transient response, specifically, small overshoot/undershoot and short recovery time, is achieved.

The proposed optimal algorithm was tested with a synchronous Buck converter and compared to a conventional PID controller. The experimental results demonstrate that the proposed algorithm achieves excellent dynamic performance. The performance is superior to the conventional current mode PID controller. These results indicate that the proposed algorithm can be an attractive alternative to classic controllers in power converter applications where good dynamic performance is required. The proposed algorithm can be easily applied to other topologies such as the Boost, and Buck-Boost converters.

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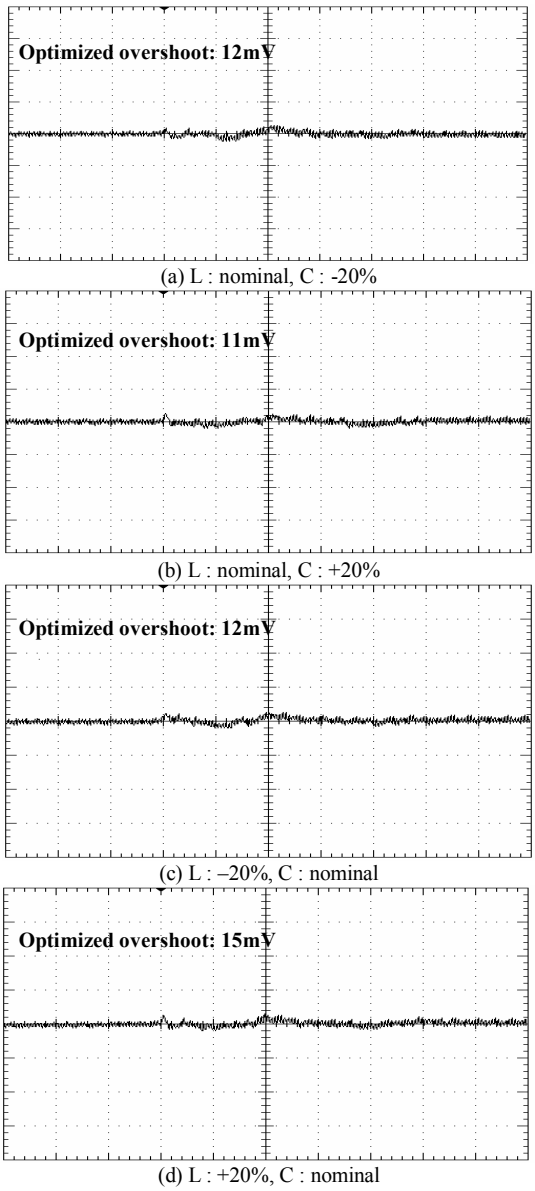

Fig. 11 Experimental result of output voltage response to input voltage change from 5V to 7.5V under different L, C values (load current is 5A) (X axis: 40us/div; Y axis: 50mv/div)