NOTE: This paper has minor revisions from the original published at APEC 2006 in Dallas Texas. This version includes a corrected design procedure section and updated experimental results that were presented at APEC.

A Novel High Performance Resonant Gate Drive Circuit with Low Circulating Current

Wilson Eberle (*Student Member IEEE*), Yan-Fei Liu (*Senior Member IEEE*), **and** P.C. Sen (*Fellow IEEE*)
Queen's Power Group, www.queenspowergroup.com
Department of Electrical and Computer Engineering, Queen's University, Kingston, Ontario, Canada, K7L 3N6
wilsoneberle@wilsoneberle.com, senp@post.queensu.ca and yanfei.liu@queensu.ca

***Abstract* - In this paper, a new resonant gate drive circuit is proposed for power MOSFETs. The proposed circuit can recover a portion of the CV^2 gate energy and it achieves quick turn on and turn off transition times to reduce switching loss and conduction loss in power MOSFETS. The circuit consists of four control switches and a small resonant inductance. The current through the resonant inductance is discontinuous in order to minimize circulating current conduction loss present in other methods. An analysis, design procedure, loss analysis, simulation results and experimental results are presented for the proposed circuit.**

I. INTRODUCTION

In recent years there has been a trend to increase the switching frequency beyond 1MHz in low voltage high current DC-DC power supplies. The objectives of this trend are to increase the power density by decreasing the size of passive components and to improve the dynamic performance. Furthermore, it is well understood that as switching frequency increases, both switching loss and gate loss increase if conventional drivers are used. In the past two decades, much work has been done on reducing, or eliminating switching loss, while relatively little work has been done on reducing gate loss. Therefore, with the improvements achieved through reduction in switching loss, it is now essential to focus some effort on reducing gate loss in order to continue to achieve greater power density and dynamic performance.

A conventional gate drive circuit is illustrated in Fig. 1 to drive a power MOSFET, Q. With these drivers, all of the power MOSFET gate energy is dissipated. Energy is absorbed from the line source, V_{cc} during turn on of Q and then dumped to ground during turn off. For this drive circuit, the gate energy loss due to charging and discharging the gate capacitance of Q is given by (1), where Q_g represents the total gate charge, V_{gs} is the driving voltage and f_s is the switching frequency. This energy is dissipated as RMS loss in: 1) the driver switches Q_N and Q_P, 2) the external resistance, R_{ext}, and 3) the parasitc gate mesh resistance, R_g, of Q. This loss component is well understood and is often called the CV^2 gate loss.

$$P_{gate} = Q_g V_{gs} f_S \qquad (1)$$

In addition to the CV^2 loss, conventional gate drivers exhibit switching loss, shoot-through loss and gate loss in their control switches. These losses are often neglected in mathematical analysis by engineers, which is a mistake. It was demonstrated in [1] and verified experimentally by the present authors that the power MOSFET CV^2 RMS loss is approximately only 65% of the total gate drive circuit loss. The additional components of the gate drive circuit loss include approximately 20% for switching loss and 15% for gate loss in the driver switches Q_N and Q_P. As illustrated in Fig. 3, normalized with respect to the CV^2 RMS gate loss, these components are significant. An additional 31% of loss can be attributed to hard switching in the control switches and 23% to gate loss in the control switches. Neglecting these components yields an under estimate of gate loss that neglects 54% of the CV^2 loss.

The problems of the conventional gate driver extend beyond the gate drive circuit loss. Since these drivers operate with RC type charging and discharging, switching speed is limited since the MOSFET gate current is limited to a value significantly less than the peak driver current during the turn on and turn off times. This is illustrated by simulation in Fig. 2. In this example, the peak driver current is 1.5A. However, during the turn on switching time from the threshold to the end of the Miller plateau, the gate current decays to 0.75A. During the turn off switching time, the problem is even more severe since the gate current decays to -0.25A. Therefore, since these drivers are designed for peak current capability, they are not optimized to minimize switching loss and in particular, turn off switching loss.

In order to recover a portion of the gate energy otherwise lost in conventional drivers, several papers have been published since the early 1990s proposing resonant gate drive techniques. In these techniques, the resonant inductance yields current source drive which has the potential to reduce switching times and therefore switching loss. However, none of the papers have advertised the significant benefit of reduced switching loss due to current source drive.

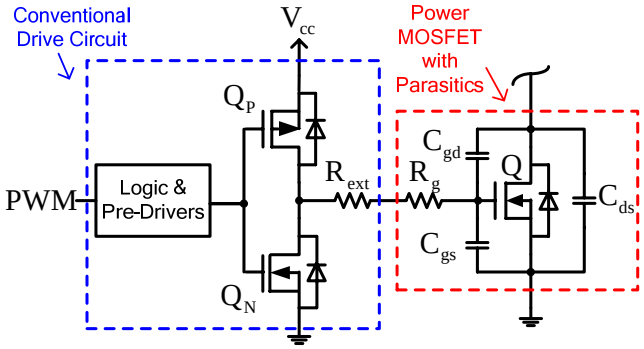

Fig. 1 Conventional gate drive circuit with power MOSFET and its associated parasitics

NOTE: This paper has minor revisions from the original published at APEC 2006 in Dallas Texas. This version includes a corrected design procedure section and updated experimental results that were presented at APEC.

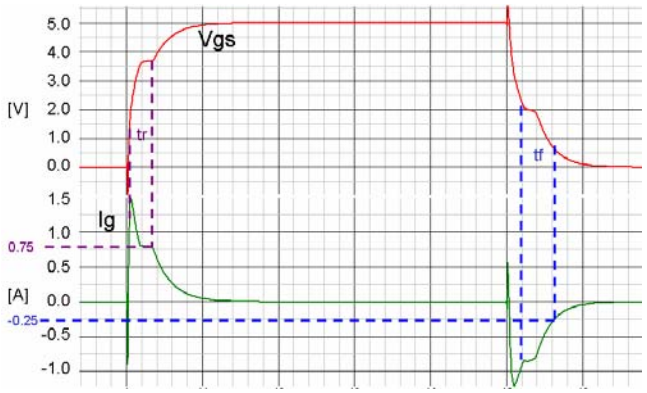

Fig. 2 Power MOSFET gate-to-source voltage, Vgs (top curve) and gate current (bottom curve), Ig during switching transitions

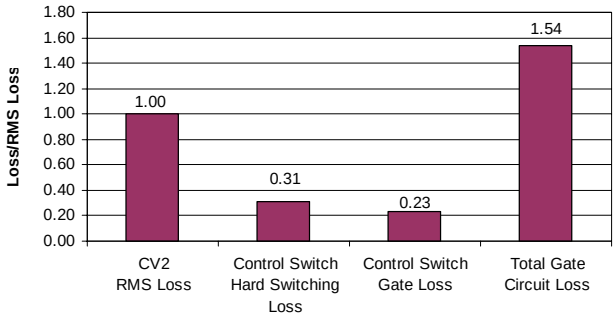

Fig. 3 Conventional gate drive circuit loss normalized with respect the power MOSFET CV^2 gate loss

Of the methods previously proposed, all of them suffer from at least one of five problems:

1) High circulating current in the driver control switches during the power MOSFET on and off states resulting in excessive conduction loss [2].
2) Peak driver current dependent on duty cycle, or switching frequency resulting in switching times and gate loss that varies with the operating point [2] .
3) Large inductance [2], bulky transformer, or coupled inductance [3]-[7].
4) Slow turn on and/or turn off transition times, which increases both conduction and switching losses in the power MOSFET due to charging the power MOSFET gate beginning at zero current [3]-[9].
5) The inability to actively clamp the power MOSFET gate to the line during the on time and/or to ground during the off time, which can lead to undesired false triggering of the power MOSFET gate, i.e. lack of Cdv/dt immunity [3]-[7],[9].

To solve the problems inherent to conventional drivers, the five problems above, and to reduce switching loss, a new resonant gate drive circuit is proposed in the following section.

II. Proposed Resonant Driver and Operation

The proposed resonant gate driver is illustrated in Fig. 4. It consists of four control switches, Q_1-Q_4 including their body diodes, D_1-D_4, and a small inductance, L_R. The switches and diodes are controlled in a way to allow the inductor current to be discontinuous and allow the power MOSFET to turn on or off beginning from a non-zero pre-charge current. Following charging, or discharging of the power MOSFET, the excess inductor stored energy is allowed to return to the line voltage, V_{cc}, thereby allowing ideally 100% of the power MOSFET gate charge energy to be recovered.

The current paths during the four intervals of the turn on stage are illustrated in Fig. 5. The current paths during the four intervals of the turn off stage are illustrated in Fig. 6. The gating waveforms of the four control switches, Q_1-Q_4, along with the inductor current, gate current, power MOSFET gate-to-source voltage and the line current are illustrated in Fig. 7.

The operation of the circuit is explained in the following paragraphs. Initially it is assumed that the power MOSFET is in the off state before time t_0. For the control switches, the shaded regions indicate the on state, so initially only switch Q_3 and D_4 are on and the gate of Q is clamped to zero volts. The black regions indicate the on state for the diodes.

t_0-t_1: At t_0, D_4 turns off with zero current switching (ZCS) and Q_2 turns on (with ZCS) allowing the inductor current to ramp up. The current path during this interval is Q_2-L_R-Q_3. Since Q_3 is in the on state, the gate of Q is clamped low. The interval ends at t_1.

t_1-t_2: At t_1, Q_3 turns off, which allows the inductor current to begin to charge the power MOSFET gate. The inductor current continues to ramp up, but with a reduced slope as the voltage across the gate capacitance increases. The current path during this interval is Q_2-L_R-C_g, where C_g represents the equivalent gate capacitance of Q. This interval ends at t_2, when V_{gs} reaches V_{cc}. If this interval is allowed to continue, D_1 allows the current to freewheel through Q_2-L_R-D_1.

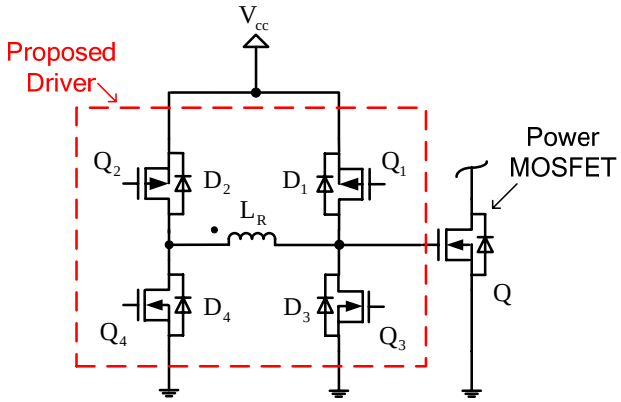

Fig. 4 Proposed resonant gate drive circuit

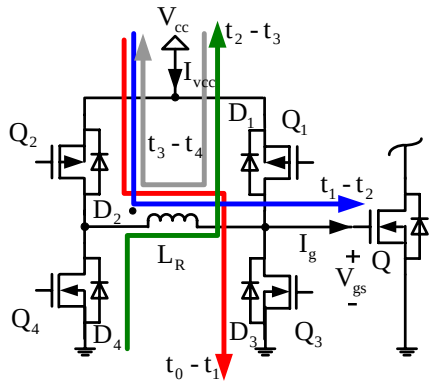

Fig. 5 Proposed resonant gated drive circuit current paths during the turn on interval

NOTE: This paper has minor revisions from the original published at APEC 2006 in Dallas Texas. This version includes a corrected design procedure section and updated experimental results that were presented at APEC.

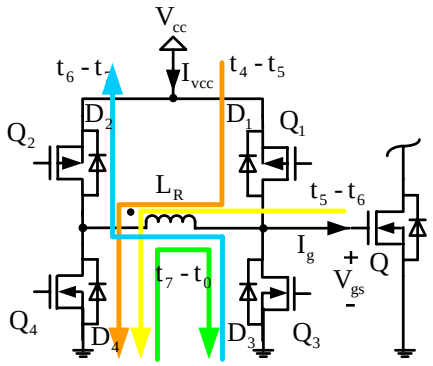

Fig. 6 Proposed resonant gated drive circuit current paths during the turn off interval

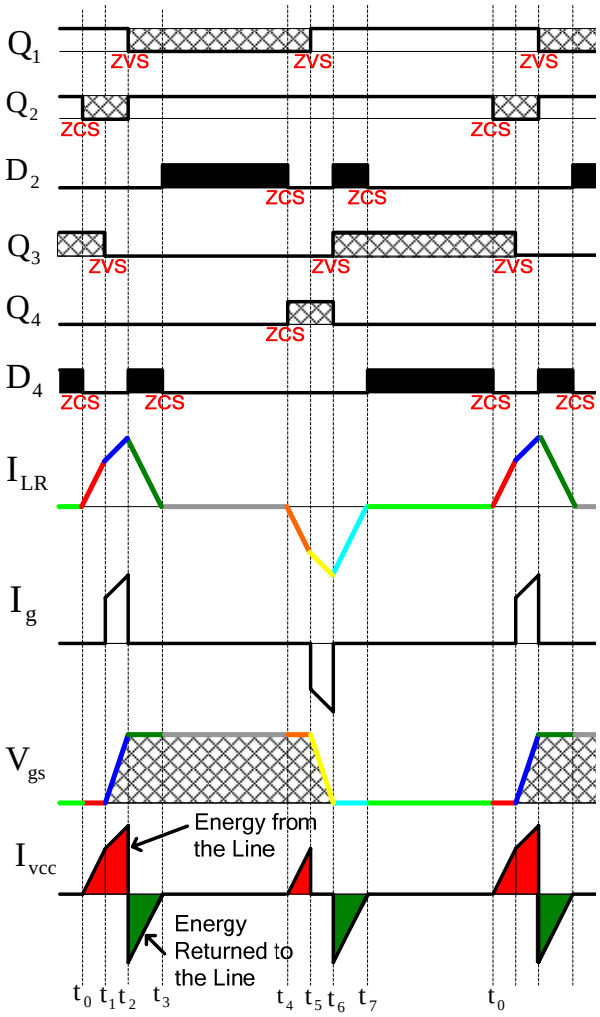

Fig. 7 Waveforms of the proposed resonant gate driver

t_2-t_3: At t_2, Q_2 turns off and Q_1 turns on with zero voltage switching (ZVS) and D_4 turns on, allowing the inductor current to conduct into the dot through the path D_4-L_R-Q_1. Most importantly, it is during this interval when the stored energy in the inductor is returned to the line. This can be observed from the negative portion of the I_{Vcc} curve in Fig. 7. Also, during this interval, the inductor voltage has become reverse biased, so the inductor current quickly ramps down towards zero. During this interval, the gate voltage of Q remains clamped to the line voltage, V_{cc}. The interval ends when the inductor current reaches zero at t_3.

t_3-t_4: At t_3, D_4 turns off (with ZCS) and D_2 turns on, which allows any residual inductor current to freewheel through Q_1-L_R-D_2. During this interval, the gate voltage of Q remains clamped to V_{cc}. The interval ends at t_4 when the pre-charging interval for the turn off cycle begins as dictated by the PWM signal.

t_4-t_5: At t_4, the turn off pre-charging interval begins. D_2 turns off (with ZCS) and Q_4 turns on (with ZCS). Since Q_1 was previously on, the inductor current begins to ramp negative out of the dot through the path Q_1-L_R-Q_4. During this interval, the gate voltage of Q remains clamped to V_{cc}. The interval ends at t_5.

t_5-t_6: At t_5, Q_1 turns off, which allows the inductor current to begin to discharge the power MOSFET gate. The inductor current continues to ramp negative, but with a reduced slope as the voltage across the gate capacitance decreases. The current path during this interval is C_g-L_R-Q_4, where C_g represents the equivalent gate capacitance of Q. This interval ends at t_6, when V_{gs} reaches zero. If this interval is allowed to continue, D_3 allows the current to freewheel through D_3-L_R-Q_4.

t_6-t_7: At t_6, Q_4 turns off and D_2 turns on and Q_3 turns on (with ZVS) allowing the inductor current to conduct out of the dot through the path Q_3-L_R-D_2. Most importantly, it is during this interval when the gate discharging energy is returned to the line. This can be observed from the negative portion of the I_{Vcc} curve in Fig. 7. Also, during this interval, the inductor voltage has become reverse biased, so the inductor current quickly ramps down positive towards zero. During this interval, the gate voltage of Q remains clamped to ground. The interval ends when the inductor current reaches zero at t_7.

t_7-t_0: At t_7, D_2 turns off (with ZCS) and D_4 turns on, which allows any residual inductor current to freewheel through D_4-L_R-Q_3. During this interval, the gate voltage of Q remains clamped to ground. The interval ends at t_0 when the pre-charging interval for the turn on cycle begins and the entire process repeats as dictated by the PWM signal.

III. Logic Implementation

The logic required to produce the gating signals for the four control switches, Q_1-Q_4 is very simple. The logic circuit is illustrated in Fig. 8. The circuit requires only 2 delay elements and 6 logic elements. The delay elements can be implemented using tapped delay line ICs. The delayed PWM signals are labeled TD1 and TD2 in Fig. 8. The output of the logic circuit is the four gate drive signals. Following the logic, pre-drivers (not shown) should be used to drive the control switches. These can be implemented with a simple Bipolar totem pole pair. The waveforms used to derive the logic are illustrated in Fig. 9.

IV. Design Procedure

The power MOSFET turn on transition time, t_{on}, (from 0V to V_{cc}) is not calculated, but must be chosen by the designer for the given application. For the designer, there is a tradeoff between speed, which translates into switching loss savings, and gate energy recovery. Smaller values of t_{on} reduce

NOTE: This paper has minor revisions from the original published at APEC 2006 in Dallas Texas. This version includes a corrected design procedure section and updated experimental results that were presented at APEC.

switching loss, but require greater peak current in the driver and therefore suffer from greater conduction loss in the driver. Typically, t_{on} should be less than 10% of the switching period. After selecting t_{on}, the turn on inductor pre-charge time, t_{d1} should be selected. This is illustrated in Fig. 10 from t_0-t_1, of the inductor current waveform during the turn on interval. Typically, t_{d1} should be less than t_{on}. Larger values of t_{d1} yield a larger required inductance and add more delay in the control loop. On the other hand, if t_{d1} is too small, the gate energy recovery is limited, or the pre-charge current level is small. A typical starting value of t_{d1} is half of t_{on}.

In order to calculate the required resonant inductance, (2)-(4), must be used.

Equation (2) is derived assuming that there is no resistive loss in the drive circuit during t_{d1}.

$$L_R = \frac{V_{cc} t_{d1}}{i_{LR}(t_1)} \tag{2}$$

Equation (3) is derived using an approximation. The equivalent resonant circuit during t_{on} is complex to solve, but since the power MOSFET gate capacitor voltage increases from zero to V_{cc} during t_{on}, then the average capacitor voltage during the interval is $V_{cc}/2$. Using this approximation, the ripple current component, Δi_{LR}, is approximated as (3).

$$\Delta i_{LR} \approx \frac{V_{cc}}{2} \frac{t_{on}}{L_R} \tag{3}$$

The current at time t_1 is then approximated by (4).

$$i_{LR}(t_1) \approx I_{avg} - \frac{\Delta i_{LR}}{2} \tag{4}$$

Using (2)-(4), the required resonant inductance can be calculated using (5).

$$L_R = \frac{V_{cc} t_{on}}{Q_g} \left(\frac{t_{on}}{4} + t_{d1} \right) \tag{5}$$

The design procedure is summarized as follows:

1) Set the turn on transition time, t_{on}. This value is typically no more than 10% of the total switching period in order to minimize conduction loss, duty cycle loss and switching loss.
2) Set the turn on pre-charge current time, t_{d1}.
3) Calculate the resonant inductance using (5).

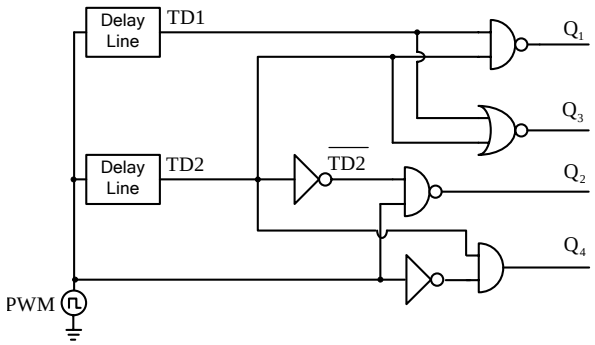

Fig. 8 Logic circuit

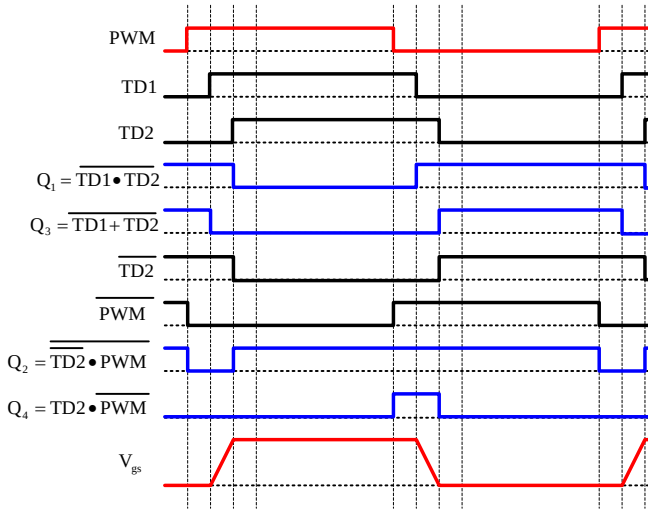

Fig. 9 Logic waveforms

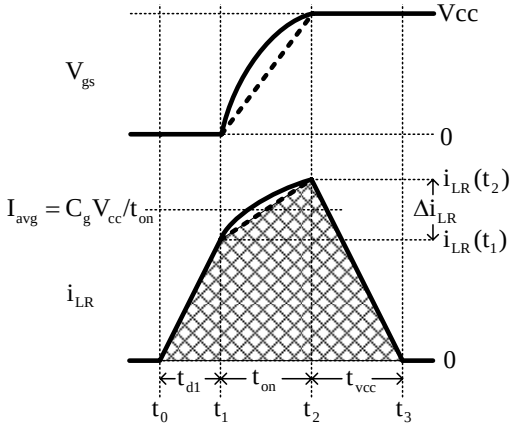

Fig. 10 Detailed inductor current waveform and power MOSFET gate voltage during the turn on interval

V. Loss Analysis

Switches Q_1 and Q_3 turn on with zero voltage switching and since they are shunted by the large gate capacitance, C_g, their turn off loss is negligible. Switches Q_2 and Q_4 turn on with zero current switching. The sources of loss in the proposed driver include:

1) Conduction loss in the control switches, diodes, inductor winding resistance and MOSFET gate resistance.
2) Gate loss in Q_1-Q_4.
3) Output CV^2 turn on loss in Q_2 and Q_4.
4) Turn off loss in Q_2 and Q_4.
5) Inductor core loss.
6) Logic loss.

A. Conduction Loss

This sub-section will focus on the conduction loss in the control switches. The equivalent circuit for loss analysis of the proposed driver is given in Fig. 11. The power MOSFET being driven is represented by an RC network consisting of its parasitic series gate resistance, R_g, and an equivalent gate capacitance, C_g, which is calculated using (6) and total gate charge data from the device datasheet. During the on state, the control switches can be represented by series resistances R_1-R_4. The inductor copper loss can be represented by an

equivalent series AC resistance, R_L, which can be estimated, measured, or obtained from the inductor datasheet.

$$C_g = \frac{Q_g}{V_{cc}} \tag{6}$$

The conduction loss in the proposed resonant gate driver can be determined by analyzing the losses during the three main states of the turn on interval (t_0-t_3) and three states of the turn off interval (t_4-t_7) when the inductor current is non-zero.

The detailed inductor current waveform and power MOSFET gate voltage waveform are shown for the turn on interval in Fig. 10. The actual inductor current waveform will follow the shape given by the solid line with a non-linear transition during the turn on of the gate voltage. Using a piecewise linear approximation to simplify the analysis, the inductor current waveform can be approximated using the dotted portion during t_{on}, if it is assumed that the gate is driven by a constant current source of value I_{avg} during t_{on}. Under this assumption, the entire interval is given by the shaded region.

In Fig. 10, the inductor current pre-charge interval is labeled t_{d1} and it occurs from time t_0 to t_1. The turn on interval is labeled t_{on}, and it occurs from time t_1 to t_2. The ramp down interval is labeled t_{ret} and it occurs from t_2 to t_3.

The analysis of the turn on intervals is explained as follows.

t_{d1}: The equivalent circuit during t_a is given in Fig. 12. During this interval switches Q_2 and Q_3 are on, so the circuit is a series RL circuit consisting of R_2, R_L, R_3 and L_R, where the resistances R_2, R_L and R_3 have been lumped together as R_{td1}. The inductor current, $i_{LR}(t)$, is given by (7). Since the series resistance R_{td1} is quite small, the time constant is large relative to the transition interval, so (7) can be approximated by (8). Using the approximation, the RMS current during this interval is given by (9) and the power consumption, P_{td1}, during the interval is given by (10).

$$i_{LR}(t) = \frac{V_{cc}}{L_R} t e^{-\frac{R_{td1a}}{L_R} t} \tag{7}$$

$$i_{LR}(t) \approx \frac{V_{cc}}{L_R} t \tag{8}$$

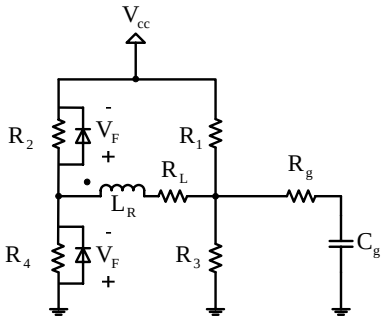

Fig. 11 Proposed resonant gate driver equivalent circuit

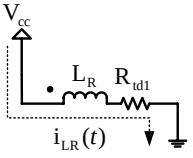

Fig. 12 Equivalent circuit during the pre-charge interval t_{d1}

$$i_{td1\_RMS} = i_{LR}(t_1)\sqrt{\frac{t_{d1} f_S}{3}} \tag{9}$$

$$P_{td1} = i_{LR}(t_1)^2 \frac{t_{d1} f_S}{3} R_{td1} \tag{10}$$

The pre-charge time interval can be derived as (11).

$$t_{d1} = \frac{L_R}{V_{cc}} i_{LR}(t_1) \tag{11}$$

t_{on}: The equivalent circuit during t_{on} is given in Fig. 13. During this interval only switch Q_2 is on, so the circuit is a series RLC circuit consisting of R_2, R_L, R_G, L_R and C_g, where the resistances R_2, R_L and R_G have been lumped together as R_{on}. The inductor current, $i_{LR}(t)$, is given by (12), which is quite complex to calculate the RMS value during the given interval. However, using the piecewise linear approximation illustrated in Fig. 10, the RMS current during t_{on} is given by (13) and the power consumption, P_{on}, during the interval is given by (14).

$$i_{LR}(t) = \frac{V_{cc}\sqrt{L_R C_g}}{L_R} \sin\left(\frac{1}{\sqrt{L_R C_g}} t\right) + i_{LR}(t_1)\cos\left(\frac{1}{\sqrt{L_R C_g}} t\right) \tag{12}$$

$$i_{on\_RMS} \approx \sqrt{t_{on} f_S}\sqrt{\left[\frac{i_{LR}(t_2)+i_{LR}(t_1)}{2}\right]^2 + \frac{\left[i_{LR}(t_2)-i_{LR}(t_1)\right]^2}{12}} \tag{13}$$

$$P_{on} = t_{on} f_S \left(I_{avg}{}^2 + \frac{\Delta i_{LR}{}^2}{12}\right) R_{on} \tag{14}$$

t_{vcc}: The equivalent circuit during t_{vcc} is given in Fig. 14. During this interval diode D_4 and switch Q_1 are on, so the circuit is a series R_L circuit consisting of D_4, R_L, R_1 and L_R, where the resistances R_L and R_1 have been lumped together as R_{vcc} and the diode voltage drop is considered constant at V_F. The inductor current, $i_{LR}(t)$, is given by (15). Since the series resistance R_{vcc} is quite small, the time constant is large relative to the transition interval, so (15) can be approximated by (16). Using the approximation, the RMS current during this interval is given by (17) and the power consumption, P_{vcc}, during the interval is given by (18).

$$i_{LR}(t) = i_{LR}(t_2) - \frac{V_{cc} - V_F}{L_R} t e^{-\frac{Rvcc}{L_R} t} \tag{15}$$

$$i_{LR}(t) \approx i_{LR}(t_2) - \frac{V_{cc} - V_F}{L_R} t \tag{16}$$

$$i_{vcc\_RMS} = i_{LR}(t_2)\sqrt{\frac{t_{vcc} f_S}{3}} \tag{17}$$

$$P_{vcc} = i_{LR}(t_2)^2 \frac{t_{vcc} f_S}{3} R_{vcc} + V_F \int_{t_2}^{t_3} \left(i_{LR}(t_2) - \frac{V_{cc} - V_F}{L_R} t\right) dt \tag{18}$$

The time interval t_{vcc} can be expressed as (19).

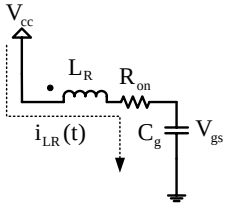

Fig. 13 Equivalent circuit during the turn-on transition interval t_{on}

NOTE: This paper has minor revisions from the original published at APEC 2006 in Dallas Texas. This version includes a corrected design procedure section and updated experimental results that were presented at APEC.

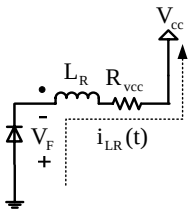

Fig. 14 Equivalent circuit during the ramp down interval t_{vcc}

$$t_{vcc} = \frac{L_R}{V_{cc} + V_F} i_{LR}(t_2) \tag{19}$$

During turn off, the three states of operation have the same loss as the turn on states previously analyzed with the small exception that during the gate discharge interval (t_5-t_6), the discharge path is through the n-channel MOSFET Q_4 instead of the p-channel MOSFET Q_2. To simplify the analysis, it can be assumed that the turn on and turn off states of operation are identical. Therefore, under this assumption, the total conduction loss in the proposed resonant gate drive circuit is two times the sum of P_{td1} plus P_{on} plus P_{vcc} as given by (20).

$$P_{cond} = 2(P_{td1} + P_{on} + P_{vcc}) \tag{20}$$

B. *Gate Loss*

The gate loss in Q_1-Q_4 is given by (21).

$$P_{Q1-Q4\,gate} = (Q_{g1} + Q_{g2} + Q_{g3} + Q_{g4})V_{cc} f_s \tag{21}$$

C. *CV^2 Output Loss*

The CV^2 output loss in Q_2 and Q_4 at turn on, is given by (22) where C_{oss2} and C_{oss4} represent the output capacitance values for Q_2 and Q_4 obtained from the MOSFET data sheets.

$$P_{out} = (C_{oss2} + C_{oss4})V_{cc}^{\ 2} f_s \tag{22}$$

D. *Turn Off Loss*

Q_2 and Q_4 turn off at the peak inductor current, $i_{LR}(t_2)$. The turn off loss in Q_2 and Q_4 is given by (23) where the fall times, t_{f2} and t_{f4} are obtained from the MOSFET data sheets.

$$P_{off} = \frac{1}{2} V_{cc} i_{LR}(t_2)(t_{f2} + t_{f1}) f_s \tag{23}$$

E. *Core Loss*

The core loss can be obtained by standard core loss estimation methods. If the inductor is designed such that core loss equals copper loss, the core loss can be included in the conduction loss estimate by doubling R_L. For certain applications, with a small resonant inductance, it is also possible to use an air core inductor with zero core loss.

F. *Logic Loss*

The loss in the logic circuit should be negligible in comparison to the other components, so it can be neglected.

VI. Design Example

A loss analysis of the proposed driver was conducted using the parameters in Table 1. The results were compared to the estimated loss in a conventional driver with 1.54 times the CV^2 loss as calculated in section I. The results are given in Fig. 15 for 5V drive (left bars) and 12V drive (right bars). For the 12V drive configuration, it was assumed that n-channel devices were used for Q_1 and Q_2 and that a level shift circuit is used to shift the logic level control signals for Q_1 and Q_2.

Table 1 Loss Analysis Parameters and Components

V_{cc} [V]	5		12
f_s [MHz]	1		
t_{on} [ns]	50		100
L_R [nH]	185		800
R_L [mΩ]	25		75
Part #	**MBR0520L**		
Parameter	D2, D4		
V_F [V]	0.385		
	Vcc=5V		Vcc=12V
Part #	**IRF6618**		
Parameter	Q		
V_{ds} [V]	10		10
V_{gs} [V]	5		12
Q_g [nC]	45		100
C_g [nF]	9		8.3
R_g [mΩ]	1000		1000
V_{cc} [V]	5		12
Part #	**FDN342P**	**FDN335N**	
Parameter	Q1,Q2	Q3,Q4	Q1,Q2,Q3,Q4
V_{ds} [V]	5	5	12
V_{gs} [V]	5	5	5
Q_g [nC]	6.5	3.25	3.6
C_g [nF]	1.30	0.65	0.72
R_{ds} [mΩ]	60	50	50
C_{oss} [pF]	225	100	75
t_f [ns]	5	1.5	3.5

For the 5V drive case, approximately 30% of the gate driver energy is recovered in comparison to the conventional driver. For the 12V case, approximately 70% of the gate driver energy is recovered in comparison to the conventional driver.

The largest loss component is due to the power MOSFET parasitic gate resistance, R_g. Curves of loss recovery as a function of R_g are given in Fig. 16 in order to demonstrate the potential benefits of using MOSFETS with lower R_g.

In order to demonstrate the tradeoff between speed and energy recovery, an analysis was conducted using the design procedure and component parameters in Table 1.

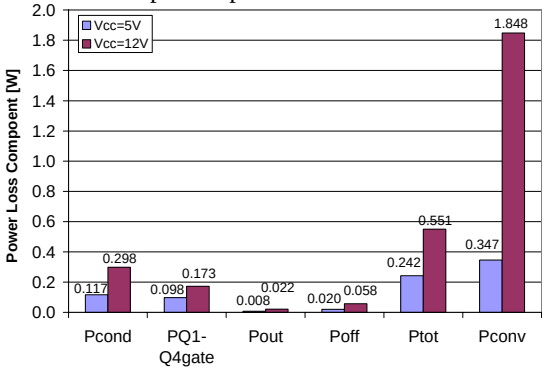

Fig. 15 Calculated gate drive loss breakdown (Vcc=5V left bar, Vcc=12V right bar; conventional driver far right bars)

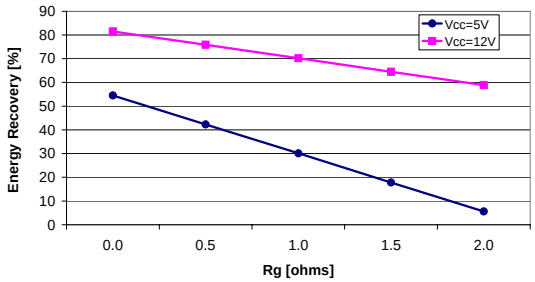

Fig. 16 Energy recovery as a function of R_g in comparison to a conventional gate driver

NOTE: This paper has minor revisions from the original published at APEC 2006 in Dallas Texas. This version includes a corrected design procedure section and updated experimental results that were presented at APEC.

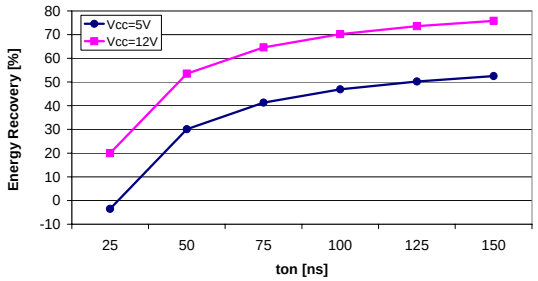

Fig. 17 Energy recovery as a function of t_{on} (speed)

VII. Simulation and Experimental Results

SIMetrix 5.1, was used to simulate the proposed resonant gate driver with a Boost converter using the parameters given in Table 2. Spice models were used for all components. The resonant driver was compared to a conventional driver consisting of one complementary pair MOSFET Si3585DV with external current limiting resistor.

Table 2 Boost Converter Simulation Parameters

Parameter	Boost	Parameter	Resonant Driver	Parameter	Conventional Driver
Vin	5V	**V_{cc}**	12V	**Q_N, Q_P**	Si3585DV
Vo	10V	**t_{on}**	100ns	**R_{ext}**	6Ω
f_s	1MHz	**L_R**	800nH	**Ipk**	2A
Rload	1Ω	**Q_1-Q_4**	FDN335N		
I_L	20A	**D_2,D_4**	MBR0520L		
L	470nH	**R_L**	75mΩ		
C	50uF	**Pre-drivers**	MMBT3904 MMBT3906		
Q	IRF6618	**V_{dd} logic**	5V		
D	10TQ045	**t_{d1}**	40ns		
		t_{d2}	140ns		

The waveforms for the proposed driver are illustrated in Fig. 18. It is clear that since the line current, I_{vcc} goes negative, therefore gate energy is saved. The proposed driver recovered 68% of the gate energy in comparison to the conventional driver. This is close the 70% calculated in the design example.

More impressive than the gate energy recovery was the switching loss savings. The total conduction and switching loss power dissipated in Q in the conventional driver was 4.715W, however with the resonant driver, only 2.658W were dissipated. Both drivers achieved a turn on rise time of approximately 30ns, however the resonant driver achieved a turn off fall time of only 15ns in comparison to 38ns for the conventional driver. It is clear that potential switching loss savings using the proposed driver is very significant.

A prototype of the proposed driver has been built using discrete components. The gating signals for the four control switches are illustrated in Fig. 19.

VIII. Conclusions

A new resonant gate drive circuit has been proposed that can recover power MOSFET gate energy and reduce switching loss. The current in the resonant inductance is discontinuous to minimize conduction loss. This also allows the driver to operate effectively over a wide range of duty cycles with constant peak current – a significant advantage for many applications since turn on and turn off times do not vary with the operating point. The driver provides superior performance in comparison to conventional drivers and solves the problems of existing resonant gate drivers.

A simple design procedure has been included in order to determine the optimum inductor value and delay times. A loss analysis and design example have also been presented in addition to simulation and experimental results. It was demonstrated that the proposed driver reduced the switch loss in a 1MHz Boost converter by 43%.

Boost converter experimental results are illustrated for 5V gate drive in Fig. 20 and 12V gate drive in Fig. 21. The switching frequency of the Boost was 1MHz and two IRF6618 MOSFETs were used in parallel. The Boost diode was 10TQ035. The results were compared to the UCC37322 conventional gate driver. At 5V a 4% efficiency improvement was achieved with the resonant driver at full load. At 12V a 6.5% efficiency improvement was achieved at full load.

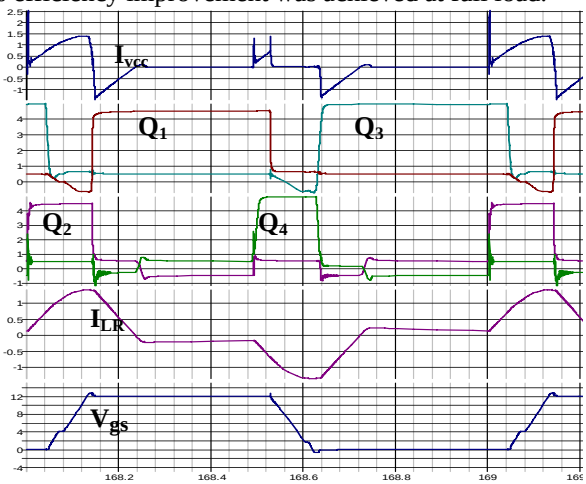

Fig. 18 Simulation results for the proposed driver at 1MHz switching frequency (top: line current from V_{CC}, second: Q_1 & Q_3 gate signals, third: Q_2 & Q_4 gate signals, fourth: L_R current, bottom: power MOSFET gate voltage)

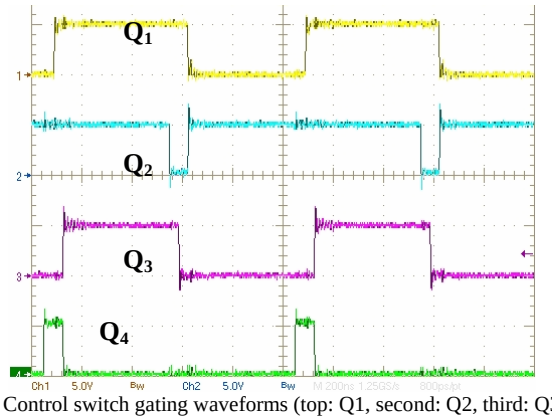

Fig. 19 Control switch gating waveforms (top: Q1, second: Q2, third: Q3, bottom: Q4, X axis: 200ns/div, Y axis: 5V/div)

NOTE: This paper has minor revisions from the original published at APEC 2006 in Dallas Texas. This version includes a corrected design procedure section and updated experimental results that were presented at APEC.

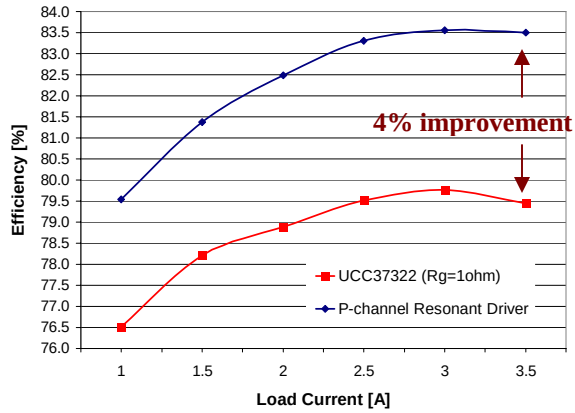

Fig. 20 Boost converter efficiency at 5V Vcc

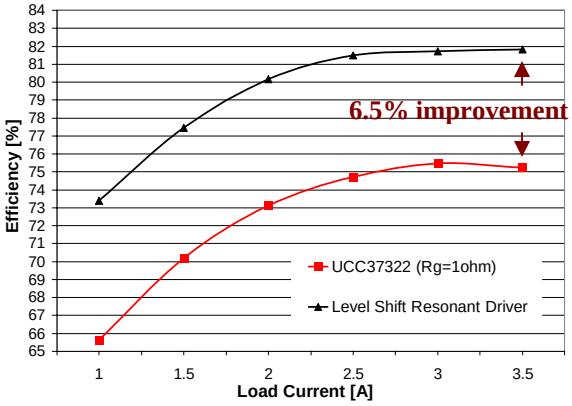

Fig. 21 Boost converter efficiency at 12V Vcc

REFERENCES

[1] T. Lopez, G. Sauerlaender, T. Duerbaum, T. Tolle, "A detailed analysis of a resonant gate driver for PWM applications," IEEE Applied Power Electronics Conference (APEC), 2003, pp. 873-878.

[2] D. Maksimovic, "A MOS gate drive with resonant transitions," IEEE Power Electronics Specialists Converence (PESC), 1991, pp. 527-532.

[3] H.L.N. Wiegman, "A resonant pulse gate drive for high frequency applications," IEEE Applied Power Electronics Conference (APEC), 1992, pp. 738-743.

[4] S.H. Weinberg, "A novel lossless resonant MOSFET driver," IEEE Power Electronics Specialists Conference (PESC), 1992, pp. 1003-1010.

[5] B.S. Jacobson, "High frequency resonant gate drive for a power MOSFET," High Frequency Power Conversion Conference (HFPC), 1993, pp. 133-141.

[6] J. Diaz, M.A. Perez, F.M. Linera and F. Aldana, "A new losless power MOSFET driver based on simple DC/DC converters," IEEE Power Electronics Specialists Conference (PESC), 1995, pp. 37-43.

[7] K. Yao, F.C. Lee, "A novel resonant gate driver for high frequency synchronous buck converters," IEEE Transactions on Power Electronics, Vol. 17, No. 2, March 2002, pp.180-186.

[8] L. Faye, Q. Jinrong, "Gate driver apparatus having an energy recovering circuit," United States Patent No. US 6,650,169 B2, Nov. 18, 2003.

[9] Y. Chen, F.C. Lee, L. Amoroso, H. Wu, "A resonant MOSFET gate driver with efficient energy recovery," IEEE Transactions on Power Electronics, Vol. 19, No.2, March 2004, pp.470-477.