A New Resonant Gate Drive Circuit for Synchronous Buck Converter

Zhihua Yang*, Sheng Ye and Yan-Fei Liu (Senior Member IEEE)

Dept. of Electrical and Computer Engineering

Queen's University, Kingston, Ontario, Canada, K7L 3N6

Email: zhihua.yang@gmail.com, sheng.ye@queensu.ca and yanfei.liu@queensu.ca

Abstract: **The paper proposed a new resonant gate drive circuit for Buck converter with synchronous rectifier. The circuit can recover more than 50% of the conventional gate drive loss. It charges and discharges the gate of MOSFET at constant current. It can also reduce the switching loss significantly. Other advantages of the proposed circuit include better noise immunity for dv/dt turn on, less sensitive to track inductance. The experimental prototype shows that the loss reduction is 10% of the output power at 1MHz.**

I. INTRODUCTION

Powering the latest microprocessor is always a challenge to power industry. Buck converter is used almost exclusively for this application. In order to reduce size and to meet the stringent transient response requirement, the switching frequency of a Buck converter that converts 12V bus voltage to 1.5V and lower to power the CPU core has to be increased to beyond 1MHz range. Another benefit of high switching frequency is lower cost as ceramic capacitor would be enough to provide the hold up during transient operation.

With high switching frequency operation, the switching loss and gate drive loss are both increased [1]. Using the conventional gate drive scheme with voltage source driven approach, when switching frequency is increased to higher than 1MHz, significant compromise has to be made between conduction loss and frequency related loss, such as switching loss and gate drive loss. MOSFET with higher on resistor has to be used in order to reduce the switching loss and gate drive loss. In addition, the impact of the parasitic inductor caused by PCB track becomes worse. The parasitic inductance introduced by PCB track will reduce the turn on and turn off time of the MOSFET, which further increases the switching loss. Another possible problem with Buck converter at high switching frequency operation is dv/dt turn on for the synchronous FET.

Therefore, effective gate drive scheme is needed to meet this challenge. Resonant gate drive schemes have been proposed to reduce the gate drive loss, [2]-[11]. However, most of them are designed for one MOSFET which increases the complexity and cost for 2 MOSFET driving required by Buck converter [2]-[8]. Some of them require transformers which further increases the complexity and cost [9]-[10]. Only one resonant gate driver circuit is for two MOSFETs driving required by Buck converters [11]. However, this circuit is complicated and more importantly, the MOSFET gate remains open during on and off period, which is prone to noise and causes malfunction. Other problems of the existing resonant gate drive schemes include (1) it can only recover the gate drive energy, which limit the potential for total power saving; (2) minimum Ton time is needed; (3) it is difficult to achieve high side driver.

This paper presents a new resonant gate drive circuit for synchronous Buck converter that can reduce both the gate drive loss and switching loss. It uses a constant current level to charge and discharge the MOSFET gate capacitor. Other benefit includes simple circuit configuration, better dv/dt turn on immunity, less impact by parasitic inductance.

II. OPERATING PRINCIPLE OF THE PROPOSED RESONANT GATE DRIVE CIRCUIT

The proposed new resonant gate drive circuit is shown in Figure 1. The circuit consists of four switches *S1 – S4*, which is inherited from dual channel conventional gate drive circuit, connecting as a bridge configuration, an inductor, *L1* and a capacitor *C1* connecting across the bridge. Diode D1 and capacitor C2 consist of a charge pump circuit. Capacitors, C_{g_Q1} and C_{g_Q2}, are the gate capacitors of the power MOSFETs *Q1* and *Q2* respectively. Q1 is the high side switch and Q2 is the lower side switch. V_c is the voltage source. In order to simplify the implementation, P-channel MOSFET is used for *S1* and *S2* and N-channel MOSFET is used for *S3* and *S4*. It is noted that other implementation methods can also be used to achieve the same objective.

The proposed resonant gate drive circuit shown in Figure 1 can operate in both complementary and symmetrical mode. It provides two drive signals with duty cycle D and 1-D respectively when it works in complementary mode, which can be used for driving two MOSFETs in a synchronous buck converter or primary MOSFETs in an asymmetrical half bridge converter. It provides two drive signals with the same duty cycle when it works in symmetrical mode, which can be applied to drive two primary MOSFETs in half bridge and

* Zhihua Yang has been graduated from Queen's University. Now he is working in Paradigm Advanced Research Center of Paradigm Electronics Inc. 5340 Canotek Road, Unit #4, Ottawa, Ontario, K1J 9C6, Canada

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full bridge converters.

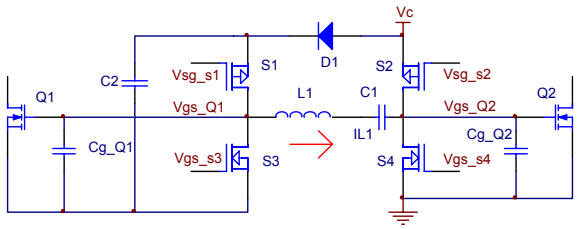


Figure 1 Dual channel high side and low side resonant gate drive circuit

The following provides the detailed operation of dual high side and low side resonant gate driver circuit operating at complementary mode. The duty cycle for *Q1* is *D* and duty cycle for *Q2* is *1 – D*. In high side and low side configuration, the current of the resonant inductor will flow through the power train of the converter in addition to the switches *S1-S4*. A synchronous buck converter is used for the operation principle depiction. The key waveforms are shown in Figure 2 and a synchronous buck converter with the proposed resonant gate drive circuit is shown in Figure 3.

In Figure 2, V_{sg_S1}, V_{sg_S2}, V_{gs_S3}, and V_{gs_S4} are gate drive signals for *S1 – S4*. V_{gs_Q1} and V_{gs_Q2} are the voltage across C_{g_Q1} and C_{g_Q2}. The rising edge and falling edge of V_{gs_Q1} and V_{gs_Q2} are shown to illustrate the details of charging and discharging interval. I_{L1} is the current waveform through inductor *L1*. In the analysis, it is assumed that capacitor *C1* is very large and the voltage across *C1* is a DC value. If the capacitor value *C1* is small, the operation of the circuit does not change.

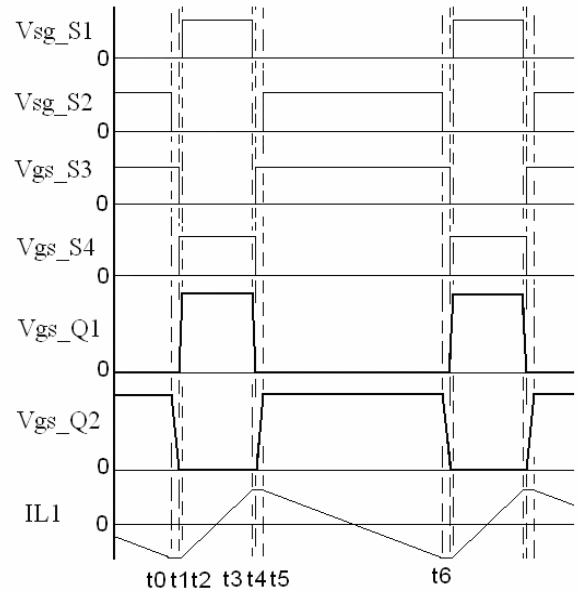


Figure 2 Typical waveforms of dual channel high side and low side resonant gate drive circuit with complementary drive signal

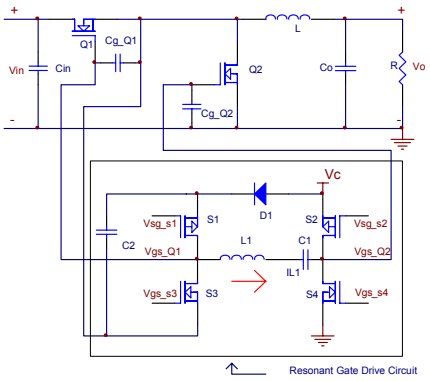


Figure 3 Synchronous buck converter with dual high side and low side gate drive circuit

The operation of this circuit can be briefly described as following by six operation modes as shown in Figure 4:

(1) Before t0:

S1 and *S4* are off while *S2* and *S3* are on. *Q1* is off and *Q2* is on. The inductor current, I_{L1}, increases to negative maximum value. The inductor current I_{L1} flows in the loop consisted of *S2, C1, L1, S3, Q2* and V_c. The voltage across C2 is charged to the level of V_c via *D1* and *Q2*. As shown in Figure 4(a).

(2) From t0 to t1:

S2 is turned off at t0. Inductor *L1* resonates with the input capacitor of MOSFET *Q2*, C_{g_Q2}. C_{g_Q2} will be discharged at this period. The voltage across C_{g_Q2} decreases and it will be clamped to zero by the body diode of *S4* before t1. *Q2* is turned off in this time interval. The current IL1 flows in the loop consisted of C_{g_Q2}, *C1, L1, S3* and *Q2*. Then at t1, *S3* is turned off and *S4* is turned on with zero voltage simultaneously. By controlling the turn off instant for *S2* (t0), the turn off instant of *Q2* can be controlled. As shown in Figure 4(b).

(3) From t1 to t2:

S3 is turned off and *S4* is turned on with zero voltage at t1 simultaneously. Inductor *L1* resonates with the input capacitor of MOSFET *Q1*, C_{g_Q1}. C_{g_Q1} will be charged at this period. The voltage across C_{g_Q1} increases and it will be clamped to the level of V_c by the body diode of *S1* before t2. *Q1* is turned on in this time interval. The current I_{L1} flows in the loop consisted of *S4, C1, L1,* C_{g_Q1}, *Q1* and V_{in} after *Q1* is turned on. Then at t2, *S1* is turned on with zero voltage. By controlling the turn off instant for *S3* (t1), the turn on instant for *Q1* can be controlled. As shown in Figure 4(c).

(4) From t2 to t3:

S1 and *S4* are on while *S2* and *S3* are off. *Q1* is on and *Q2* is off. The negative inductor current I_{L1} rises to zero and further increases. The value of the current I_{L1} will increase to positive maximum at t3. The current I_{L1} flows in the loop consisted of *C2, S1, L1, C1, S4,* V_{in} and *Q1*. Then at t3, *S1* is turned off with zero voltage. As shown in Figure 4(d).

(5) From t3 to t4:

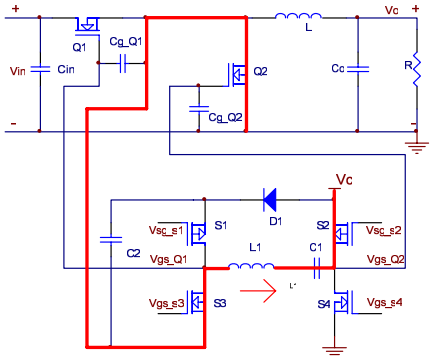
S1 is turned off at t3. Inductor *L1* resonates with capacitor C_{g_Q1}. C_{g_Q1} will be discharged at this period. The voltage across C_{g_Q1} decreases and it will be clamped to zero by the body diode of *S3* before t4. *Q1* is turned off in this time interval. The current I_{L1} flows in the loop consisted of C_{g_Q1}, *L1, C1, S4,* V_{in} and *Q1*. At t4, *S3* is turned on and *S4* is turned off with zero voltage simultaneously. By controlling the turn off instant for *S1* (t3), the turn off instant of *Q1* can be controlled. As shown in Figure 4(e).

(6) From t4 to t5:

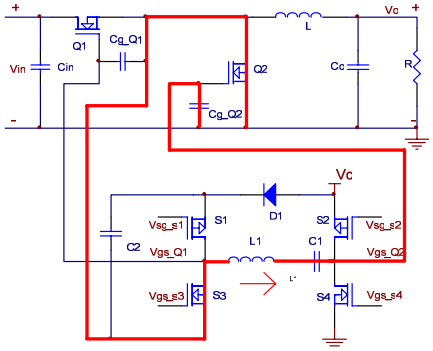
S3 is turned on and *S4* is turned off with zero voltage at t4 simultaneously. Inductor *L1* resonates with capacitor C_{g_Q2}. C_{g_Q2} will be charged at this period. The voltage across C_{g_Q2} increases and it will be clamped to the source voltage V_c by the body diode of *S2* before t5. *Q2* is turned on in this time interval. The current I_{L1} flows in the loop consisted of *S3, L1, C1,* C_{g_Q2}, and *Q2*. At t5, *S2* is turned on with zero voltage. By controlling the turn on instant for *S3* (t4), the turn on instant for *Q2* can be controlled. As shown in Figure 4(f).

(7) From t5 to t6:

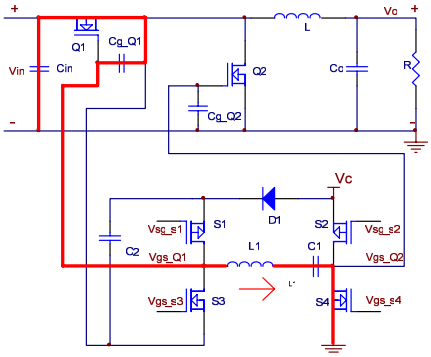
S1 and *S4* are off while *S2* and *S3* are on, while *Q1* is off and *Q2* is on. The inductor current I_{L1} decreases to zero and then it will increase in opposite direction. The value of the current I_{L1} will increase to negative maximum at t6. The current I_{L1} flows in the loop consisted of S2, *C1, L1, S3, Q2* and V_c. The next cycle will start at t6. As shown in Figure 4(a).



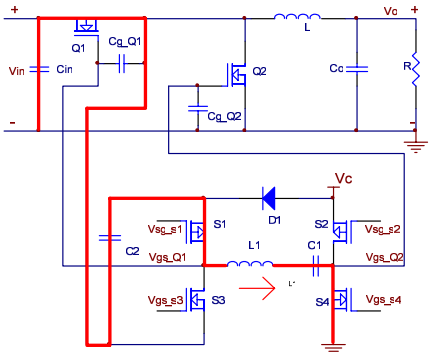
(a) Mode 1 (t0 < t and t5 < t < t6)



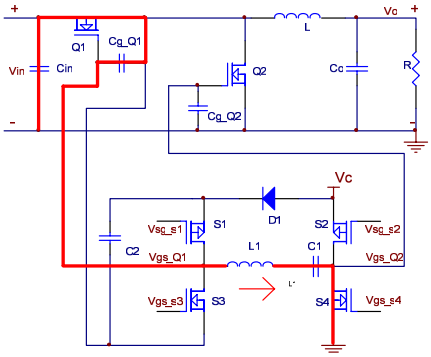
(b) Mode 2 (t0 < t < t1)



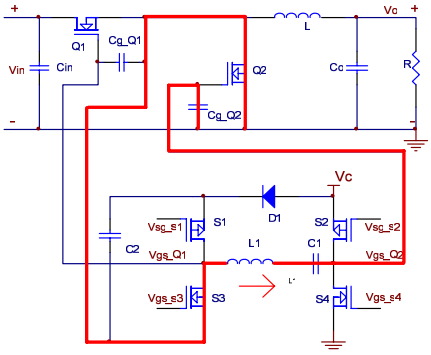
(c) Mode 3 (t1 < t < t2)



(d) Mode 4 (t2 < t < t3)



(e) Mode 5 (t3 < t < t4)



(f) Mode 6 (t4 < t < t5)

Figure 4 Equivalent circuits of 6 operation modes of the proposed resonant gate drive circuit working in complementary mode

In a synchronous buck converter shown in Figure 3, the DC voltage across capacitor C1 is given by equation (1):

$$V_{C1} = D * V_{in} + (2D - 1) * V_C \tag{1}$$

The relationship of the peak inductor current and the inductor value is given by equation (2):

$$I_{Lpeak} = \frac{(V_{in} + 2V_C) * D * (1 - D) * T_s}{2L} \tag{2}$$

Where, V_{in} is the input voltage of the converter. V_c is the gate drive voltage, which can be the input voltage of the converter. T_s is switching period. L is the resonant inductor value. D is the duty cycle of the control MOSFET.

III. ADVANTAGIES

One key point of this circuit is that during the transition when the MOSFET is turned on, its gate capacitor is charged by the peak inductor current, I_{Lpeak} and during the transition when the MOSFET is turned off, the gate capacitor is discharged by the peak inductor current as well. During charging and discharging period, the inductor current is constant. This fact brings significant advantages to the operation of synchronous Buck converter as summarized below.

(a) Smaller gate drive loss

The gate charge loss can be significantly reduced. The analysis shows that more than 50% of the gate drive loss can be recovered at 1MHz switching frequency.

(b) Reduced switching loss and body diode conduction loss

The charge current and discharge current is constant and is the peak value of the inductor current. This ensures quick discharge of the miller capacitor, which is critical to reduce the turn off loss. An additional benefit from this fact is that the dead time required to avoid cross conduction between the control FET and synchronous FET can also be reduced. Thus the diode conduction loss can be reduced.

(c) High noise immunity and alleviation of dv/dt effect

With the proposed resonant gate drive circuit, as shown in Fig. 1a, the gate of both MOSFETs are connected to either the voltage source or ground via low impedance path (S1 to S4). With the conventional gate drive scheme, the gate is connected to ground or to Vcc through external gate resistor (around 1 ohm) and driver's on-resistance (a few ohms). Therefore, the noise immunity is significantly improved and it is much less likely the synchronous FET will be turned on by dv/dt effect.

(d) Less impact of parasitic inductance

As the gate is charged / discharged by a constant current source, the impact caused by the parasitic inductance in the gate drive loop (such as PCB track, lead inside MOSFET) is much less. It is noted that in the conventional gate drive scheme, the parasitic inductance will reduce the charge and discharge current and therefore increase switching loss.

IV. LOSS ANALYSIS AND DESIGN PROCEDURE

The proposed resonant gate drive circuit can reduce gate drive loss. It can also reduce the turn-off switching loss. This section provides the loss analysis and design procedure.

(a) Gate drive loss analysis

The current used to charge and discharge the input capacitors of the power MOSFETs is the peak inductor current I_{Lpeak}, which is almost constant as the resonant transition is much shorter than the resonant period and the switching period T_s.

The inductor current waveform indicated in Figure 2 for a switching cycle can be divided into 2 pieces: t0-t3 and t3-t6. Duty cycle D equals to interval t0-t3 divided by the switching period. During interval t0-t3, the inductor current increases from negative peak current $-I_{Lpeak}$ to positive peak current I_{Lpeak}, whereas during interval t3-t6, the inductor current declines from positive peak current I_{Lpeak} to negative peak current $-I_{Lpeak}$. Therefore, the RMS value of the inductor current I_{LRMS} equals to $I_{Lpeak} / \sqrt{3}$.

The RMS currents flowing through the switches *S1-S4* can also be derived. The RMS currents flowing through switches *S1* and *S4* are the same and given by equation (3):

$$I_{S1RMS} = I_{S4RMS} = I_{Lpeak} * \sqrt{\frac{D}{3}} \tag{3}$$

Meanwhile, the RMS currents flowing through switches *S2* and *S3* are the same and given by equation (4):

$$I_{S2RMS} = I_{S3RMS} = I_{Lpeak} * \sqrt{\frac{1 - D}{3}} \tag{4}$$

The total power loss of the proposed resonant gate drive circuit is the sum of the resistive losses and gate drive losses of switches *S1-S4*, the core loss and copper loss of the resonant inductor *L1* and the resistive loss caused by the internal gate mesh resistance of the power MOSFETs. There is no switching loss or cross conduction loss as switches *S1-S4* operate in ZVS condition.

DC resistance of the inductor winding cannot be used here to directly calculate its copper loss because of the high operation frequency. Skin-effect has to be considered. The copper loss of the inductor winding is given by equation (5):

$$P_{copper} = R_{ac} * I_{LRMS}^{\ 2} \tag{5}$$

R_{ac} is the AC resistance of the inductor winding. I_{LRMS} is the RMS value of the inductor current. Core loss of the resonant inductor is another loss in this resonant gate drive circuit. The core loss P_{core} depends upon the inductor design. Core materials with high permeability such as 3F5 or PC50 should be used to reduce core loss. Air core inductor may be used when the switching frequency goes above 2 MHz. In

that case, core loss is eliminated. The total inductor loss is given in equation (6):

$$P_{ind} = P_{copper} + P_{core} \tag{6}$$

Both the charge and discharge currents flow through the internal gate mesh resistance R_G of the power MOSFET and cause resistive loss. The charge and discharge current is the peak value of the inductor current. Thus the total losses caused by the internal resistance of two power MOSFETs during turn-on and turn-off can be given in equation (7):

$$P_{RG} = 2 * R_{G1} * I_{Lpeak}^{\ 2} * t_{sw1} * f_s + 2 * R_{G2} * I_{Lpeak}^{\ 2} * t_{sw1} * f_s \tag{7}$$

Where t_{sw1} and t_{sw2} are the switching time of MOSFET *Q1* and *Q2* respectively, and R_{G1} and R_{G2} are the internal gate resistors of *Q1* and *Q2* respectively. f_s is the switching frequency. P_{RG} includes both the charging loss and discharging loss caused by the internal resistance of two power MOSFETs.

The RMS current flowing through switches *S1* and *S4* is given by equation (3). So the resistive loss caused by the on-resistor of *S1* and *S4* can be given by equation (8):

$$P_{S1,4} = 2 * R_{DS(on)} * I_{Lpeak}^{\ 2} * \frac{D}{3} \tag{8}$$

The RMS current flowing through bottom switches *S2* and *S3* is given by equation (4). So the resistive loss caused by the on-resistor of *S2* and *S3* can be given by equation (9):

$$P_{S2,3} = 2 * R_{DS(on)} * I_{Lpeak}^{\ 2} * \frac{1-D}{3} \tag{9}$$

As mentioned before, switches *S3* and *S4* are N-channel MOSFETs, whereas switches *S1* and *S2* can be either N-channel MOSFET or P-channel MOSFETs depend on design. When the same MOSFET is selected for all switches *S1-S4*, the total conduction loss caused by the switches S1-S4 is given by equation (10):

$$P_{cond} = P_{S1,4} + P_{S2,3} = 2 * R_{DS(on)} * I_{Lpeak}^{\ 2} * \frac{1}{3} \tag{10}$$

Although the total gate charges of switches *S1-S4* are very small, they will still cause some losses at high switching frequency. The operating frequency of these four switches is the same as the switching frequency f_s of the power MOSFETs. The total gate drive loss of all four switches is given by equation (11):

$$P_{Gate} = 4 * Q_{g\_s} * V_{gs\_s} * f_s \tag{11}$$

Where Q_{g_s} is the total gate charge of switch, V_{gs_s} is the drive voltage of the switch, which is usually 5V.

Therefore, the total loss of the resonant gate drive circuit can be derived by adding all above mentioned losses together and is given by equation (12):

$$P_{DRV} = P_{cond} + P_{RG} + P_{Gate} + P_{ind} \tag{12}$$

An example is taken for understanding the gate drive loss under the proposed resonant gate drive circuit. MOSFETs IRF6618 and IRF6691 are selected as control MOSFET *Q1* and synchronous MOSFET *Q2* respectively. FDN335N is selected for switches *S1-S4*, with typical $R_{DS(on)}$ = 0.07Ω and total gate charge Q_{g_s} = 3.5nC. Assume the inductor peak current is 1.2A. The switching frequency is 1 MHz. DS3316P-2.2uH is chosen as the resonant inductor. The core loss of the inductor at 1MHz is 0.147W and the estimated AC winding resistance is 0.044 Ω.

On the other side, the gate drive loss under conventional gate drive scheme can be calculated by equation (13):

$$P_{DRV} = Q_g * V_{gs} * f_s \tag{13}$$

There are lots of driver chip based on conventional gate drive scheme in the market. The loss caused by the driver chip itself is usually around 300mW [1].

In the proposed resonant gate drive circuit, it is expected that the logic circuit and level shift circuit for generating the drive signals of switches *S1-S4* will have some loss. This loss can be estimated from the datasheets of conventional driver chip operating at no load, which is less than 40mW.

Therefore, the total gate drive losses under conventional gate drive circuit and resonant gate drive circuit can be calculated and listed in Table 1. The gate drive loss saving realized by using resonant gate drive circuit is 52.7% (0.79/1.5).

Table 1 Calculated gate drive loss

	Gate charge loss	Driver chip loss	Total Drive loss
Conventional driver	1.2W	0.3W	1.5W
Resonant gate driver	0.67W	0.04W	0.71W
Loss Saving	0.53W	0.26W	0.79W

(b) Switching loss analysis

Turn-off behaviour of the driven MOSFETs under the proposed resonant gate drive circuit is much different from that of conventional voltage gate drive scheme. Switching loss can be reduced by reducing switching time and therefore, significant switching loss reduction is achieved.

Normally, $V_{gs(th)}$ of a power MOSFET is around 2V, and the plateau voltage V_p is around 3V. Under conventional gate drive scheme, assume gate drive voltage V_{gs} is 12V and the total gate resistance is around 4 - 6 Ω. Then the average charge current in turn-on transition is 1.54A, whereas the average discharge current in turn-off transition is determined

by the threshold voltage and plateau voltage and is only 0.46A [1]. It is noted that the discharge current is just one third of the charge current. Therefore, the interval associated with switching loss in turn-off transition is three times of that in turn-on transition. Furthermore, the current flowing through the MOSFET before the turn-off transition is usually much higher than that at the beginning of the on state. The switching loss is proportional to the current amplitude.

Hence, the turn-off switching loss of the MOSFET is much higher than its turn-on switching loss when conventional voltage gate drive circuit is used. The actual turn-on switching loss is hard to evaluate precisely because of the current spike at the front edge of the current waveform. It is noted that normally turn-off switching loss is 80% of the total switching loss and is 4 times of the turn-on switching loss. In other words, the total switching loss can be reduced significantly if the turn off time can be reduced. In the proposed circuit, the discharge current is the same as the charge current. Therefore the switching loss can be reduced.

There is an additional benefit for synchronous Buck converter when the proposed resonant gate drive circuit is used. The body diode loss can be reduced as the switching time is reduced. It is noted that there is no switching loss when ZVS is achieved for the power MOSFET. This is a common phenomenon in synchronous rectifier, where the conduction losses of MOSFET body diodes become significant instead. The diode conduction time is determined by the dead time of the drive signal and the switching time of the MOSFET. The dead time can be reduced as the MOSFETs can turn-off faster when resonant gate drive circuit is adopted. Therefore, the diode conduction loss can be reduced.

V. EXPERIMENTAL RESULTS

A prototype is also built to verify the feasibility and advantages of the proposed resonant gate drive circuit. As comparison, a Buck converter with conventional gate drive circuit is also built. The input voltage is 12V. The output is 1.5V/15A. The switching frequency is 1MHz. For Buck converter, the control FET is IRF7821 and the synchronous FET is FDS7088N7. The Buck inductor value is selected as 0.5uH with ripple current of 2.6A peak to peak. The only difference between the two Buck converters is the gate drive circuit.

For resonant gate drive circuit, FDN335N is selected for switches *S1 – S4*. The inductor is DS3316P-2.2uH.The peak inductor current is 1.2A.

For conventional gate drive scheme, the driver chip is TPS2832 from Texas Instrument, which uses adaptive dead-time control circuit to eliminate shoot-through currents through the control FET and SR FET during switching transition. The external gate resistor is 1 Ω. It is noted that when the external gate resistor is set to zero. The measurement result does not change.

The total power loss for two converters under different load current is measured and summarized in Table 2.

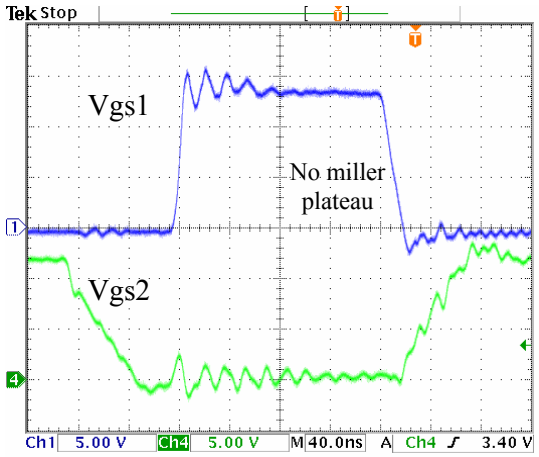
It is observed from the measurement that significant power loss reduction is achieved. At 15A output current, the power loss reduction is 2.15W, almost 10% of the output power.

A more detailed look at the measurement data shows that when the load current increases, the total power loss reduction achieved by the resonant gate drive circuit is also increased. At 5A load current, the total loss reduction is 1.03W and at 15A, the total loss reduction is increased to 2.15W. As the gate drive loss is independent of load current and the conduction loss is same for both gate drive schemes, the result shows that the switching loss is reduced by the resonant gate drive scheme. The power loss reduction due to switching loss reduction is very significant.

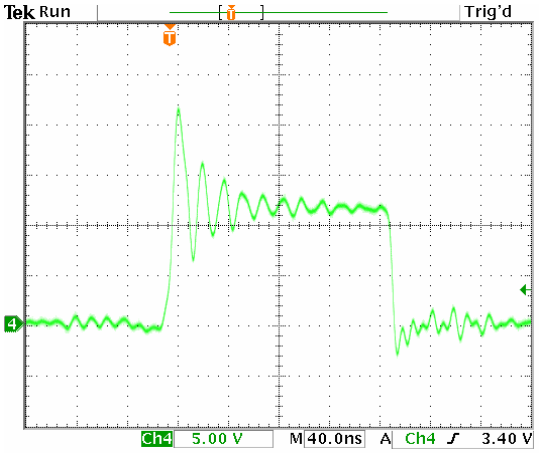
Table 2 Loss Comparison for Buck Converter, Vin = 12V, fs = 1MHz

Output	Ploss, TPS2832	Ploss, Resonant	ΔPloss	ΔPloss/Po
1.5V/5A/7.5W	3.00W	1.97W	1.03W	13.7%
1.5V/10A/15W	5.32W	3.78W	1.54W	10.3%
1.5V/15A/22.5W	9.06W	6.91W	2.15W	9.6%

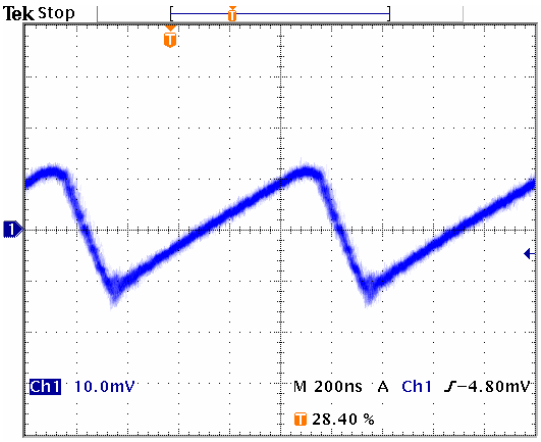
Figure 5 shows the measured waveforms under resonant gate drive circuit. As shown in Figure 5(a), the gate drive signal for Vgs1 (control FET) is very clean and smooth. No miller plateau is observed as the miller charge is removed very quickly. The rise time and fall time of Vgs1 is less than 20ns. This indicates a very fast switching time. The ringing in Vgs2 is caused by noise picked by the probe. Figure 5(b) shows the drain to source voltage of synchronous rectifier. Figure 5(c) shows the resonant inductor current waveform. The peak inductor current, which is also the charge and discharge current, is 1.2A.



(a) Top trace: Vgs1 (control FET). Bottom trace: Vgs2 (SR FET), scale: 5V/div, 40ns/div



(b) Drain to source voltage for SR FET scale: 5V/div, 40ns/div



(c) Resonant inductor current 1A/div (10mV/div), 200ns/div

Figure 5 Measured key waveforms of the proposed resonant gate drive circuit

VI. CONCLUSIONS

A new resonant gate drive circuit suitable for synchronous Buck converter is proposed in this paper. The gate drive loss can be reduced. More importantly, the switching loss can also be reduced significantly. Therefore, the overall power loss can be reduced significantly. Measurement result shows that the power loss can be reduced by almost 10% of the output power for 1.5V/15A output at switching frequency of 1MHz.

The proposed resonant gate drive circuit provides a new and very promising way to improve the performance for VRM application. Although extra components are needed to implement the resonant gate drive circuit, this cost penalty can be offset by the following factors:

At high switching frequency operation, ceramic capacitors will be able to provide adequate dynamic response and more expensive Oscon capacitor is no longer needed. In addition, Buck inductor value can also be reduced, which also reduce the cost.

If the switching frequency remains same as present application, such as around 300 KHz, the reduction of switching loss will improve the efficiency and thermal performance. Therefore, each phase can deliver more load current or the number of phases can be reduced to deliver same amount of load current.

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