A New Dual Channel Resonant Gate Drive Circuit for Synchronous Rectifiers

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***Abstract*-At high frequency applications, the gate drive loss of the power MOSFET becomes quite significant. A new dual channel low side resonant gate drive circuit is proposed in this paper. The proposed drive circuit can provide two symmetrical drive signals for driving two MOSFETs. It can recover most of the driving energy and clamp the gate and source voltage of the driven MOSFETs to either drive voltage or ground via a low impedance path. The circuit can also alleviate the dv/dt issue. The proposed circuit consists of four switches and a single winding inductor. The proposed resonant gate drive circuit can be used to drive the synchronous MOSFETs in a current doubler or full-wave rectifier. It can also be used to drive the primary MOSFETs in push-pull converters.**

I. INTRODUCTION

The development of microprocessor and other integrated circuits submits new challenges to power converter. In order to reduce the passive component size, and also to meet the stringent transient response requirement, the switching frequency of the power converter will move into the MHz range in the next few years. At high frequency application, the performance of the gate drive circuit for MOSFETs on the overall converter becomes quite significant. As the operating frequency of power converters rise, the losses associated with driving the power MOSFET rise as well, which is proportional to the switching frequency. On the other side, as power MOSFET die size is increased to improve the MOSFET on-resistance, the gate-source capacitance of the MOSFET increases in a proportional manner. Therefore, the gate drive loss becomes more significant, especially in low voltage, high current applications.

Unfortunately, the conventional gate drive scheme is a voltage source drive approach and all the drive energy is dissipated on the resistor in the charge and discharge path. Lossless gate drive circuits have already attracted much attention in recent years. Resonant gate drivers are an efficient alternative to the conventional methods to drive power MOSFETs. Many approaches have already been proposed. Most of them are designed for one MOSFET and based on L-C resonance techniques [1]-[5]. Simple DC/DC converters and transformers are adopted in some other solutions [6]-[8]. A few of drive schemes for synchronous rectifier are also proposed [9] [10]. Unfortunately, these circuits are complicated and they can only reduce the gate drive loss, which limit the potential of loss reduction.

This paper presents a new resonant gate drive circuit, which can provide two symmetrical drive signals for driving two MOSFETs. The proposed drive circuit can recover most of the driving energy. It can also reduce the switching loss significantly. The proposed resonant gate drive circuit can be used to drive the synchronous rectifier in a current doubler or full-wave rectifier. It can also be used to drive the primary MOSFETs in push-pull converters.

II. OPERATING PRINCIPLE OF THE PROPOSED RESONANT GATE DRIVE CIRCUIT

The proposed new resonant gate drive circuit is shown in Figure 1. The circuit consists of four switches *S1* – *S4*, which is inherited from dual channel conventional gate drive circuit, connecting as a bridge configuration, and an inductor, *L1*, connecting across the bridge. Capacitors, C_{g_Q1} and C_{g_Q2}, are the gate capacitors of the power MOSFETs *Q1* and *Q2* respectively. V_c is the voltage source. In order to simplify the implementation, P-channel MOSFET is used for *S1* and *S2* and N-channel MOSFET is used for *S3* and *S4*. It is noted that other implementation methods can also be used to achieve the same objective.

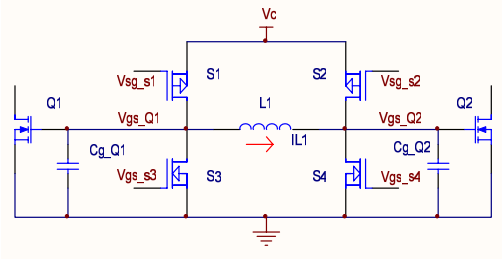

Figure 1 Proposed resonant gate drive circuit

The major objective of the resonant gate drive circuit is to charge and discharge capacitors, C_{g_Q1} and C_{g_Q2}, with minimum energy loss and as soon as possible, and to clamp the voltages across C_{g_Q1} and C_{g_Q2} to either source voltage V_c or zero via low impedance path. With this circuit, the duty cycles of the voltages across C_{g_Q1} and C_{g_Q2} are the same, which is decided by the gate drive signals for *S1* – *S4*. With different gate drive signals to *S1*, *S2*, *S3*, and *S4*, the duty cycle *D* for *Q1* and *Q2* can be changed from below 0.5, to 0.5

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and to above 0.5. The operating is a little different from each other. The operation of this circuit under D > 0.5 situation is described as following by eight operation modes shown in Figure 2. The corresponding typical waveforms are shown in Figure 3.

(1) Before t0:

S1, *S4* are on and *S2*, *S3* are off. *Q1* is on and *Q2* is off. Inductor current I_{L1} increases to maximum value at t0. As shown in Figure 2(a).

(2) From t0 to t1:

S4 is turned off at t0. Inductor *L1* resonates with the gate capacitor of MOSFET *Q2*, C_{g_Q2}. C_{g_Q2} will be charged at this period. The voltage across C_{g_Q2} increases and it will be clamped to the source voltage, V_c, by the body diode of *S2* before t1. *Q2* is turned on in this time interval. At t1, *S2* turns on with zero voltage. By controlling the turn off instant for *S4* (t0), the turn on instant of *Q2* can be controlled. As shown in Figure 2(b).

(3) From t1 to t2:

S1, *S2* are on and *S3*, *S4* are off. Both *Q1* and *Q2* are on and inductor current I_{L1} is circulating through *S1* and *S2* and remains constant in this interval. As shown in Figure 2(c).

(4) From t2 to t3:

S1 is turned off at t2 with zero voltage. Inductor *L1* resonates with the gate capacitor of MOSFET *Q1*, C_{g_Q1}. C_{g_Q1} will be discharged at this period. The voltage across C_{g_Q1} decreases and it will be clamped to zero by the body diode of *S3* before t3. *Q1* is turned off in this time interval. At t3, *S3* turns on with zero voltage. By controlling the turn off instant of *S1* (t2), the turn off instant of *Q1* can be controlled. As shown in Figure 2(d).

(5) From t3 to t4:

S2, *S3* are on and *S1*, *S4* are off. *Q1* is off and *Q2* is on. The inductor current I_{L1} decreases to zero and it will increase in opposite direction. It reaches the negative maximum at t4. As shown in Figure 2(e).

(6) From t4 to t5:

S3 is turned off at t4. Inductor *L1* resonates with capacitor C_{g_Q1}. C_{g_Q1} will be charged. The voltage across C_{g_Q1} increases and it will be clamped to the source voltage V_c by the body diode of *S1* before t5. *Q1* is turned on in this time interval. At t5, *S1* turns on with zero voltage. By controlling the turn off instant of *S3* (t4), the turn on instant of *Q1* can be controlled. As shown in Figure 2(f).

(7) From t5 to t6:

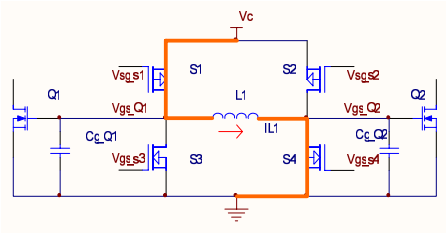
S1, *S2* are on and *S3*, *S4* are off. Both *Q1* and *Q2* are on and inductor current I_{L1} is circulating through *S1* and *S2* and remains constant in this interval. As shown in Figure 2(g).

(8) From t6 to t7:

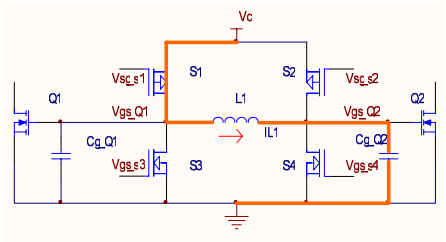
S2 is turned off at t6 with zero voltage. Inductor *L1* resonates with capacitor C_{g_Q2}. C_{g_Q2} will be discharged at this period. The voltage across C_{g_Q2} decreases and it will be clamped to zero by the body diode of *S4* before t7. *Q2* is turned off in this time interval. At t7, *S4* turns on with zero voltage. By controlling the turn off instant for *S2* (t6), the turn off instant of *Q2* can be controlled. As shown in Figure 2(h).

(9) From t7 to t8:

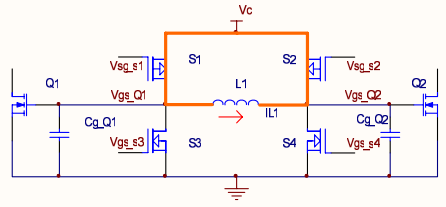
S1, *S4* are on and *S2*, *S3* are off. *Q1* is on and *Q2* is off. The negative inductor current rises through zero and then further increases. The value of the current I_{L1} will increase to positive maximum at t8. The next cycle will start at t8. As shown in Figure 2(a).



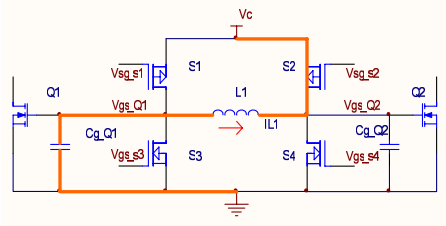
(a) Mode 1 (t < t0 and t7 < t < t8)



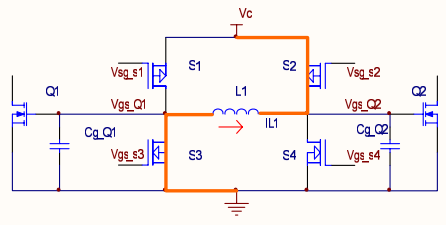
(b) Mode 2 (t0 < t < t1)



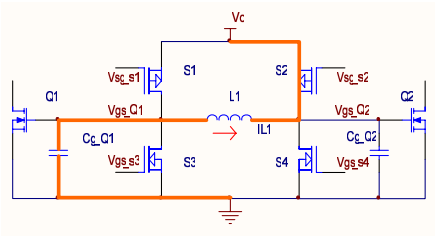
(c) Mode 3 (t1 < t < t2)



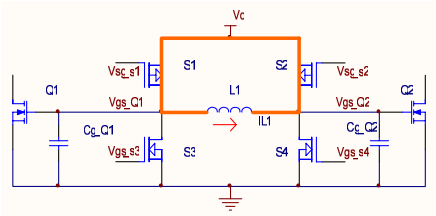
(d) Mode 4 (t2 < t <t3)



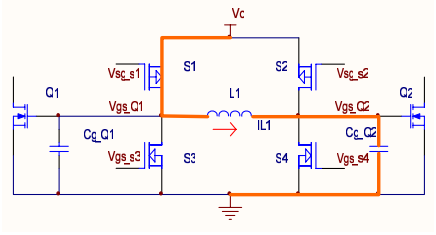
(e) Mode 5 (t3 < t < t4)



(f) Mode 6 (t4 < t < t5)



(g) Mode 7 (t5 < t < t6)



(h) Mode 8 (t6 < t < t7)

Figure 2 Equivalent circuits of 8 operation modes in dual low side symmetrical drive circuit

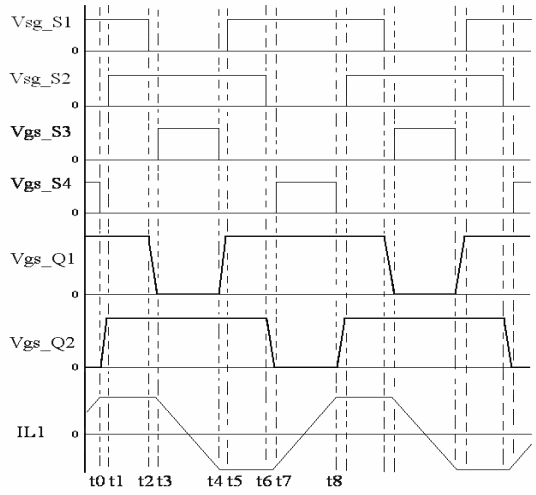


Figure 3 Typical waveforms in the proposed resonant gate drive circuit

When the duty cycle D equals 0.5, the operation is similar to that for $D > 0.5$ and is not explained here. The key difference is that there is no overlap between the drive signal of *S1* and *S2*, so *S1* and *S2* won't conduct simultaneously and there is no current cycling through them.

When the duty cycle D is less than 0.5, the operation is similar to that for $D > 0.5$ and is not explained here. The key difference is that there is a current cycling though *S3* and *S4* instead of *S1* and *S2*.

III. LOSS ANALYSIS

The current used to charge and discharge the input capacitors of the power MOSFETs is the peak inductor current I_{L1}, which is almost constant as the resonant transition is much shorter than the resonant period and the switching period T_s. Assume the power MOSFET *Q1* and *Q2* in Figure 1 are identical and their desired switching time is t_{sw}, the required peak inductor current, which is also the charge and discharge current can be given by equation (1):

$$I_{Lpeak} = \frac{Q_g}{t_{sw}} \tag{1}$$

Where, Q_g is the total gate charge of each power MOSFET, t_{sw} is the desired switching time of the MOSFET.

In general consideration, the inductor current waveform indicated in Figure 3 for a switching cycle can be divided into four pieces: t0-t3, t3-t4, t4-t7 and t7-t8. The time of intervals t0-t3 and t4-t7 are the same, and intervals t3-t4 and t7-t8 are the same. The inductor current is redrawn in Figure 4. The currents through switches *S1*-*S4* are also shown in Figure 4. Duty cycle of the power MOSFET, *D*, equals to the turn-on time, interval t1-t6, divided by the switching period T_s, which equals to interval t0-t8. (Assume $D > 0.5$)

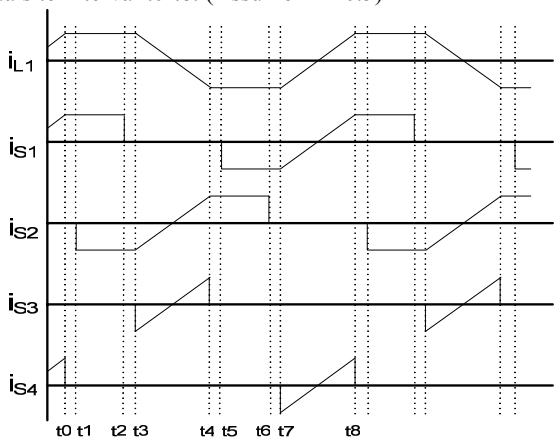


Figure 4 Current through inductor and switches S1-S4 at $D > 0.5$

During intervals t0-t3 and t4-t7, the inductor current keeps constant and its absolute value equals to I_{Lpeak}. During interval t3-t4, the inductor current decline from positive peak current I_{Lpeak} to negative peak current - I_{Lpeak}, whereas during interval t7-t8, the inductor current increases from negative peak current - I_{Lpeak} to positive peak current I_{Lpeak}. Therefore, the RMS value of the inductor current can be given in equation (2):

$$I_{LRMS} = \sqrt{2 * \frac{2D-1}{2} * I_{Lpeak}^{\ 2} + 2(1-D) * \frac{I_{Lpeak}^{\ 2}}{3}} = I_{Lpeak} * \sqrt{\frac{4D-1}{3}} \tag{2}$$

At D = 0.5, the inductor current becomes triangular and I_{LRMS} equals to $I_{Lpeak}/\sqrt{3}$.

The RMS currents flowing through the switches *S1-S4* can also be derived. The RMS currents flowing through switches *S1* and *S2* are the same and given by equation (3):

$$I_{S1RMS} = I_{S2RMS} = \sqrt{2 * \frac{2D-1}{2} * I_{Lpeak}{}^2 + (1-D) * \frac{I_{Lpeak}{}^2}{3}} = I_{Lpeak} * \sqrt{\frac{5D-2}{3}} \tag{3}$$

At D = 0.5, the RMS current flowing through switches *S1* and *S2* equals to $I_{Lpeak}/\sqrt{6}$. On the other side, the RMS current equals to I_{Lpeak} when D = 1 and the inductor current flowing through switches *S1* and *S2* during whole period, though this is impossible in practice.

Meanwhile, the RMS currents flowing through switches *S3* and *S4* are the same and given by equation (4):

$$I_{S3RMS} = I_{S4RMS} = I_{Lpeak} * \sqrt{\frac{1-D}{3}} \tag{4}$$

At D = 0.5, the RMS current equals to $I_{Lpeak}/\sqrt{6}$. On the other side, the RMS current is zero when duty cycle D = 1, though this is impossible in practice.

The total power loss of the proposed resonant gate drive circuit is the sum of the resistive losses and gate drive losses of switches *S1-S4*, the core loss and copper loss of the resonant inductor and the resistive loss caused by the internal gate mesh resistance of the power MOSFETs. There is no switching loss or cross conduction loss as switches *S1-S4* operate in ZVS condition.

Resistive losses are the major loss in this resonant gate drive circuit which is caused by $R_{DS(on)}$ of switches *S1-S4*, resonant inductor and internal gate resistance of the power MOSFET.

DC resistance of the inductor winding cannot be used here to directly calculate its copper loss because of the high operation frequency. Skin-effect has to be considered. The copper loss of the inductor winding is given by equation (5):

$$P_{copper} = R_{ac} * I_{LRMS}{}^2 \tag{5}$$

R_{ac} is the AC resistance of the inductor winding. I_{LRMS} is the RMS value of the inductor current which is given in equation (2). Core loss of the resonant inductor is another possible loss in this resonant gate drive circuit. The core loss P_{core} depends upon the inductor design. Core materials with high permeability such as 3F5 or PC50 should be used to reduce core loss. Air core inductor may be used when the switching frequency goes above 2 MHz. In that case, core loss is eliminated. The total inductor loss is given in equation (6):

$$P_{ind} = P_{copper} + P_{core} \tag{6}$$

Both the charge and discharge currents flow through the internal gate mesh resistance R_G of the power MOSFET and cause resistive loss. The charge and discharge current is the peak value of the inductor current. Thus the total losses caused by the internal resistance of two power MOSFETs during turn-on and turn-off can be given in equation (7):

$$P_{RG} = 2 * 2 * R_G * I_{Lpeak}{}^2 * t_{sw} * f_s \tag{7}$$

Where t_{sw} is the switching time and f_s is the switching frequency. P_{RG} includes both the charging loss and discharging loss caused by the internal resistance of two power MOSFETs.

The RMS current flowing through top two switches *S1* and *S2* is given by equation (3). So the resistive loss caused by the on-resistor of *S1* and *S2* can be given by equation (8):

$$P_{top} = 2 * R_{DS(on)} * I_{Lpeak}{}^2 * \frac{5D-2}{3} \tag{8}$$

The RMS current flowing through bottom switches *S3* and *S4* is given by equation (4). So the resistive loss caused by the on-resistor of *S3* and *S4* can be given by equation (9):

$$P_{bott} = 2 * R_{DS(on)} * I_{Lpeak}{}^2 * \frac{1-D}{3} \tag{9}$$

As mentioned before, switches *S3* and *S4* are N-channel MOSFETs, whereas switches *S1* and *S2* can be either N-channel MOSFET or P-channel MOSFETs depend on design. When the same MOSFET is selected for all switches *S1-S4*, the total conduction loss caused by the switches S1-S4 is given by equation (10):

$$P_{cond} = P_{top} + P_{bott} = 2 * R_{DS(on)} * I_{Lpeak}{}^2 * \frac{4D-1}{3} \tag{10}$$

Although the total gate charges of switches *S1-S4* are very small, they may still cause some losses at high switching frequency. The operating frequency of these four switches is the same as the switching frequency f_s of the power MOSFETs. The total gate drive loss of all four switches is given by equation (11):

$$P_{Gate} = 4 * Q_{g\_s} * V_{gs\_s} * f_s \tag{11}$$

Where Q_{g_s} is the total gate charge of switch, V_{gs_s} is the drive voltage of the switch, which is usually 5V.

Therefore, the total loss of the resonant gate drive circuit can be derived by adding all above mentioned losses together and is given by equation (12):

$$P_{DRV} = P_{cond} + P_{RG} + P_{Gate} + P_{ind} \tag{12}$$

The total conduction loss of switches S1-S4 will be different from each other when the duty cycle D > 0.5 and D

< 0.5. Therefore the total driving loss may be also a little different.

An example is taken for understanding the gate drive loss under the proposed resonant gate drive circuit. Two IRF6618 are selected as power MOSFET, with total gate charge Q_g = 93nC when V_{gs} = V_{ds} = 12V. Its internal gate resistor R_G is 1Ω. FDN335N is selected for switches S1-S4, with typical $R_{DS(on)}$ = 0.07Ω and total gate charge Q_{g_s} = 3.5nC. Assume the inductor peak current is 1.2A. The switching frequency is 1 MHz. DS3316P-2.2uH is chosen as the resonant inductor. The core loss of the inductor at 1MHz is 0.147W and the estimated AC winding resistance is 0.044 Ω. The loss breakdown is calculated and shown in Figure 5.

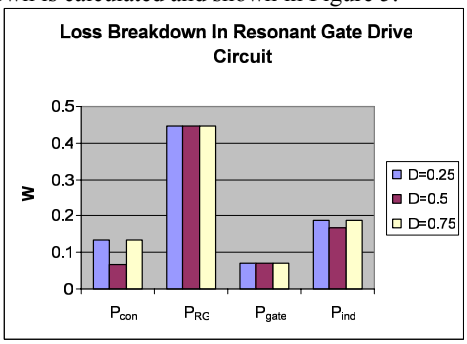


Figure 5 Loss breakdown in resonant gate drive circuit

IV. Advantages

This section analyzes the advantages of the proposed resonant gate drive circuit.

A. Gate drive loss saving

The same example is taken for comparing the gate drive loss under the proposed resonant gate drive circuit and conventional gate drive scheme. The switching frequency is 1 MHz and the duty cycle D = 0.5. The gate drive loss of resonant gate drive circuit can be calculated by using equation (12).

On the other side, the gate drive loss under conventional gate drive scheme can be calculated by equation (13):

$$P_{DRV} = Q_g * V_{gs} * f_s \tag{13}$$

There are lots of driver chip based on conventional gate drive scheme in the market. The loss of the driver chip itself is usually around 300mW [11].

In the proposed resonant gate drive circuit, it is expected that the logic circuit and level shift circuit for generating the drive signals of switches S1-S4 will cause some loss. Referring to datasheets of conventional driver chip, this loss should be less than 40mW, which is much smaller than 300mW as there is neither cross conduction loss nor switching loss in resonant gate drive circuit.

Therefore, the total gate drive losses under conventional gate drive circuit and resonant gate drive circuit can be calculated and listed in Table 1. The gate drive loss saving realized by using resonant gate drive circuit is 68.7% (1.74/2.532).

Table 1 Calculated gate drive loss

	Gate charge loss	*Driver chip loss*	*Total Drive loss*
Conventional driver	2.232W	0.3W	2.532W
Resonant gate driver	0.752W	0.04W	0.792W
Loss Saving	1.48W	0.26W	1.74W

B. Switching loss and body diode conduction loss saving

One significant feature of the proposed resonant gate drive circuit is that the charge and discharge current is high and at constant level. Therefore, the proposed resonant gate drive circuit can also reduce the switching loss as the turn on time and turn off time can be reduced. Under conventional gate drive circuit, the discharge current at and below miller plateau is much smaller than the peak discharge current, and therefore, the turn off time is longer than turn on time as it is reverse proportional to the discharge current, which causes large turn off loss. With resonant gate drive circuit, the discharge current is almost constant during the whole switching transition, and the turn off time is much shorter and the turn-off switching loss is lower.

C. High noise immunity and alleviation of dv/dt effect

With the new resonant gate drive circuit, the gate of the power MOSFET is connected to either source or ground via low impedance path, rather than through the external gate resistor and driver's on-resistance (a few ohms) in conventional gate drive scheme. Therefore, the noise immunity is significantly improved and it is much less likely the synchronous FET will be turned on by dv/dt effect.

D. Less impact of parasitic inductance

As the gate is charged/discharged by a constant current source, the negative impact by the parasitic inductance in the gate drive loop (such as PCB track, lead inside the MOSFET) can also be significantly reduced.

V. Applications

The proposed resonant gate drive circuit can be in wide range of switching power converters. Figure 6 shows the proposed resonant gate drive circuit is used to drive the synchronous rectifiers in a current doubler circuit. In this application, the duty cycles for *Q1* and *Q2* are the same and larger than 50%. With the resonant gate drive circuit, most of gate drive energy can be recovered. In addition, the turn on and turn off time of *Q1* and *Q2* can also be reduced, which will help reduce their body diode conduction loss.

Figure 7 shows current fed push-pull converter with resonant gate drive circuit to drive the primary side MOSFET, *Q1* and *Q2*. In this converter, the duty cycle for *Q1* and *Q2* is same and larger than 50%.

The proposed resonant gate drive circuit can also be used for power converters when the duty cycle is less than 0.5. Figure 8 shows voltage fed push-pull converter with resonant gate drive circuit. In this converter, the duty cycle for *Q1* and *Q2* is the same and less than 0.5.

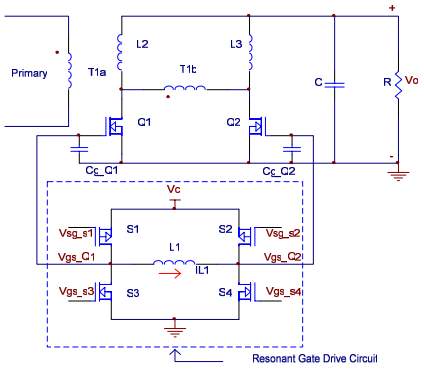


Figure 6 Current doubler with resonant gate drive circuit

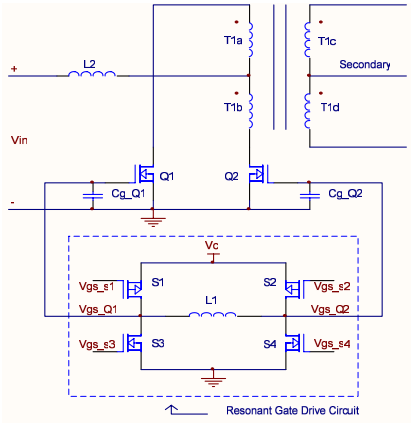


Figure 7 Current fed push-pull converter with resonant gate drive circuit

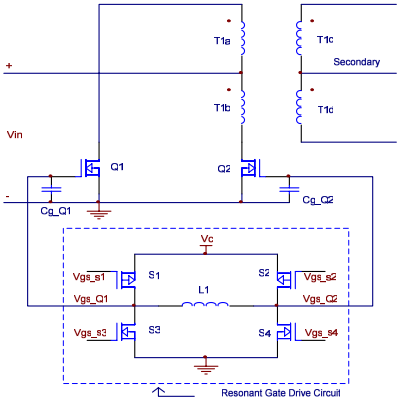
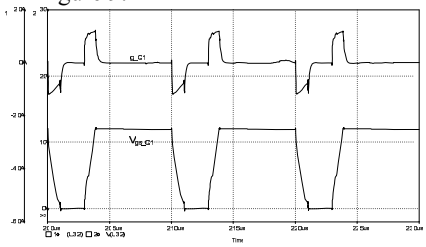


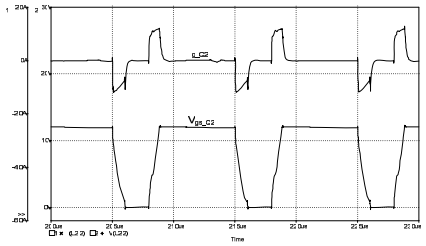
Figure 8 Voltage fed push-pull converter with resonant gate drive circuit

VI. VERIFICATION

The proposed resonant gate drive circuit was simulated by Pspice. The parameters listed above for the calculation are used for the simulation. Simulated gate drive voltage and charge/discharge waveforms at duty cycle D = 0.7 condition are shown in Figure 9.



(a) Gate drive voltage and charge / discharge current of MOSFET Q1



(b) Gate drive voltage and charge / discharge current of MOSFET Q2

Figure 9 Simulated key waveforms of the proposed resonant gate drive circuit

Two Boost converters are built. The only difference is that one uses conventional drive chip UCC27323 from Texas Instrument and the other uses resonant gate drive circuit. IRF6618 is used as the Boost MOSFET. Schottky diode 10TQ40 is used as the diode. The inductor value is 2uH. The switching frequency is 1MHz for both cases. The duty cycle is 50% and the output voltage is regulated at 11.35V by slightly adjusting the input voltage. The input voltage is around 5.7V for all the test cases. In the test setup, the gate drive circuit is powered from one power supply (with Vcc of 12V) and the Boost converter is powered from another power supply. Therefore, the gate drive loss can be separated from the power circuit loss.

The circuit diagram of the prototype is shown in Figure 10. PWM generator, logic circuit and level shift circuit are designed for generating drive signals of switches S1-S4.

The measured gate drive loss under conventional drive scheme is 2.61W at 1MHz operation. The gate drive loss for proposed resonant gate drive scheme is only 0.864W. The loss reduction is 1.746W, or 67% of the conventional gate drive loss. Figure 11 shows the measured key waveforms of the prototype.

In order to demonstrate that the resonant gate drive circuit can also reduce the switching loss, the total power train loss of the Boost converter only (excluding gate drive loss) is measured. For conventional gate drive scheme, the loss is measured under four conditions, with gate resistor of 2.5Ω and 1Ω, as well as with load current of 0.4A and 0.8A.

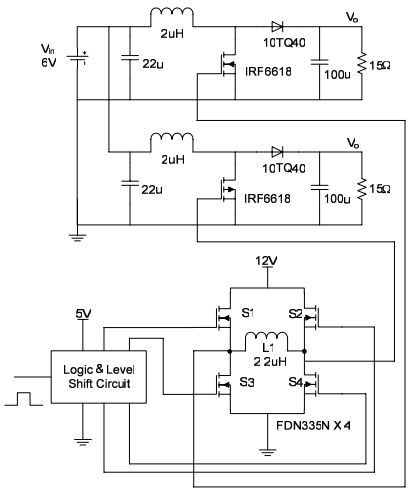
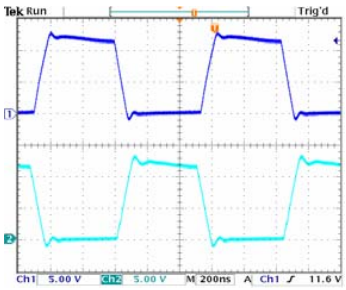
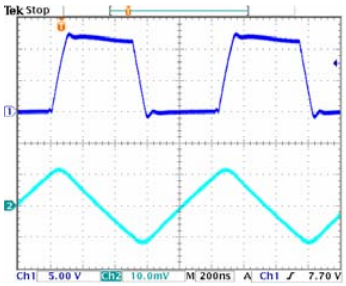


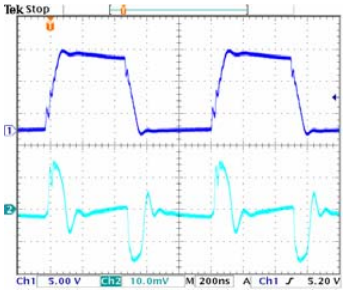
Figure 10 Circuit diagram of the prototype.



(a) Output gate drive signals of the resonant gate drive circuit (5V/div, 200ns/div)



(b) Gate drive voltage and resonant inductor current (1A/div, 200ns/div) top trace: Vgs_Q1, bottom trace: IL1



(c) Gate drive voltage and charge / discharge current (1A/div, 200ns/div) top trace: Vgs_Q1, bottom trace: Ig_Q1

Figure 11 Measured key waveforms of the proposed resonant gate drive circuit

Table 2 Switching Loss Comparison, V_c = 12V, f_s = 1MHz

Load Current	Conventional Driver		Resonant Driver	Loss Saving
	Rg_ext	P_loss	P_loss	
0.4 A	2.5 Ω	2.07 W	1.92 W	0.15 W
0.8 A	2.5 Ω	2.78 W	2.32 W	0.46 W
0.4 A	1 Ω	1.98 W	1.92 W	0.06 W
0.8 A	1 Ω	2.50 W	2.32 W	0.18 W

It is noted that with larger gate resistor (2.5Ω), the switching loss is higher and the power loss reduction by the resonant gate drive circuit is also larger (0.46W for 2.5Ω versus 0.18W for 1Ω). When load current is increased, the turn on and turn off loss will also be increased. The loss saving is also increased (0.06W at 0.4A versus 0.18W at 0.8A). It is expected that when the load current is further increased, the loss saving will be more significant.

VII. CONCLUSIONS

A new resonant gate drive circuit was proposed in this paper. The proposed drive circuit can provide two symmetrical drive signals for driving two MOSFETs. It can charge and discharge the MOSFET gate at high current level and clamp the drive voltage to either source voltage level or zero. The proposed circuit can recover most of the gate drive energy. It can also reduce the switching loss. Operation principle and loss analysis were provided. Simulation and experimental results and key waveforms are provided as well. The measured gate drive loss can be reduced by 67% as compared with the conventional gate drive approach..

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