

# A new resonant gate drive circuit utilizing leakage inductance of transformer

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**Abstract** – This paper presents a new resonant gate drive circuit that utilizes transformer leakage inductance as resonant component. The new gate driver circuit can drive a pair of MOSFETs, which can be used in both with same reference and different reference circuits such as mosfets in buck, bridge converters. Pulse controlled resonance is used to reduce the conduction loss of resonant circuit. Also it provides fast transition, thus the limitation on the duty cycle is minimized. In the paper, the theoretical analysis and simulation waveforms are provided. A prototype board is built and experimental results are also given.

## I. INTRODUCTION

With the development of computing and telecom technologies in recent years, high power density is required in switching power supply design. It has been a trend that switching frequency is moving up to above Megahertz region. Along with benefits from higher operating switching frequency in power supply, such as compact size and faster loop respond, it also brings several drawbacks. Increasing gate drive loss is one of them since it is frequency dependant. A conventional gate driver circuit shown in Fig. 1 is widely used in current power converters, including a totem-pole pair of driving mosfets, Q1 and Q2, and optional resistor, R, that is omitted in some applications between the driving mosfets and Power MOSFET, M. Triggered by PWM signal, driving mosfets, Q1 and Q2 are switched to provide the paths to charge and discharge the effective capacitance,  $C_g$  of Power MOSFET. The total gate capacitive loss can be defined as:

$$P_g = C_g \cdot (V_{CC})^2 \cdot f_s \quad (1)$$

Where  $C_g$  is effective capacitance of power MOSFET,  $f_s$  is the switching frequency.  $V_{cc}$  is the voltage of power source.

Equation (1) shows that total charge stored in effective capacitance is proportional to the switching frequency and is completely dissipated by the gate driver. With higher frequency application, it may cause gate driver itself destroyed by overheat. Also, the gate loss takes a considerable share in total power dissipation. In some case, gate loss is compatible to the conduction loss [1]. Efficiency of converters is degraded significantly. Moreover, the conventional gate driver cannot meet the requirement of switch speed in high frequency application. Fast switching transition is crucial for performance of power converters, especially for low voltage, high current output converters. It can reduce switching loss and conduction loss as well. However, the conventional gate driver operation is based on R-C charge and discharge. Turn-off transition takes quite longer time as the voltage on gate capacitance is discharged down and discharging current becomes much smaller than its

peak value. Consequently, longer turn-off transition occurs, which is not desirable to reduce the switching loss and conduction loss. In order to increase the speed of switching transition paralleled gate drivers are employed in some cases. But this results in increasing component cost.

The issues of the conventional gate driver are posing to the power designers and researches. Many attempts have been made to recover gate loss energy [1]-[10] since early the 1990s. But most efforts only focused on single circuit to drive single MOSFET.

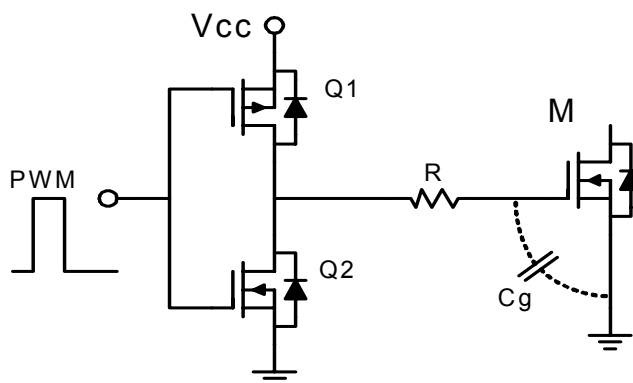


Fig. 1 Conventional gate driver

In this paper, a new resonant gate drive circuit is proposed and its operating principle is described in section II. Section III covers the loss analysis. Design guideline is also introduced. Simulation and experimental results are given in section IV. Finally, conclusion is drawn in section V.

## II. PROPOSED RESONANT GATE DRIVE CIRCUIT

Fig. 2 shows the proposed resonant gate drive circuit. It consists of 6 driving mosfets, S1-S6, two diodes, D1-D2 and a small transformer, TX. Llk represents the transformer leakage inductance that acts as resonant inductance during the operating. M1 and M2 are power MOSFETs that are driven by resonant gate drive circuit.  $C_g$  represents effective capacitance of power MOSFETs. Complementary P-channel and N-channel mosfets are used for Q1, Q2 and Q3, Q4. Turn's ratio of primary and secondary windings of transformer is 1:1. The grounds for primary and secondary circuits can be isolated or arranged as common ground, where the diagram shows as common ground. Fig. 3 shows the key operating waveforms. Fig. 4 illustrates the circuit operation in each stage.

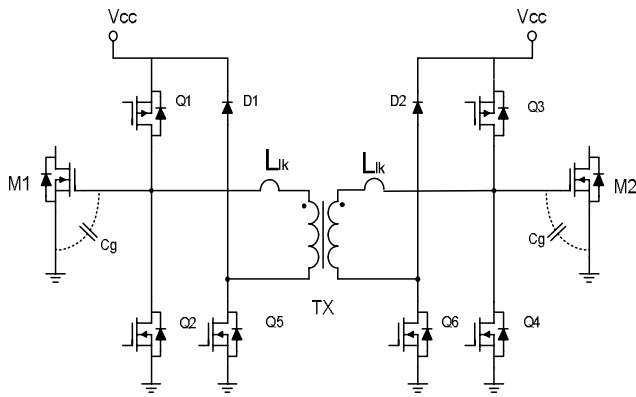


Fig. 2 Proposed resonant gate drive circuit

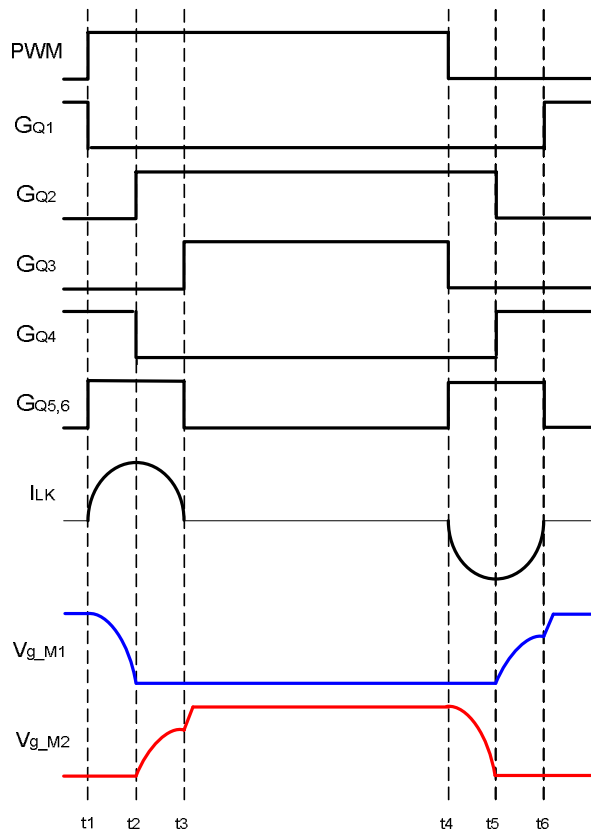


Fig. 3 Operating waveforms

Assume initially, before  $t_1$ , Q1 and Q4 stay on. Power MOSFET M1 is on, whereas M2 is off. Q2, Q3, Q5 and Q6 are off.

At  $t_1$ , the signal of turning off M1 and turning M2 arrives. Q1 is turned off. Simultaneously, Q5 and Q6 are on. Thus the secondary winding of transformer is short-circuited, the secondary leakage inductance is connected with primary leakage inductance in series, combining total inductance that resonates and discharges effective gate capacitance,  $C_g$  of M1. As long as the voltage on  $C_g$  is discharged below threshold, M1 is turned off and M2 can be started to turn on. Voltage on  $C_g$  of M1 continues to be discharged to zero, body diode of Q2 then conducts the current and Q2 can be turned on at ZVS. During this transition, the energy stored in

gate capacitance is transferred to leakage inductance of transformer.

At  $t_2$ , Q2 is turned on at ZVS and Q4 is turned off. The transformer is now short-circuited in primary winding. Combining total inductance of primary and secondary leakage inductance then resonates with effective gate capacitance,  $C_g$  of M2. The energy stored in leakage inductance in last period delivers to  $C_g$  of M2 and voltage on  $C_g$  of M2 is charged up. At the moment that resonant current reaches zero, voltage on  $C_g$  of M2 is charged to a certain value that is less than  $V_{cc}$  because of conduction loss of resonant gate drive circuit. Mosfets Q5 and Q6 are now required to turn off otherwise the resonance continues and  $C_g$  of M2 is discharged. Also Q3 should be turned on at the moment to charge the deficit voltage of  $C_g$  from  $V_{cc}$  voltage.

At  $t_3$ , resonant current reaches zero, mosfets Q5 and Q6 can be turned off at ZCS. Q3 is turned on. Gate voltage of M2 is charged to  $V_{cc}$  voltage. D2 starts to conduct the resonant current as Q5 and Q6 are turned off. The rest of energy goes through D2 and sends back to power source.

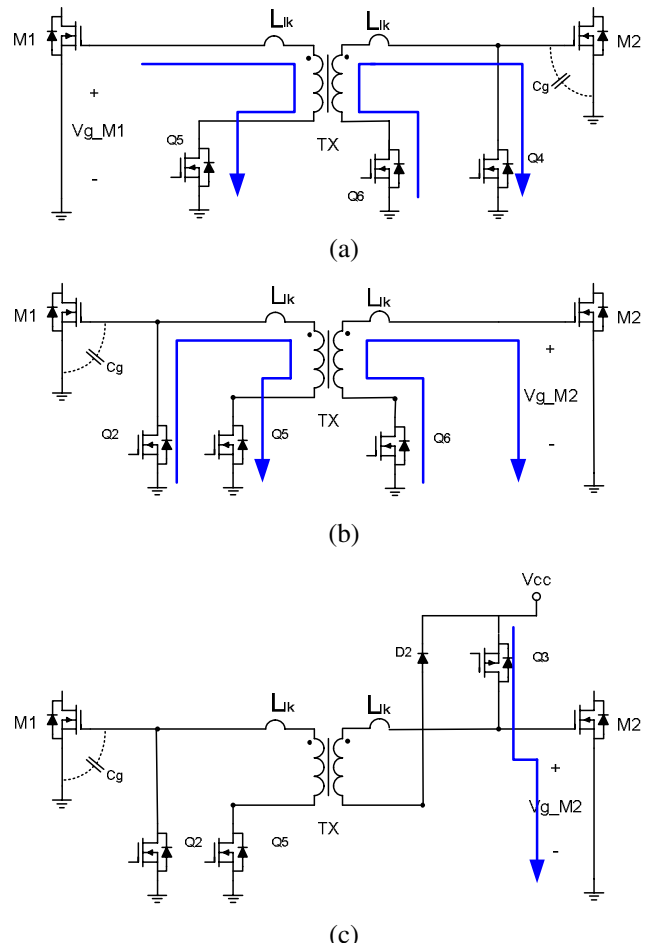


Fig. 4 Operation stages: (a) M1 turning off ( $t_1 \sim t_2$ ), (b) M2 turning on ( $t_2 \sim t_3$ ), (c) M1 turned off and M2 turned on (after  $t_3$ ).

Operating principle in the other half switching period (from  $t_4$  to  $t_6$ ) works the same as from  $t_1$  to  $t_3$  except that the direction is reversed.

From analysis above, it can be observed that the effective capacitances of power MOSFETs are charged and discharged through combined leakage inductance of transformer to recover gate charge energy. Pulse controlled resonance is utilized to minimize the conduction loss of driving circuit. Since resonance of leakage inductance and effective capacitance of MOSFET provides fast transition, it can speed up the switching transition and reduce switching loss. Also the limitation on duty cycle can be minimized. Furthermore, the fast transition time results in low voltage-second applied to transformer, therefore the transformer size can be designed very small. Because of implement with transformer, there is possibility to drive MOSFETs whose references are at different voltage potential, which is suitable to buck or bridge type converters.

### III. ANALYSIS AND DESIGN GUIDELINE

The total losses of proposed resonant gate drive circuit are distributed to conduction loss, driving loss of Q1-Q6 and transformer core loss. That is:

$$P_{gr} = P_{rms} + P_{drive} + P_{core} \quad (2)$$

Among the total losses, conduction loss,  $P_{rms}$  is the major loss. As stated in section II, a sine shaped current flows through total resistance and equivalent gate capacitance is charged and discharged. The equivalent circuit can be shown in Fig. 5 as below.

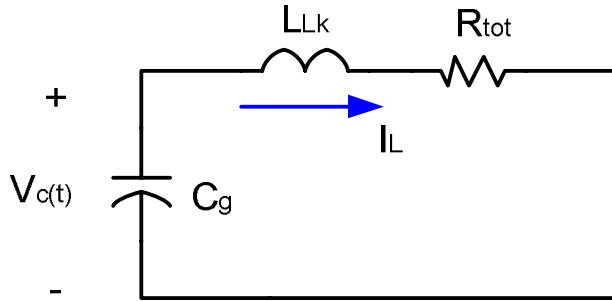


Fig. 5 Resonance equivalent circuit

In the equivalent circuit, the  $R_{tot}$  is the total resistance through resonant path, which includes  $R_{ds,on}$  of driving mosfets, winding resistance of transformer and gate resistance of power MOSFET,  $R_g$ .  $L_{Lk}$  is total leakage inductance of transformer.

The resonant current and gate capacitance voltage can be derived as (3) and (4) respectively.

$$I_L(t) = I_{PK} e^{-\alpha t} \sin(\omega_d t) \quad (3)$$

$$V_c(t) = V_{cc} \cdot (1 - K e^{-\alpha t} \cos(\omega_d t)) \quad (4)$$

Where  $\alpha = \frac{R_{tot}}{2L_{LK}}$ ,

$$\omega_d = \sqrt{\omega_o^2 - \alpha^2}, \quad \omega_o = \frac{1}{\sqrt{L_{LK} C_g}}$$

$$K = \frac{1}{\sqrt{1 - \xi^2}}, \quad \xi = \frac{R_{tot}}{2} \cdot \sqrt{\frac{C_g}{L_{LK}}}$$

$$I_{PK} = \frac{V_{cc}}{\sqrt{\frac{L_{LK}}{C_g} - \left(\frac{R_{tot}}{2}\right)^2}} \quad (5)$$

The power dissipation on total resistances can be calculated in (6)

$$P_{rms} = \int i_L(t)^2 \cdot R_{tot} \cdot dt \quad (6)$$

In the total conduction losses,  $R_g$  loss is main contributor. At range of 0.5-2  $\Omega$  for standard gate resistance of power MOSFET, even the MOSFETs transition period is normally short, the loss on internal gate resistance of power MOSFETs still takes large share of conduction loss, which gives a significant impact on the efficiency of resonant gate driver. Fig. 6 shows the calculation of total resistance's impact on loss saving of resonant gate driver.

Since the total gate charge of driving switches is small, driving losses just occupy small part of total loss. Besides, the driving mosfets can achieve ZVS or ZCS, switching loss of those driving mosfets can be neglected. Since resonant transition takes very short time, the voltage-second on transformer is quite small. With optimal turns of transformer, the core loss of transformer can be minimized.

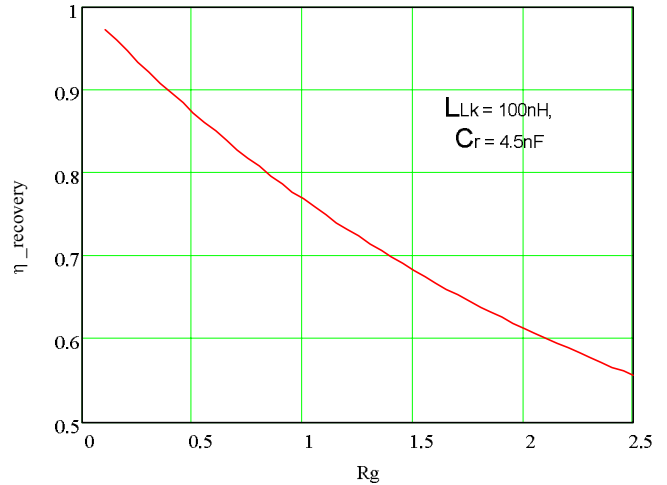


Fig. 6 Calculated total resistance impact on loss saving

Resonant gate driver is designed not only to recover much of gate energy to improve the driving efficiency, but also to realize the faster switching transition as well. Faster switching transition will reduce switching loss. In this proposed resonant gate drive circuit, the input capacitance of power MOSFETs,  $C_g$  is charged and discharged through the leakage inductance of transformer, shown in Fig. 3, from  $t_1$  to  $t_3$ . MOSFETs switching transition takes place during L-C resonance. It can provide much faster driving speed comparing with conventional driver with appropriate circuit parameter. It can overcome the drawback of slow turn-off of conventional driver. However, faster driving speed requires higher driving current that may increase conduction loss dramatically because of power dissipation on the internal

resistance of power MOSFET,  $R_g$ . Therefore the inductance of resonant inductor is another main parameter to take account into. Fig. 7 shows calculated loss recovery curve with different total resonant inductance. To design this resonant gate driver, the driving speed and driving current are the main parameters to be determined. As discussion above, the trade-off between driving speed and driving peak current need to be considered. The peak driving current is already given in (5) and the transition time ( $t_1$  to  $t_3$ ) is simply to get from (7):

$$T_t = \sqrt{L_{LK} \cdot C_g} \quad (7)$$

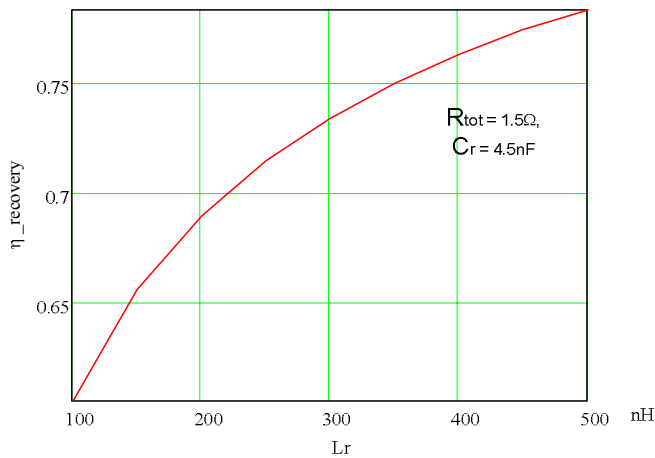


Fig. 7 Calculated loss saving with various resonant inductance

#### IV. SIMULATION AND EXPERIMENTAL RESULTS

Computer simulation has been done to verify the proposed resonant gate driver circuit. Fig. 8 gives logic circuit block used in simulation and experiment. Fig. 9 and Fig. 10 show the simulation result at switching frequency of 500 KHz and 1MHz respectively. Simulation condition is listed as following:

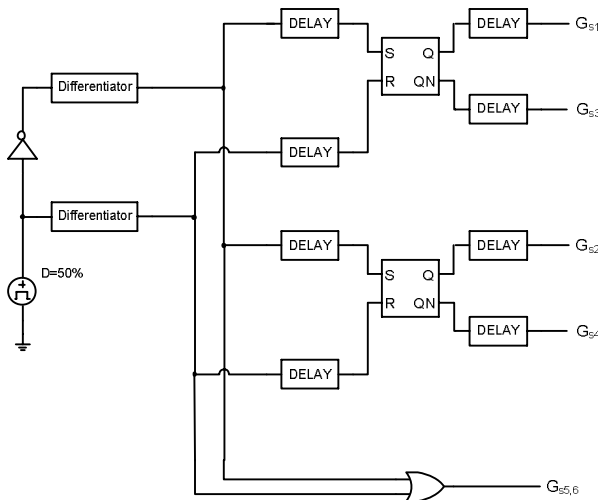


Fig. 8 Logic control block for resonant gate driver

Source voltage is 5V. Switching frequencies are set at 500KHz and 1MHz and corresponding total leakage

inductances of transformer are 200nH and 180nH respectively. 6.6nF capacitor is used to simulate equivalent gate capacitance of MOSFET. A 0.5Ω resistance is connected in series with gate capacitor to simulate the internal gate resistance of MOSFET.

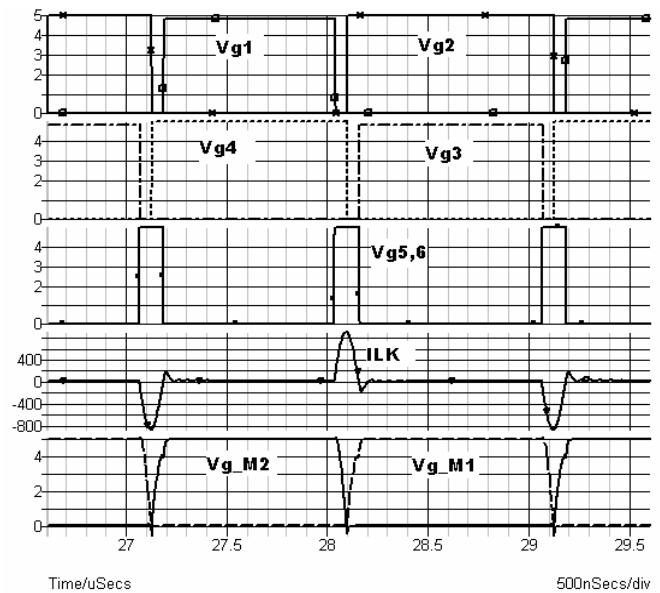


Fig. 9 Simulation results (fs = 500KHz)

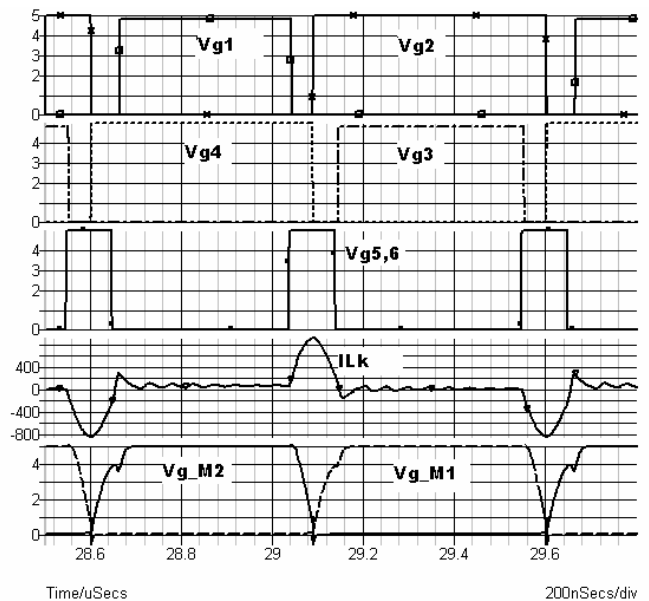


Fig. 10 Simulation results (fs = 1MHz)

A prototype was built. The voltage of power source is 5V and switching frequency is set at 500KHz. The logic circuits are implemented by discrete gate components. A RM4 core is used for driving transformer where the leakage is designed about 100nH for each winding. Mosfets with small total gate charge are chosen for S1 to S6, where FDN361AN from Fairchild is selected for S2, S4, S5 and S6, FDN352AP is selected for S1 and S3. ZHCS400 from Zetex is for D1 and D2.

Two paralleled mosfets on each side are driven by resonant gate driver circuit. FDS6680 is selected as Power

MOSFET. Fig. 11 and Fig. 12 show the measured waveforms. Fig. 11 gives driving fet gate signal and gate voltage waveforms of power MOSFETs. Fig. 12 shows zoom-in picture of detail gate voltage transition, where one side MOSFET gate energy is dumped out into the other side's gate of MOSFET. It is noticed that Vg1 and Vg3 signal is intentional to apply with delay so that the peak voltage can be observed. The energy transfer efficiency is about  $V_{peak}^2/V_{cc}^2$ , which is 69.9%. From actual measurement, the circuit loss saving is 52.9%, where total gate loss is 172mW and circuit loss is 81mW. It is expected that when logic circuit is implemented with an ASIC, the circuit loss can be significantly reduced.

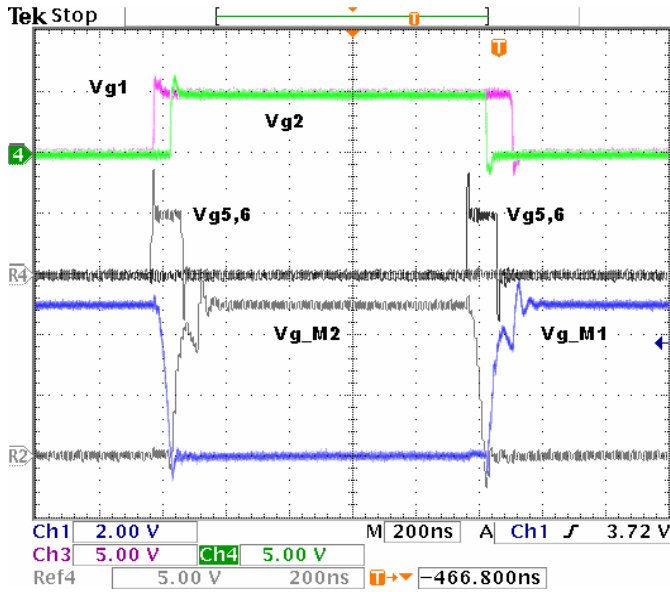


Fig. 11 Key experiment waveform

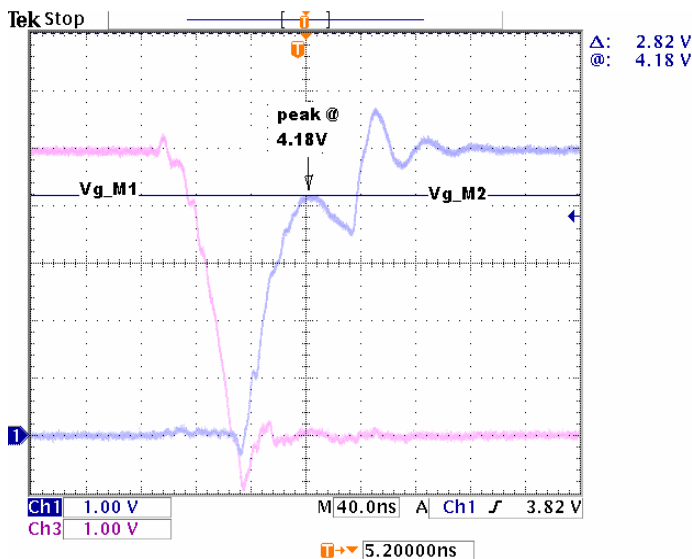


Fig. 12 Detail gate voltage waveform

### V. CONCLUSION

This paper presents a new resonant gate drive circuit. About 70% gate energy can be recovered by utilizing leakage inductance of transformer as resonant component. Pulse

controlled resonance is used to alleviate the conduction loss. Resonance between leakage inductance and gate capacitance can also provide fast transition that would not only reduce switching loss of MOSFET, also minimize the limitation of duty cycle. Further, voltage is only applied on transformer during transition. Voltage-second of transformer is small, thus smaller size of transformer is expected. Because of transformer implementation, it can drive MOSFETs with both same reference ground and different ground, which is suitable for buck converter or bridge converter. The internal gate resistance has significant impact on the resonant gate driver's performance. With improvement of gate resistance of MOSFET, resonant gate driver will benefit from it, saving more gate drive energy.

### VI. REFERENCES

- [1] K. Yao, F.C. Lee, "A novel resonant gate driver for high frequency synchronous buck converters," *IEEE Transaction on power electronics*, Vol. 17, No.2, March 2003, pp.180-186.
- [2] D. Maksimovic, "A MOS gate drive with resonant transitions," in *Proc. IEEE PESC'91 Conf.*, pp. 527-532
- [3] Y. Panov, M.M. Jovanovic, "Design considerations for 12-V/1.5-V, 50-A voltage regulator modules," *IEEE transaction on power electronics*, Nov. 2001, pp. 776-783.
- [4] S.H. Weinberg, "A novel lossless resonant MOSFET driver," in *Proc. IEEE PESC'92 Conf.*, pp. 1003-1010
- [5] J.Diaz, M.A. Perez, F.M. Linera, F. Aldana, "A new lossless power MOSFET driver based on simple DC/DC converters," in *Proc. IEEE PESC'95 Conf.*, pp. 37-43.
- [6] J. Diaz, M.A. Perez, F.J. Linera, F. Nuno, "A new family of loss-less power MOSFET drivers," in *Power Electronics Congress Proceedings (CIEP)*, 1994, pp. 43-48.
- [7] Y. Chen, F.C. Lee, L. Amoroso, H. Wu, "A resonant MOSFET gate driver with efficient energy recovery," *IEEE Transactions on Power Electronics*, Vol. 19, No.2, March 2004, pp.470-477.
- [8] B.S. Jacobson, "High frequency resonant gate drive for a power MOSFET," in *High Frequency Power Conversion Conference (HFPC)*, 1993, pp. 133-141.
- [9] T. Lopez, G. Sauerlaender, T. Duerbaum, T. Tolle, "A detailed analysis of a resonant gate driver for PWM applications," in *IEEE Applied Power Electronics Conference (APEC)*, 2003, pp. 873-878.
- [10] H.L.N. Wiegman, "A resonant pulse gate drive for high frequency applications," in *IEEE Applied Power Electronics Conference (APEC)*, 1992, pp. 738-743.