A Resonant Gate Drive Circuit with Reduced MOSFET Switching and Gate Losses

Wilson Eberle (*Student Member IEEE*), Yan-Fei Liu (*Senior Member IEEE*), **and** P.C. Sen (*Fellow IEEE*)
Queen's Power Group, www.queenspowergroup.com
Department of Electrical and Computer Engineering, Queen's University, Kingston, Ontario, Canada, K7L 3N6
wilsoneberle@wilsoneberle.com, senp@post.queensu.ca and yanfei.liu@queensu.ca

Abstract **- In this paper, a new resonant gate drive circuit is proposed for power MOSFETs. The proposed circuit achieves quick turn on and turn off transition times to reduce switching loss and conduction loss in power MOSFETS. In addition, it can recover a portion of the CV^2 gate energy normally dissipated in a conventional driver. The circuit consists of four control switches and a small resonant inductance. The current through the resonant inductance is discontinuous in order to minimize circulating current conduction loss. Experimental results are presented for the proposed driver operating in a boost converter at 1MHz. At 5V gate drive, 4% efficiency improvement is achieved. At 12V gate drive, 6.5% efficiency improvement is achieved.**

I. INTRODUCTION

In recent years there has been a trend to increase the switching frequency beyond 1MHz in low voltage high current DC-DC power supplies. The objectives of this trend are to increase the power density by decreasing the size of passive components and to improve the dynamic performance. Furthermore, it is well understood that as switching frequency increases, both switching loss and gate loss increase. In the past two decades, much work has been done on reducing, or eliminating turn on switching loss through soft switching techniques. However, in general, these techniques require additional components and do not reduce turn off switching loss. In addition, these techniques do nothing to reduce gate loss. Therefore, with some improvements achieved through reduction in turn on switching loss, it is now essential to focus some effort on reducing turn off switching loss and gate loss in order to continue to achieve greater power density and dynamic performance.

A conventional gate drive circuit is illustrated in Fig. 1 to drive a power MOSFET, Q. With these drivers, all of the power MOSFET gate energy is dissipated. Energy is absorbed from the line source, V_{cc} during turn on of Q and then dumped to ground during turn off. For this drive circuit, the gate energy loss due to charging and discharging the gate capacitance of Q is given by (1), where Q_g represents the total gate charge, V_{gs} is the driving voltage and f_s is the switching frequency. This energy is dissipated as RMS loss in: 1) the driver switches Q_N and Q_P, 2) the external resistance, R_{ext}, and 3) the parasitc gate mesh resistance, R_g, of Q. This loss component is well understood and is often called the CV^2 gate loss.

$$P_{gate} = Q_g V_{gs} f_S \qquad (1)$$

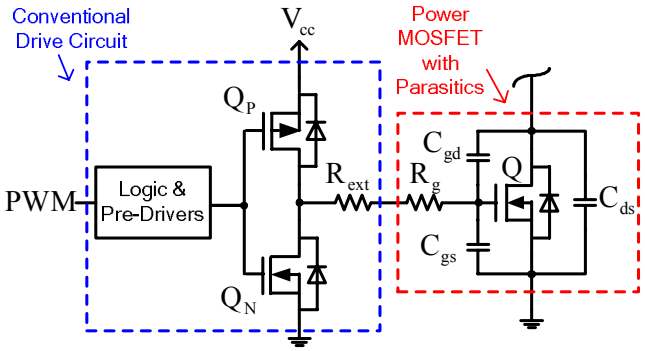


Fig. 1 Conventional gate drive circuit with power MOSFET and its associated parasitics

In addition to the CV^2 loss, conventional gate drivers exhibit switching loss, shoot-through loss and gate loss in their control switches. These losses are often neglected in by engineers, which is a mistake. It was demonstrated in [1] that the power MOSFET CV^2 RMS loss is approximately only 66.7% of the total gate drive circuit loss. The additional components of the gate drive circuit loss include approximately 17.6% for switching loss and 15.7% for gate loss in the driver switches Q_N and Q_P. As illustrated in Fig. 2, normalized with respect to the CV^2 RMS gate loss, these components are significant. An additional 26% of loss can be attributed to hard switching in the control switches and 24% to gate loss in the control switches. Neglecting these components yields an under estimate of gate loss that neglects an additional 50% of the total gate circuit loss!

The problems of the conventional gate driver extend beyond the gate drive circuit loss. Since these drivers operate with RC type charging and discharging, switching speed is limited. The MOSFET gate current is limited to a value significantly less than the peak driver current during the turn on and turn off times which occur during the plateau and threshold regions of the MOSFET gate-to-source voltage. This is illustrated by simulation in Fig. 3. In this example, the peak driver current is 1.5A. However, during the turn on switching time from the threshold to the end of the Miller plateau, the gate current decays to 0.75A. During the turn off switching time, the problem is even more severe since the gate current decays to -0.3A. Therefore, since these drivers are designed for peak current capability, they are not optimized to minimize switching loss and in particular, turn off switching loss.

1-4244-0136-4/06/$20.00 ©2006 IEEE

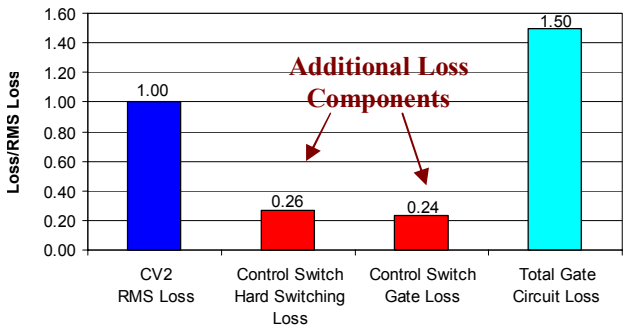


Fig. 2 Conventional gate drive circuit loss normalized with respect the power MOSFET CV^2 gate loss in (1)

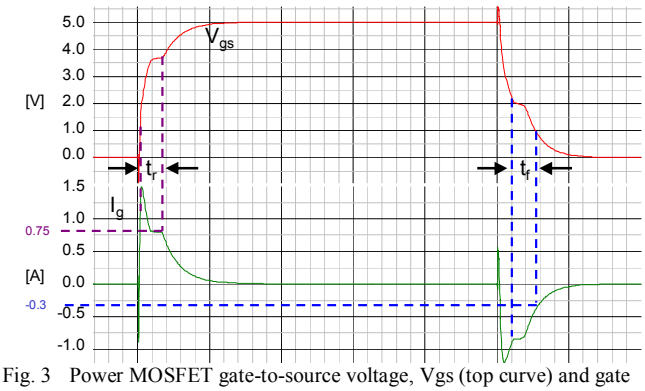


Fig. 3 Power MOSFET gate-to-source voltage, Vgs (top curve) and gate current (bottom curve), Ig during switching transitions

In hard switching converters, the turn on switching loss is given by (2), and the turn off switching loss is given by (3), where V_{ds} represents the voltage across. In (2), I_{onpk}, represents the instantaneous current through the switch at turn on and t_r represents the rise time. In (3), I_{offpk} represents the instantaneous current through the switch at turn off and t_f represents the fall time. Since both t_r and t_f are both inversely proportional to the gate current, I_g, it is clear that switching losses can be reduced by increasing gate current. However, in conventional gate drivers, this is generally not possible since the peak current is already limited by the current handling capability of the driver switches.

$$P_{on} = \frac{1}{2} V_{ds} I_{onpk} t_r f_S \quad (2)$$

$$P_{off} = \frac{1}{2} V_{ds} I_{offpk} t_f f_S \quad (3)$$

From a gate energy perspective, in order to recover a portion of the gate energy otherwise lost in conventional drivers, several papers have been published since the early 1990s proposing resonant gate drive techniques. In these techniques, the resonant inductance yields current source drive which has the potential to reduce switching times and therefore switching loss. However, none of the papers have advertised the significant benefit of reduced switching loss due to current source drive.

Of the methods previously proposed, all of them suffer from at least one of five problems:

1) High circulating current in the driver control switches during the power MOSFET on and off states resulting in excessive conduction loss [2].
2) Peak driver current dependent on duty cycle, or switching frequency resulting in switching times and gate loss that varies with the operating point [2] .
3) Large inductance [2], bulky transformer, or coupled inductance [3]-[7].
4) Slow turn on and/or turn off transition times, which increases both conduction and switching losses in the power MOSFET due to charging the power MOSFET gate beginning at zero current [3]-[9].
5) The inability to actively clamp the power MOSFET gate to the line during the on time and/or to ground during the off time, which can lead to undesired false triggering of the power MOSFET gate, i.e. lack of Cdv/dt immunity [3]-[7],[9].

To solve the problems inherent to conventional drivers, the five problems above, and to reduce switching loss, a new resonant gate drive circuit is proposed in the following section. This driver is an improvement over that proposed in [10], which operated with two of the switches switching at three times the switching frequency and did not exploit the potential switching loss savings.

II. Proposed Resonant Driver and Operation

The proposed resonant gate driver is illustrated in Fig. 4. It consists of four control switches, Q_1-Q_4 including their body diodes, D_1-D_4, and a small inductance, L_R. The switches and diodes are controlled in a way to allow the inductor current to be discontinuous and allow the power MOSFET to turn on or off beginning from a non-zero pre-charge current. Following charging, or discharging of the power MOSFET, the excess inductor stored energy is allowed to return to the line voltage, V_{cc}, thereby allowing ideally 100% of the power MOSFET gate charge energy to be recovered.

The current paths during the four intervals of the turn on stage are illustrated in Fig. 5. The current paths during the four intervals of the turn off stage are illustrated in Fig. 6. The gating waveforms of the four control switches, Q_1-Q_4, along with the inductor current, gate current, power MOSFET gate-to-source voltage and the line current are illustrated in Fig. 7.

The operation of the circuit is explained in the following paragraphs. Initially it is assumed that the power MOSFET is in the off state before time t_0. For the control switches, the shaded regions indicate the on state, so initially only switch Q_3 and D_4 are on and the gate of Q is clamped to zero volts. The black regions indicate the on state for the diodes.

t_0-t_1: At t_0, D_4 turns off with zero current switching (ZCS) and Q_2 turns on (with ZCS) allowing the inductor current to ramp up. The current path during this interval is Q_2-L_R-Q_3. Since Q_3 is in the on state, the gate of Q is clamped low. The interval ends at t_1.

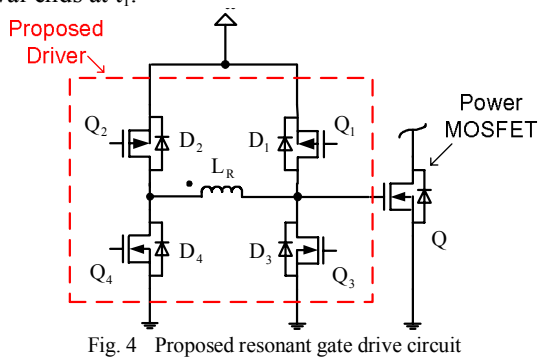


Fig. 4 Proposed resonant gate drive circuit

t_1-t_2: At t_1, Q_3 turns off, which allows the inductor current to begin to charge the power MOSFET gate. The inductor current continues to ramp up, but with a reduced slope as the voltage across the gate capacitance increases. The current path during this interval is Q_2-L_R-C_g, where C_g represents the equivalent gate capacitance of Q. This interval ends at t_2, when V_{gs} reaches V_{cc}. If this interval is allowed to continue, D_1 allows the current to freewheel through Q_2-L_R-D_1.

t_2-t_3: At t_2, Q_2 turns off and Q_1 turns on with zero voltage switching (ZVS) and D_4 turns on, allowing the inductor current to conduct into the dot through the path D_4-L_R-Q_1. Most importantly, it is during this interval when the stored energy in the inductor is returned to the line. This can be observed from the negative portion of the I_{Vcc} curve in Fig. 7. Also, during this interval, the inductor voltage has become reverse biased, so the inductor current quickly ramps down towards zero. During this interval, the gate voltage of Q remains clamped to the line voltage, V_{cc}. The interval ends when the inductor current reaches zero at t_3.

t_3-t_4: At t_3, D_4 turns off (with ZCS) and D_2 turns on, which allows any residual inductor current to freewheel through Q_1-L_R-D_2. During this interval, the gate voltage of Q remains clamped to V_{cc}. The interval ends at t_4 when the pre-charging interval for the turn off cycle begins as dictated by the PWM signal.

t_4-t_5: At t_4, the turn off pre-charging interval begins. D_2 turns off (with ZCS) and Q_4 turns on (with ZCS). Since Q_1 was previously on, the inductor current begins to ramp negative out of the dot through the path Q_1-L_R-Q_4. During this interval, the gate voltage of Q remains clamped to V_{cc}. The interval ends at t_5.

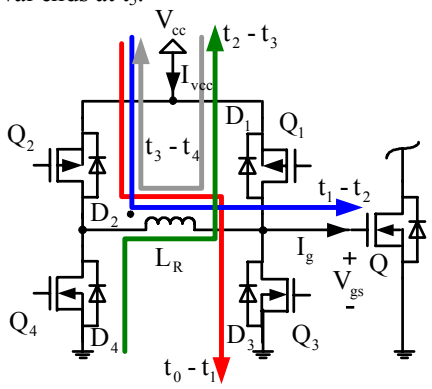


Fig. 5 Proposed resonant gated drive circuit current paths during the turn on interval

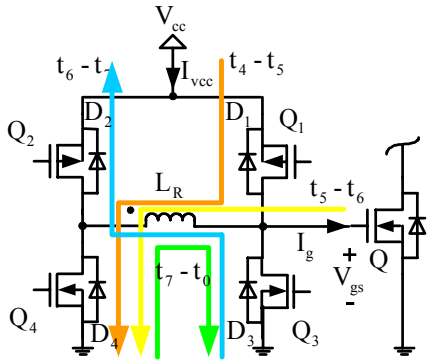


Fig. 6 Proposed resonant gated drive circuit current paths during the turn off interval

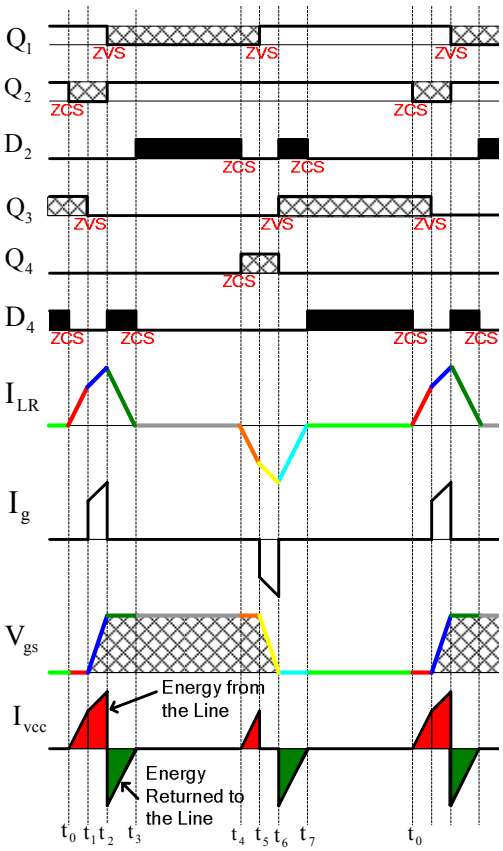


Fig. 7 Waveforms of the proposed resonant gate driver

t_5-t_6: At t_5, Q_1 turns off, which allows the inductor current to begin to discharge the power MOSFET gate. The inductor current continues to ramp negative, but with a reduced slope as the voltage across the gate capacitance decreases. The current path during this interval is C_g-L_R-Q_4, where C_g represents the equivalent gate capacitance of Q. This interval ends at t_6, when V_{gs} reaches zero. If this interval is allowed to continue, D_3 allows the current to freewheel through D_3-L_R-Q_4.

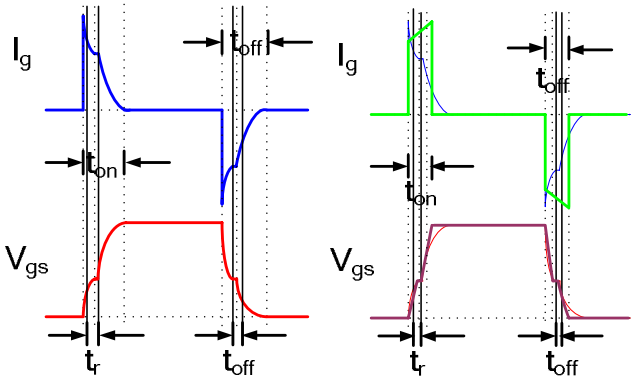
t_6-t_7: At t_6, Q_4 turns off and D_2 turns on and Q_3 turns on (with ZVS) allowing the inductor current to conduct out of the dot through the path Q_3-L_R-D_2. Most importantly, it is during this interval when the gate discharging energy is returned to the line. This can be observed from the negative portion of the I_{Vcc} curve in Fig. 7. Also, during this interval, the inductor voltage has become reverse biased, so the inductor current quickly ramps down positive towards zero. During this interval, the gate voltage of Q remains clamped to ground. The interval ends when the inductor current reaches zero at t_7.

t_7-t_0: At t_7, D_2 turns off (with ZCS) and D_4 turns on, which allows any residual inductor current to freewheel through D_4-L_R-Q_3. During this interval, the gate voltage of Q remains clamped to ground. The interval ends at t_0 when the pre-charging interval for the turn on cycle begins and the entire process repeats as dictated by the PWM signal.

III. Switching Loss Savings

As discussed in section I, switching loss is proportional to the rise and fall times, t_r and t_f, during the switching transition. The rise and fall times are inversely proportional to the gate current provided by the driver. In the

conventional driver, the gate current decays significantly from its peak value due to the RC type charging and discharging as illustrated in Fig. 8(a). On the other hand, the proposed resonant gate driver behaves like a current source and the gate current actually increases slightly during the rise and fall times as illustrated in Fig. 8(b). The result is that the turn on and turn off times decrease significantly and more importantly, the rise and fall times decrease significantly, which decreases switching loss.



(a) (b)

Fig. 8 Comparison between the gate current (top) and voltage (bottom) waveform shapes for the conventional driver (a) left and resonant driver (b) right

IV. Logic Implementation

The logic required to produce the gating signals for the four control switches, Q_1-Q_4 is very simple. The waveforms used to derive the logic are illustrated in Fig. 9. The logic circuit is illustrated in Fig. 10. The circuit requires only 2 delay elements and 6 logic elements. The delay elements can be implemented using tapped delay line ICs. The output of the logic circuit is the four gate drive signals. Following the logic, pre-drivers (not shown) should be used to drive the control switches.

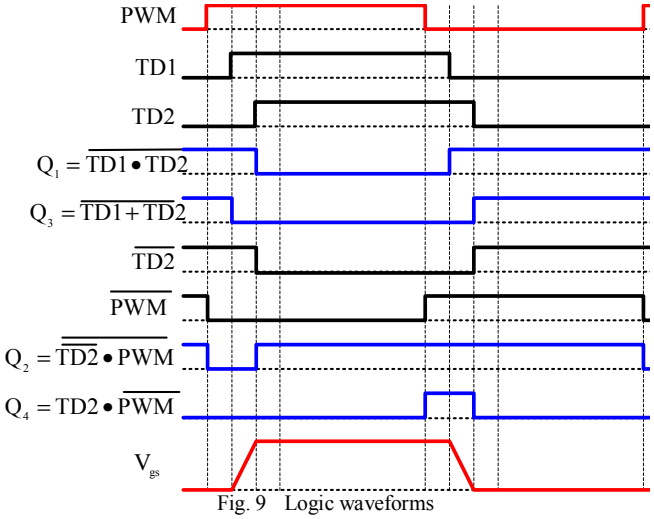


Fig. 9 Logic waveforms

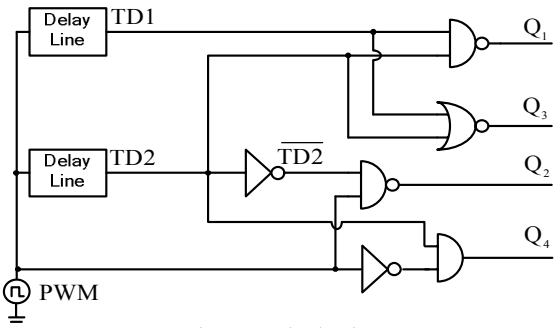


Fig. 10 Logic circuit

V. Design Procedure

The power MOSFET turn on transition time, t_{on}, (from 0V to V_{cc}) is not calculated, but must be chosen by the designer for the given application. For the designer, there is a tradeoff between speed, which translates into switching loss savings, and gate energy recovery. Smaller values of t_{on} reduce switching loss, but require greater peak current in the driver and therefore suffer from greater conduction loss in the driver. Typically, t_{on} should be less than 10% of the switching period. After selecting t_{on}, the turn on inductor pre-charge time, t_{d1} should be selected. This is illustrated in Fig. 11 from t_0-t_1, of the inductor current waveform during the turn on interval. Typically, t_{d1} should be less than t_{on}. Larger values of t_{d1} yield a larger required inductance and add more delay in the control loop. On the other hand, if t_{d1} is too small, the gate energy recovery is limited, or the pre-charge current level is small. A typical starting value of t_{d1} is half of t_{on}.

In order to calculate the required resonant inductance, (4)-(6), must be used. Equation (4) is derived assuming that there is no resistive loss in the drive circuit during t_{d1}.

$$L_R = \frac{V_{cc} t_{d1}}{i_{LR}(t_1)} \tag{4}$$

Equation (5) is derived using an approximation. The equivalent resonant circuit during t_{on} is complex to solve, but since the power MOSFET gate capacitor voltage increases from zero to V_{cc} during t_{on}, then the average capacitor voltage during the interval is $V_{cc}/2$. Using this approximation, the ripple current component, Δi_{LR}, is approximated as (5).

$$\Delta i_{LR} \approx \frac{V_{cc}}{2} \frac{t_{on}}{L_R} \tag{5}$$

The current at time t_1 is then approximated by (6).

$$i_{LR}(t_1) \approx I_{avg} - \frac{\Delta i_{LR}}{2} \tag{6}$$

Using (4)-(6), the required resonant inductance can be calculated using (7).

$$L_R = \frac{V_{cc} t_{on}}{Q_g} \left(\frac{t_{on}}{4} + t_{d1} \right) \tag{7}$$

VI. Loss Analysis

The loss components are outlined below.

A. Conduction Loss

This sub-section will focus on the conduction loss in the control switches. The power MOSFET being driven is represented by an RC network consisting of its parasitic series gate resistance, R_g, and an equivalent gate capacitance, C_g and total gate charge data from the device datasheet.

During the on state, the control switches can be represented by series resistances R_1-R_4. The inductor copper loss can be represented by an equivalent series AC resistance, R_L.

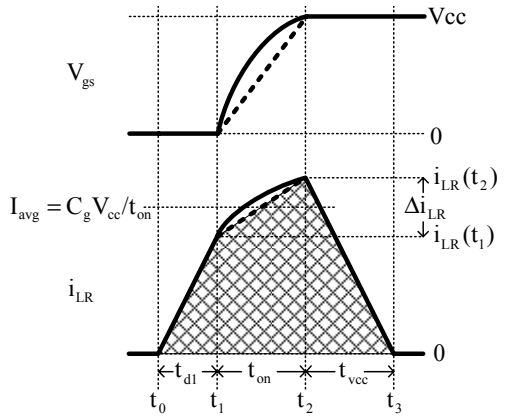


Fig. 11 Detailed inductor current waveform and power MOSFET gate voltage during the turn on interval

The conduction loss can be determined by analyzing the losses during the three main states of the turn on interval (t_0-t_3) and three states of the turn off interval (t_4-t_7) when the inductor current is non-zero. The detailed inductor current waveform and power MOSFET gate voltage waveform are shown for the turn on interval in Fig. 11. Using a piecewise linear approximation to simplify the analysis, the inductor current waveform can be approximated using the dotted portion during t_{on}, if it is assumed that the gate is driven by a constant current source of value I_{avg} during t_{on}. The analysis of the turn on intervals is explained as follows.

t_{d1}: The equivalent circuit during t_a is given in Fig. 12(a), where R_2, R_L and R_3 have been lumped together as R_{td1}. The inductor current, $i_{LR}(t)$, is given by (8). Since the series resistance R_{td1} is quite small, the time constant is large relative to the transition interval, so (8) can be approximated by (9). Using the approximation, the RMS current during this interval is given by (10) and the power consumption, P_{td1}, during the interval is given by (11).

$$i_{LR}(t) = \frac{V_{cc}}{L_R} t e^{-\frac{R_{td1a}}{L_R}t} \tag{8}$$

$$i_{LR}(t) \approx \frac{V_{cc}}{L_R} t \tag{9}$$

$$i_{td1\_RMS} = i_{LR}(t_1)\sqrt{\frac{t_{d1} f_S}{3}} \tag{10}$$

$$P_{td1} = i_{LR}(t_1)^2 \frac{t_{d1} f_S}{3} R_{td1} \tag{11}$$

The pre-charge time interval can be derived as (12).

$$t_{d1} = \frac{L_R}{V_{cc}} i_{LR}(t_1) \tag{12}$$

t_{on}: The equivalent circuit during t_{on} is given in Fig. 12(b). The circuit is a series RLC circuit consisting of R_2, R_L, R_G, L_R and C_g, where R_2, R_L and R_G have been lumped together as R_{on}. The inductor current, $i_{LR}(t)$, is given by (13), which is quite complex to calculate the RMS value during the given interval. However, using the piecewise linear approximation illustrated in Fig. 11, the RMS current during t_{on} is given by (14) and the power consumption, P_{on}, during the interval is given by (15).

$$i_{LR}(t) = \frac{V_{cc}\sqrt{L_R C_g}}{L_R} \sin\left(\frac{1}{\sqrt{L_R C_g}} t\right) + i_{LR}(t_1)\cos\left(\frac{1}{\sqrt{L_R C_g}} t\right) \tag{13}$$

$$i_{on\_RMS} \approx \sqrt{t_{on} f_S}\sqrt{\left[\frac{i_{LR}(t_2)+i_{LR}(t_1)}{2}\right]^2 + \frac{[i_{LR}(t_2)-i_{LR}(t_1)]^2}{12}} \tag{14}$$

$$P_{on} = t_{on} f_S \left(I_{avg}{}^2 + \frac{\Delta i_{LR}{}^2}{12}\right) R_{on} \tag{15}$$

t_{vcc}: The equivalent circuit during t_{vcc} is given in Fig. 12(c), where R_L and R_1 have been lumped together as R_{vcc} and the diode voltage drop is considered constant at V_F. The inductor current, $i_{LR}(t)$, is given by (16). Since the series resistance R_{vcc} is quite small, the time constant is large relative to the transition interval, so (16) can be approximated by (17). Using the approximation, the RMS current during this interval is given by (18) and the power consumption, P_{vcc}, during the interval is given by (19).

$$i_{LR}(t) = i_{LR}(t_2) - \frac{V_{cc} - V_F}{L_R} t e^{-\frac{Rvcc}{L_R}t} \tag{16}$$

$$i_{LR}(t) \approx i_{LR}(t_2) - \frac{V_{cc} - V_F}{L_R} t \tag{17}$$

$$i_{vcc\_RMS} = i_{LR}(t_2)\sqrt{\frac{t_{vcc} f_S}{3}} \tag{18}$$

$$P_{vcc} = i_{LR}(t_2)^2 \frac{t_{vcc} f_S}{3} R_{vcc} + V_F \int_{t_2}^{t_3} \left(i_{LR}(t_2) - \frac{V_{cc} - V_F}{L_R} t\right) dt \tag{19}$$

The time interval t_{vcc} can be expressed as (20).

$$t_{vcc} = \frac{L_R}{V_{cc} + V_F} i_{LR}(t_2) \tag{20}$$

To simplify the analysis, it can be assumed that the turn on and turn off states of operation are identical. Therefore, under this assumption, the total conduction loss in the proposed resonant gate drive circuit is two times the sum of P_{td1} plus P_{on} plus P_{vcc} as given by (21).

$$P_{cond} = 2(P_{td1} + P_{on} + P_{vcc}) \tag{21}$$

B. Gate Loss

The gate loss in Q_1-Q_4 is given by (22).

$$P_{Q1-Q4gate} = (Q_{g1} + Q_{g2} + Q_{g3} + Q_{g4}) V_{cc} f_s \tag{22}$$

C. CV^2 Output Loss

The CV^2 output loss in Q_2 and Q_4 at turn on, is given by (23) where C_{oss2} and C_{oss4} represent the output capacitance values for Q_2 and Q_4 obtained from the MOSFET data sheets.

$$P_{out} = (C_{oss2} + C_{oss4}) V_{cc}{}^2 f_s \tag{23}$$

D. Turn Off Loss

Q_2 and Q_4 turn off at the peak inductor current, $i_{LR}(t_2)$. The turn off loss in Q_2 and Q_4 is given by (24) where the fall times, t_{f2} and t_{f4} are obtained from the MOSFET data sheets.

$$P_{off} = \frac{1}{2} V_{cc} i_{LR}(t_2)(t_{f2} + t_{f1}) f_s \tag{24}$$

E. Core Loss

The core loss can be obtained by standard core loss estimation methods and should be small in comparison to the other loss components.

F. Logic Loss

The loss in the logic circuit should be negligible in comparison to the other components, so it can be neglected.

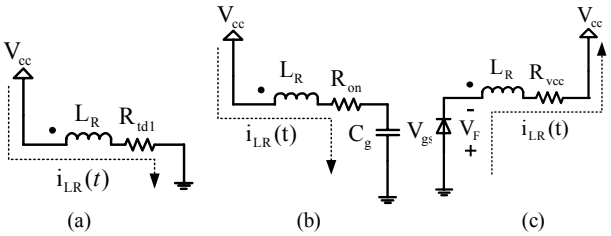


Fig. 12 (a) Equivalent circuit during the pre-charge interval td1, (b) Equivalent circuit during the turn-on transition interval ton (c) Equivalent circuit during the ramp down interval tvcc

VII. Simulation and Experimental Results

SIMetrix 5.1, was used to simulate the proposed resonant gate driver with a Boost converter operating at 1MHz. Spice models were used for all components. The waveforms for the proposed driver are illustrated in Fig. 13. It is clear that since the line current, I_{vcc} goes negative, therefore gate energy is saved. The proposed driver recovered 68% of the gate energy in comparison to the conventional driver. This is close the 70% calculated using the loss analysis.

More impressive than the gate energy recovery was the switching loss savings. The total conduction and switching loss power dissipated in Q in the conventional driver was 4.715W, however with the resonant driver, only 2.658W were dissipated. Both drivers achieved a turn on rise time of approximately 30ns, however the resonant driver achieved a turn off fall time of only 15ns in comparison to 38ns for the conventional driver. It is clear that potential switching loss savings using the proposed driver is very significant.

Boost converter experimental results are illustrated for 5V gate drive in Fig. 14 and 12V gate drive in Fig. 15. The switching frequency of the Boost was 1MHz and two IRF6618 MOSFETs were used in parallel. The Boost diode was 10TQ035. The results were compared to the UCC37322 conventional gate driver. At 5V a 4% efficiency improvement was achieved with the resonant driver at full load. At 12V a 6.5% efficiency improvement was achieved.

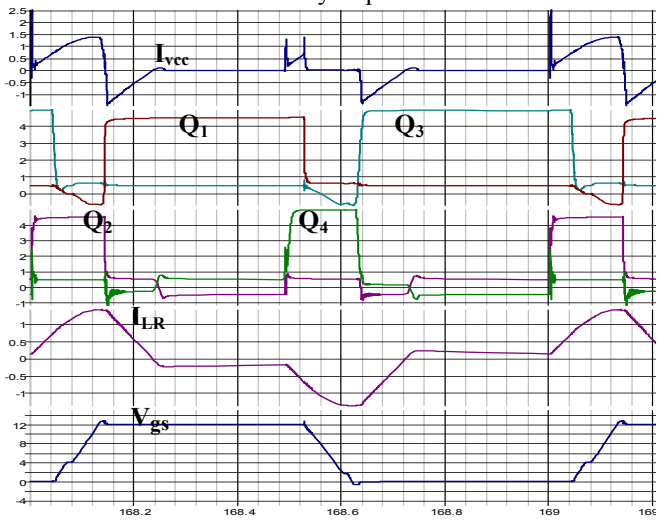


Fig. 13 Simulation results for the proposed driver at 1MHz switching frequency (top: line current from V_{CC}, second: Q_1 & Q_3 gate signals, third: Q_2 & Q_4 gate signals, fourth: L_R current, bottom: power MOSFET gate voltage)

VIII. Conclusions

A new resonant gate drive circuit has been proposed that can recover power MOSFET gate energy and reduce switching loss. The current in the resonant inductance is discontinuous to minimize conduction loss. This also allows the driver to operate effectively over a wide range of duty cycles with constant peak current – a significant advantage for many applications since turn on and turn off times do not vary with the operating point. The driver provides superior performance in comparison to conventional drivers and solves the problems of existing resonant gate drivers.

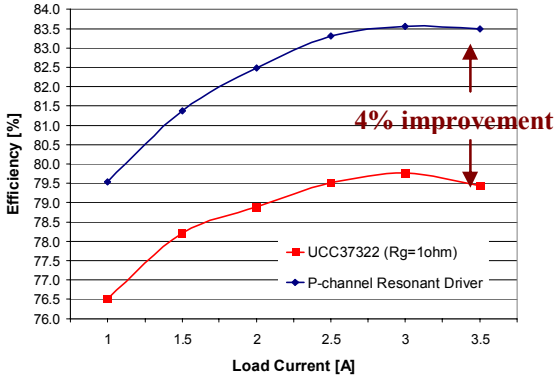


Fig. 14 Boost converter efficiency at 5V Vcc

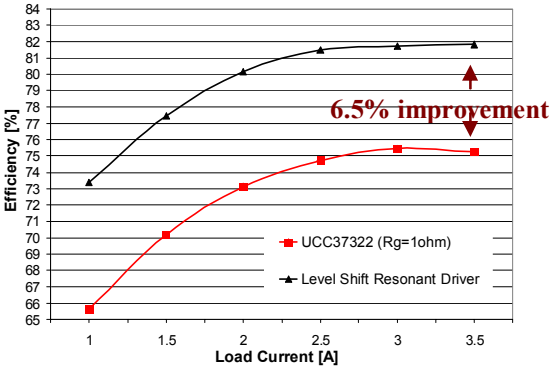


Fig. 15 Boost converter efficiency at 12V Vcc

References

[1] T. Lopez, G. Sauerlaender, T. Duerbaum, T. Tolle, "A detailed analysis of a resonant gate driver for PWM applications," IEEE Applied Power Electronics Conference (APEC), 2003, pp. 873-878.

[2] D. Maksimovic, "A MOS gate drive with resonant transitions," IEEE Power Electronics Specialists Converence (PESC), 1991, pp. 527-532.

[3] H.L.N. Wiegman, "A resonant pulse gate drive for high frequency applications," IEEE Applied Power Electronics Conference (APEC), 1992, pp. 738-743.

[4] S.H. Weinberg, "A novel lossless resonant MOSFET driver," IEEE Power Electronics Specialists Conference (PESC), 1992, pp. 1003-1010.

[5] B.S. Jacobson, "High frequency resonant gate drive for a power MOSFET," High Frequency Power Conversion Conference (HFPC), 1993, pp. 133-141.

[6] J. Diaz, M.A. Perez, F.M. Linera and F. Aldana, "A new losless power MOSFET driver based on simple DC/DC converters," IEEE Power Electronics Specialists Conference (PESC), 1995, pp. 37-43.

[7] K. Yao, F.C. Lee, "A novel resonant gate driver for high frequency synchronous buck converters," IEEE Transactions on Power Electronics, Vol. 17, No. 2, March 2002, pp.180-186.

[8] L. Faye, Q. Jinrong, "Gate driver apparatus having an energy recovering circuit," United States Patent No. US 6,650,169 B2, Nov. 18, 2003.

[9] Y. Chen, F.C. Lee, L. Amoroso, H. Wu, "A resonant MOSFET gate driver with efficient energy recovery," IEEE Transactions on Power Electronics, Vol. 19, No.2, March 2004, pp.470-477.

[10] W. Eberle, Y.F. Liu and P.C. Sen, "A New Resonant Gate Drive Circuit with Low Conduction Loss and Efficient Energy Recovery," IEEE Industrial Electronics Society Conference (IECON), 2005, pp. 650-655.