Topology and Analysis of a New Resonant Gate Driver

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Abstract—This paper proposes a novel resonant gate driver for a high frequency synchronous buck converter. The proposed resonant gate driver can reduce switching losses significantly in addition to gate drive losses compared to a conventional gate driver. Additionally, the proposed driver has better noise immunity to *dv*/*dt* effect and is less sensitive to parasitic inductance. Loss analysis and optimization design of the proposed driver are presented in details. A 1MHz synchronous buck converter with the proposed resonant gate driver was built to verify the functionality.

I. INTRODUCTION

The development in microprocessor technology poses increasing challenges to the power industry. Voltage Regulator (VR) should provide extreme low output voltage with high current capabilities and fast dynamic response. Multiphase synchronous rectifier buck topology is most popular in today's VR industry. In order to achieve high power density and fast transient response, the switching frequency of a VR is expected to increase into MHz range in the near future.

However, with MHz switching frequency, the gate drive loss will increase dramatically, which is proportional to switching frequency. The performance of the gate drive circuit plays a very significant role on the whole efficiency of a VR. To reduce the gate drive loss becomes of critical importance to increase switching frequency further.

More importantly, the increasing switching frequency also increases the switching loss of the converter significantly, which decreases the efficiency of the converter and causes serious thermal problems. However, the conventional gate drive method is a voltage source driven approach and all the energy is dissipated on the resistors in charge and discharge path. In order to recover gate drive energy, several lossless gate drive circuits are proposed in [1-3] in recent years. However, all of these drive circuits are only designed for a single switch and so two sets of resonant drive circuits are required for diving both the control FET and the synchronous FET in a buck converter. A simple dc/dc converter and a transformer are used in [4], which makes the gate driver very complicated and only provides limited energy recovery. A resonant gate driver with simple configuration is proposed in [5], but the switching frequency is limited because both the turn-on interval and turn-off interval must be longer than half of the resonant period. A dual channel resonant gate driver is proposed for a synchronous buck converter in [6]. However, its complexity and coupled inductor may deteriorate the performance of the circuit, which limits its industrial application.

This paper proposes a novel resonant gate driver for high frequency synchronous buck converters, which reduces the gate drive losses and switching losses significantly compared to a conventional driver. The proposed driver has only one inductor to drive two MOSFETs and its configuration is simple, which makes it easier to be integrated into a single driver chip. The operation principle, loss analysis and optimization design procedure are presented. Experimental results verify the advantages of the proposed driver

II. OPERATION PRINCIPLE

Fig. 1 shows the synchronous buck converter with the proposed resonant gate driver as shown in the dotted area. Fig. 2 shows the key waveforms. In the buck converter, Q_1 is the control FET and Q_2 is the synchronous FET. C_{g1} and C_{g2} are the gate-source capacitors of Q_1 and Q_2 respectively. The resonant gate drive circuit consists of four switches S_1-S_4 and its configuration is very similar to full-bridge converter, which makes S_1-S_4 achieve zero-voltage-switching. The flying capacitor C_1 is used for high side drive. The diode D_1 provides the path to charge C_1 to the voltage above the supply voltage V_c. C_b is the blocking capacitor. S_1 and S_3 are switched out of phase to drive Q_1, while S_2 and S_4 are switched out of phase to drive Q_2. The switching transitions of charging and discharging C_{g1} and C_{g2} are during the interval of $[t_0, t_2]$ and $[t_3, t_5]$. The peak current during $[t_0, t_2]$ and $[t_3, t_5]$ is constant during switching transition, which ensure fast charging and discharging of the miller capacitor.

Fig. 3 show the equivalent circuits of the interval of $[t_3, t_4]$ and $[t_4, t_5]$. During $[t_3, t_4]$ as shown in Fig. 3(a), the peak current I_{Lr_pk} flows in the loop consisting of C_{g_Q1}, L_r, C_b, S_4, Q_1 and V_{in} to discharge C_{g1}. The voltage across C_{g_Q1} decreases until it is clamped to zero by the body diode of S_3 before t_4. And Q_1 are turned off.

During $[t_4, t_5]$ shown in Fig. 3(b), the peak current I_{Lr_pk} flows in the loop consisting of S_3, L_r, C_b, C_{g_Q2}, and Q_2 to charge C_{g2}. The voltage across C_{g_Q2} increases until it is clamped to V_c by the body diode of S_2 before t_5. And Q_2 are turned on.

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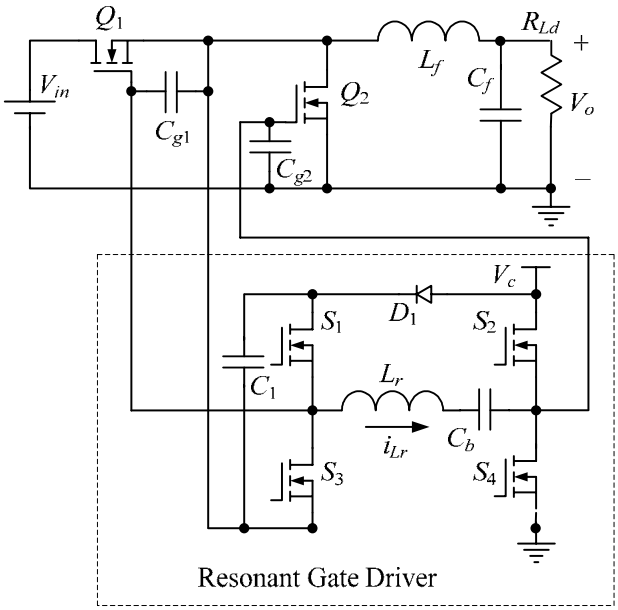


Fig. 1 Propose resonant gate driver

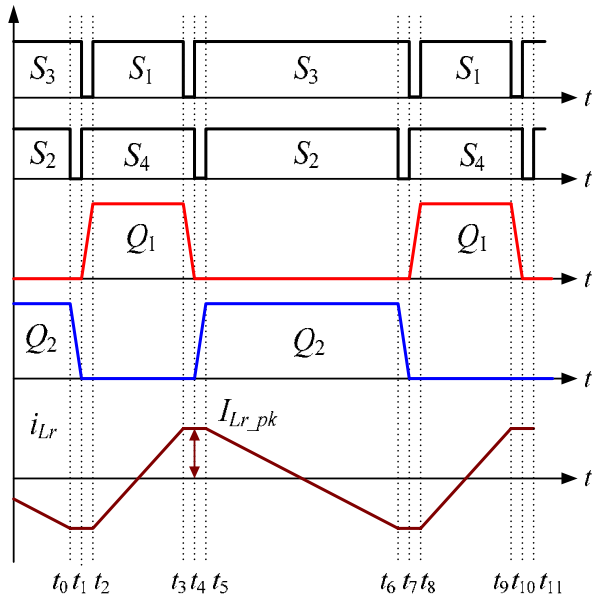
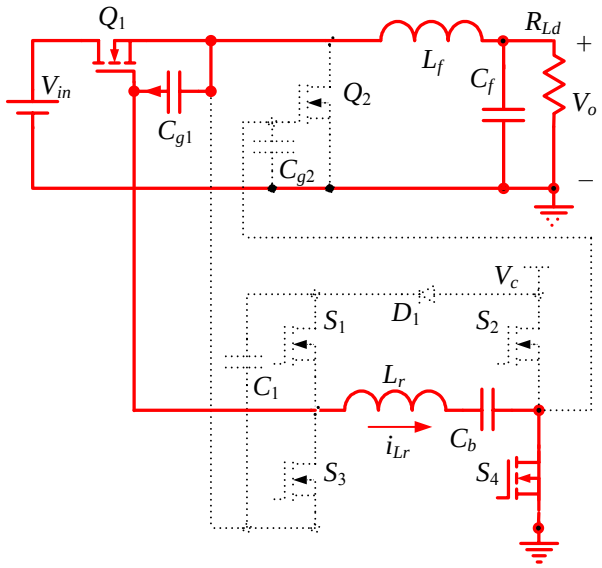
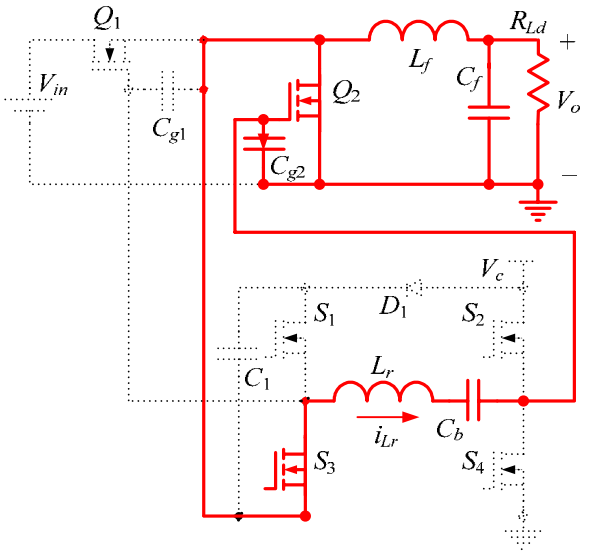


Fig. 2 Key waveforms



(a) [t_3, t_4]



(b) [t_4, t_5]

Fig. 3 Equivalent circuits of the interval of [t_3, t_4] and [t_4, t_5]

The DC voltage across the blocking capacitor C_b is given by Equation (1)

$$v_{Cb} = D \cdot V_{in} + (2D-1) \cdot V_c \tag{1}$$

The relationship of the peak inductor current and the inductor value is given by Equation (2)

$$I_{Lr\_pk} = \frac{(V_{in} + 2V_c) \cdot D \cdot (1-D)}{2L_r \cdot f_s} \tag{2}$$

where V_{in} is the input voltage of the converter; V_c is the gate drive voltage, which can be the input voltage of the converter; f_s is the switching frequency; L_r is the resonant inductor value and D is the duty cycle of the control FET Q_1.

III. Loss Analysis of Resonant Gate Driver

The total power loss of the proposed resonant gate driver includes: 1) the resistive loss and gate drive loss of switches S_1-S_4; 2) the loss of the resonant inductor; 3) the resistive loss caused by the internal gate mesh resistance of the power MOSFETs.

The inductor current waveform indicated in Fig. 2 can be regarded as a triangular waveform since the charging/ discharging time [t_0, t_2] and [t_3, t_5] are very small and can be neglected. Therefore, the RMS value of the inductor current I_{Lr_RMS} is $I_{Lr\_pk}/\sqrt{3}$.

The RMS currents flowing through the switches S_1 and S_4 can be derived as

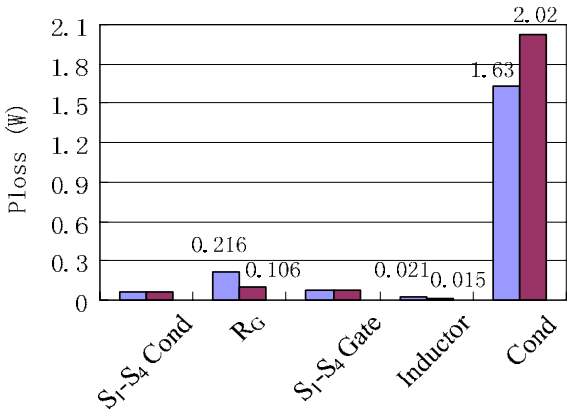


Fig. 4 Loss comparison between V_c=+12V and V_c=+5V of resonant gate driver

$$I_{s1\_RMS} = I_{s4\_RMS} = I_{Lr\_pk} \cdot \sqrt{\frac{D}{3}} \tag{3}$$

The RMS currents flowing through switches S_2 and S_3 are

$$I_{s2\_RMS} = I_{s3\_RMS} = I_{Lr\_pk} \cdot \sqrt{\frac{1-D}{3}} \tag{4}$$

The conduction loss of S_1-S_4 is expressed as

$$P_{cond\_s1-s4} = 2I_{s1\_RMS}{}^2 \cdot R_{ds(on)} + 2I_{s2\_RMS}{}^2 \cdot R_{ds(on)} \tag{5}$$

where $R_{ds(on)}$ is the on-resistance of S_1-S_4, assuming S_1-S_4 are same.

Substituting (3) and (4) into (5) yields

$$P_{cond\_s1-s4} = \frac{2}{3} \cdot I_{Lr\_pk}{}^2 \cdot R_{ds(on)} \tag{6}$$

which is dependent on peak resonant inductor only and is independent of duty cycle.

DC resistance of the inductor winding cannot be used here to directly calculate its copper loss because of the high operation frequency. Skin-effect has to be considered. The copper loss of the inductor winding is expressed as

$$P_{copper} = R_{ac} \cdot I^2{}_{Lr\_RMS} \tag{7}$$

R_{ac} is the AC resistance of the inductor winding. I_{Lr_RMS} is the RMS value of the inductor current. Core loss of the resonant inductor is another loss in this resonant gate drive circuit. The core loss P_{core} depends upon the inductor design. Core materials with high permeability such as 3F5 or PC50 can be used to reduce core loss. The total inductor loss is given in Equation (8):

$$P_{ind} = P_{copper} + P_{core} \tag{8}$$

Both the charge and discharge currents flow through the internal gate mesh resistance R_G of the power MOSFET and cause resistive loss. The charge and discharge current is the peak value of the inductor current. Thus the total loss caused by the internal resistance of two power MOSFETs during turn-on and turn-off is expressed as

$$P_{RG} = 2R_{G1}I^2{}_{Lr\_pk} \cdot t_{sw1} \cdot f_s + 2R_{G2}I^2{}_{Lr\_pk} \cdot t_{sw2} \cdot f_s \tag{9}$$

where t_{sw1} and t_{sw2} are the switching time of MOSFET Q_1 and Q_2 respectively; R_{G1} and R_{G2} are the internal gate resistors of Q_1 and Q_2 respectively and f_s is the switching frequency.

Although the total gate charges of switches S_1-S_4 are very small, they will still cause some losses at high switching frequency. The operating frequency of these four switches is the same as the switching frequency f_s of the power MOSFETs. The gate drive loss of S_1-S_4 is expressed as

$$P_{Gate} = 4 \cdot Q_{g\_s} \cdot V_{gs\_s} \cdot f_s \tag{10}$$

where Q_{g_s} is the total gate charge of a switch and V_{gs_s} is the drive voltage of the switch, which is usually 5V.

Therefore, the total loss of the resonant gate drive circuit can be derived by adding all above mentioned losses together and is expressed as

$$P_{total} = P_{cond} + P_{gate} + P_{ind} + P_{RG} \tag{11}$$

IV. DESIGN OPTIMIZATION

A. *Supply Voltage of the Resonant Gate Driver*

The supply voltage V_c of the resonant gate driver is the gate drive voltage of the control FET and Synchronous FET. Usually, V_c can be +12V or +5V in a computer power system. With a conventional gate driver, V_c of 5V is used as V_c of 12V will generate too much gate drive loss. For the gate charge/ discharge current I_{peak} of 1.2A, when V_c=+12V, the resonant inductor is 2.2uH from Equation (2) and the gate charging time is 10.2ns. For the same $I_{peak,}$ when V_c=+5V, the resonant inductor is reduced to 1.0uH with less turns and the gate charging time is also reduced to 4.3ns. Therefore, the loss of the resonant inductor and the loss of gate mesh resistance under V_c=+5V can be both reduced. But since the drive voltage of the control FET and synchronous FET is +5V, the conduction loss of the MOSFET under V_c=+5V will increase due to higher $R_{ds(on)}$ compared to V_c=+12V drive voltage.

An example is taken for choosing the supply voltage of the resonant gate driver. Fig. 4 gives the calculated loss comparison between V_c=+12V and V_c=+5V of resonant gate driver. The specifications are: input voltage: 12V; rated load current: 20A; V_c=12V; switching frequency: 1MHz; Q_1: IRF7821(30V N-channel, $R_{DS(on)}$=9mΩ@V_{GS}=6V, International Rectifier); Q_2: FNS7088(30V N-channel, $R_{DS(on)}$=3.5mΩ@V_{GS}=6V, Fairchild Semiconductor); S_1-S_4: FDN335N(20V N-channel, $R_{DS(on)}$=0.07Ω@V_{GS}=4.5V, Fairchild Semiconductor); L_f=480nH, L_r=2.2uH.

As seen from Fig. 4. With V_c=+5V, the loss of the resonant inductor and the loss of the gate mesh resistance is reduced by 0.12W, but the MOSFETs conduction loss is increased by 0.39W. Therefore with V_c=+12V, the resonant gate driver will lead to lower total loss compared to V_c=+5V.

B. *Optimizaiton Design Procedure*

As seen from the operation principle, the peak current I_{Lr_pk} of the resonant inductor L_r is regarded as the current source magnitude I_G. So the higher I_{Lr_pk} is, the shorter of switching transition is, thus more switching loss can be saved. On the other hand, higher I_{Lr_pk} will result in a larger RMS value of the inductor circulating current i_{Lr} since the waveform of i_{Lr} is triangular, which increases the energy dissipated in the windings of L_r, on- resistance $R_{ds(on)}$ of S_1-S_4 and the internal gate mesh resistance R_G of the MOSFET. Therefore it is

critical to decide I_{Lr_pk} (i.e., I_G) properly so that the maximum loss saving can be achieved.

The optimization method is proposed to find the solution on the basis of the object function that adds the switching loss and the drive circuit loss together. The object function should be U-shape curve as function the resonant current I_G, thus the optimization solution is simply located at the lowest point of the curve. The demonstration of the optimization methodology is employed to the proposed resonant gate driver with V_c=12V. The specifications are the same as the example mentioned before in previous sub-section.

First, the switching loss of the control FET as function of driven current I_G is calculated from Equation (12)

$$P_{Q1} = \frac{1}{2} \cdot V_{in} \cdot I_{(on)\_Q1} \cdot t_{sw(on)\_Q1} \cdot f_s + \frac{1}{2} \cdot V_{in} \cdot I_{(off)\_Q1} \cdot t_{sw(off)\_Q1} \cdot f_s \quad (12)$$

where $I_{(on)\_Q1}$ and $I_{(off)\_Q1}$ are the drain currents at turn-on interval and turn-off interval respectively, $t_{sw(on)\_Q1}$ is the turn-on switching time and $t_{sw(off)\_Q1}$ is the turn-off switching time. Fig. 5 shows the switching loss $P_{switching}$ as function of driven current I_G, illustrating that the switching loss reduces when I_G increases. It is also noted that when I_G is smaller than 1.5A, the reduction of the switching loss is significant; while I_G is larger than 1.5A, the reduction of the switching loss is not very significant.

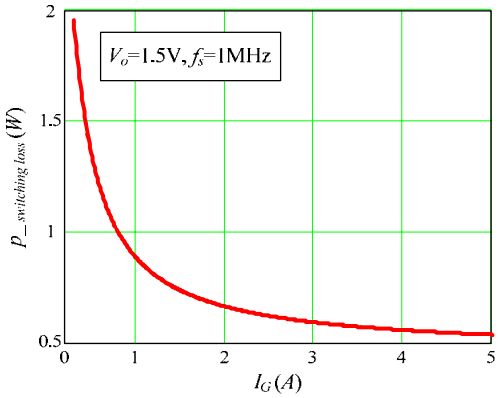


Fig. 5. Switching loss as function of drive current

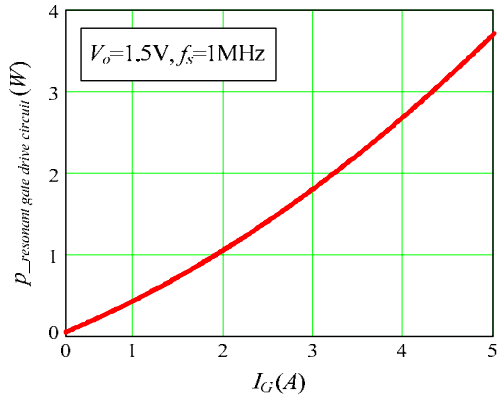


Fig. 6. Loss of resonant gate drive circuit

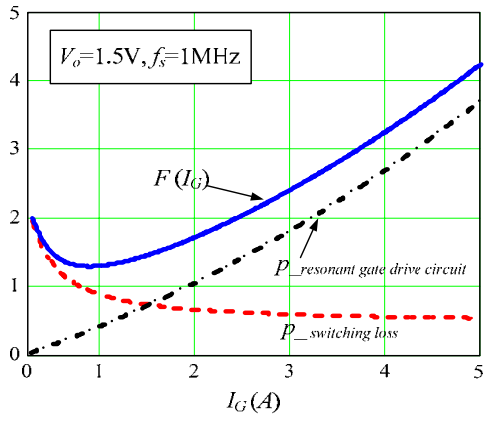


Fig. 7. Objective function $F(I_G)$ as function of current I_G

Secondly, the total loss of the resonant gate drive circuit as function of driven current I_G is calculated from Equation (11). Fig. 6 shows the loss of the total gate drive circuit as function of driven current I_G, illustrating that the circuit loss increases when I_G increases.

Thirdly, in order to find the optimized gate driven current, the objective function is established by summarizing the switching loss and the resonant gate driver loss together, which is expressed as

$$F(I_G) = P_{circuit}(I_G) + P_{switching}(I_G) \quad (13)$$

Fig. 7 shows the objective function $F(I_G)$ with the gate drive current I_G, which is a U-shaped curve. Therefore, the optimization solution can be found at the lowest point of the curve, and accordingly, the gate driven current I_G is 1A.

Finally, from the selected gate driven current, the calculated resonant inductor value from Equation (2) is 2.0uH, where V_o=1.5V, I_o=20A, V_{in}=12V, V_c=12V.

V. Advantages and Loss Comparison

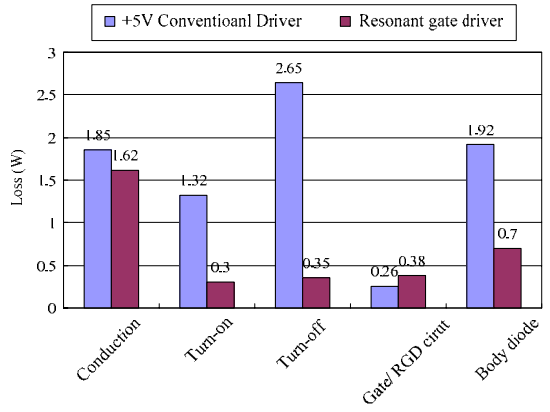
A. Advantages

The key point of this drive circuit is that during the transition when the MOSFET is turned on, its gate capacitor is charged by the peak inductor current, I_{Lpeak} and during the transition when the MOSFET is turned off, the gate capacitor is discharged by the peak inductor current as well. During charging and discharging interval, the inductor current is constant, which reduces the switching loss significantly.

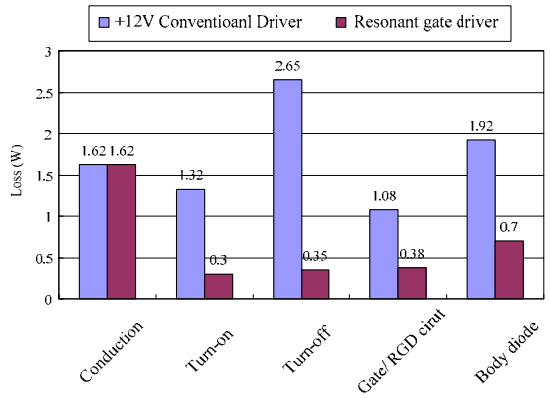
In particular, the reduced switching transition also reduces dead time required to avoid shoot-through between the control FET and the synchronous FET, which leads to the loss reduction of the body diode. Furthermore, the proposed resonant has high *Cdv/dt* immunity since the gate of both MOSFETs are connected to either the voltage source or ground via low impedance path (S_1 to S_4). The fixed delay to prevent shoot-through especially on the low to high transition in most drive ICs using adaptive dead-time circuits can be minimized due to the high *Cdv/dt* immunity and thus the power loss associated with *Cdv/dt* induced turn on of the low-side MOSFET [7] is also avoided.

B. Loss Comparison

Fig. 8 illustrates the loss breakdown comparison between conventional gate diver and the resonant gate driver. In Fig. 8(a), compared to +5V conventional gate driver, the turn-on



(a)Comparison between resonant gate driver with V_c=12V and conventional gate driver of 5V



(b) Comparison between resonant gate driver with V_c=12V and conventional gate driver of 12V

Fig. 8. Loss breakdown

loss is reduced from 1.32W to 0.3W. The turn-off loss is reduced from 2.65W to 0.35W. The loss of body diode is reduced by 1.2W. It is noted that the conduction loss is also reduced 12% (0.23W/1.85W) because the resonant gate driver charges the gate capacitor to 12V, which leads to lower $R_{ds(on)}$ of MOSFETs. So the total loss reduction by the resonant gate driver is 4.65W.

In Fig. 8(b), compared to +12V conventional gate driver, the loss saving of the turn-on loss, turn-off loss and the loss of body diode are same as +5V conventional driver. The conduction loss is same, but the gate charge loss saving is 64% (0.7W/1.1W). Therefore, the total loss reduction by the resonant gate driver is 5.24W.

VI. EXPERIMENT RESULTS

A synchronous buck converter was built to verify the operation principle and advantages of the proposed resonant gate driver. The specifications are as follows: input voltage: 12V; rated load current: 20A; switching frequency: 1MHz; Q_1: IRF7821; Q_2: FNS7088; L_f=480nH; S_1-S_4: FDN335N; L_r=2.2uH.

For comparison, TPS2832 from Texas Instruments using adaptive control from Texas Instrument is chosen as the conventional gate driver chips and its gate drive voltage is 6V. However, the resonant gate driver will charge the gate capacitor to V_c=12V. This leads to lower $R_{ds(on)}$ of the control FET and the synchronous FET, thus achieves an 12% reduction of conduction loss at I_o=20A. Fig. 9 and Fig. 10 illustrate the loss comparison between the resonant gate driver and conventional driver with different output voltages and different output currents respectively. It can be observed that at V_o=2.5V and I_o=20A, the loss reduction of 5W is achieved, which is 10% of the output power. At V_o=1.5V and I_o=20A, a loss reduction of 4.5W is achieved, which is 15% of the output power.

Fig. 11 shows the gate drive signal v_{gs_Q1} and the drain source voltage v_{ds_Q1} of control FET Q_1. v_{gs_Q1} is smooth and no miller plateau is observed as the miller charge is removed very quickly with the constant charging current. Moreover the rise time and fall time of v_{gs_Q1} is less than 20ns, which means a very short switching interval. Fig. 12 shows the gate charge/ discharge current i_{g_Q2} and the drain-source voltage v_{gs_Q2}. It is noted that the gate driven current keeps constant during the switching interval disregarding the current oscillations. Because the extra wire length is used to allow the insertion of a current probe to measure the current waveforms, this introduces higher stray inductances, which causes the parasitic oscillations of the current waveform.

Fig. 13 shows the resonant inductor current i_{Lr} and the drain-source voltage v_{ds_Q2} (Synchronous FET). It can be observed that fast switching transition is ensured by high

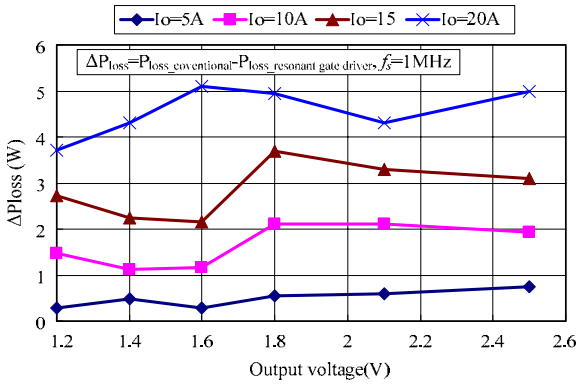


Fig. 9. Loss comparison with different output voltage

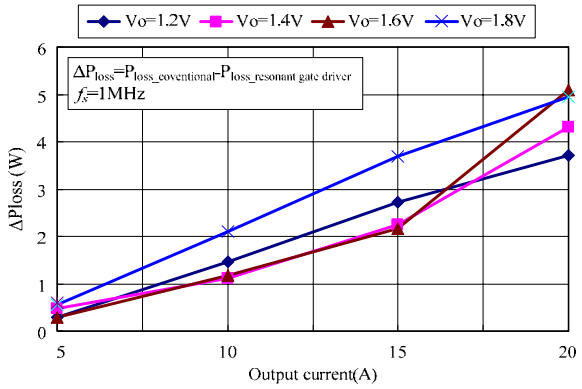


Fig. 10. Loss comparison with different output current

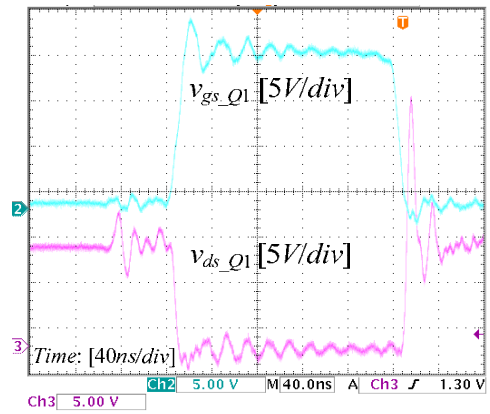


Fig. 11 Waveforms of gate drive signal v_{gs_Q1} and i_{g_Q2} and drain source voltage v_{ds_Q1} (control FET)

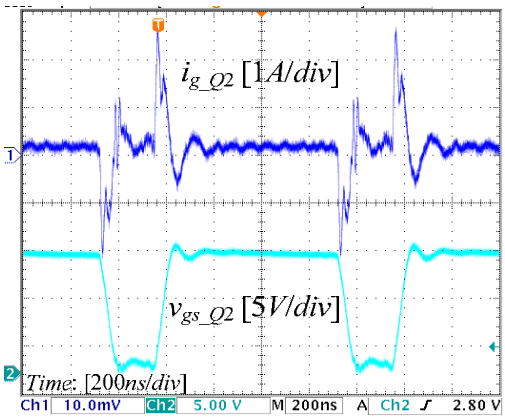


Fig. 12 Waveforms of gate charge/ discharge current drain-source voltage v_{ds_Q2} (Synchronous FET)

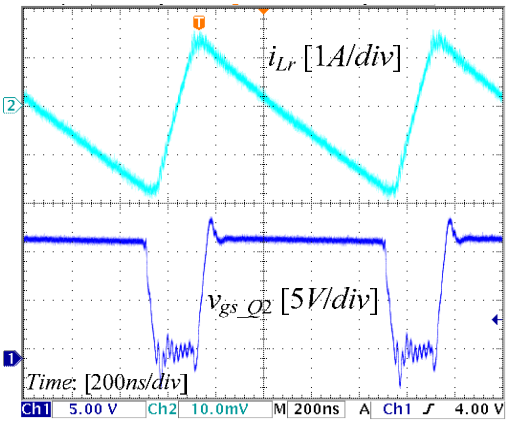


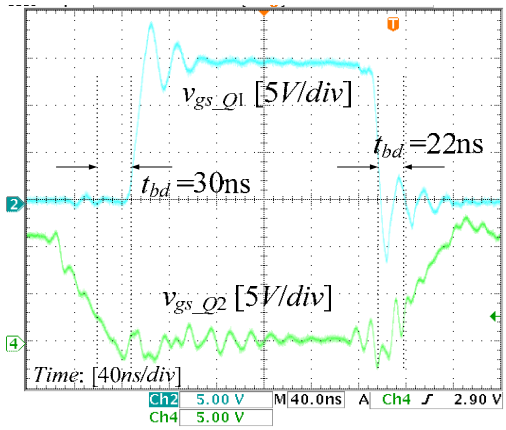
Fig. 13 Waveforms of resonant inductor current i_{Lr} and drain-source voltage v_{ds_Q2} (Synchronous FET)

charge current and discharge current.

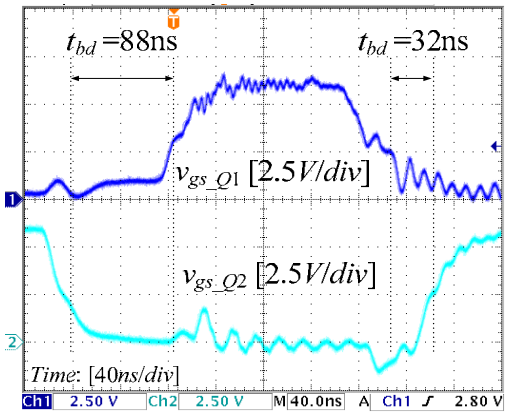
Fig. 14(a) and Fig. 14(b) show the body diode conduction time of the resonant gate driver and conventional gate driver respectively. The body diode conduction time of the resonant gate driver is reduced by 52ns in total compared to conventional gate driver, which reduces the body diode conduction loss significantly.

VII. CONCLUSION

This paper proposes a new resonant gate driver a for high frequency synchronous buck converter. The operation principle, loss analysis and optimization design of the resonant gate driver are presented. Both the gate drive loss and switching loss are significantly reduced, which leads to the reduction of the overall power loss. The proposed resonant gate driver has simple configuration for integration and provides a very promising solution to improve the performance of high frequency VRs for future microprocessors. Theoretical analysis, loss comparison and experimental results verify its functionality



(a) Resonant gate drive



(b) Conventional gate driver

Fig. 14. Waveforms comparison of gate-to-source voltage v_{gs_Q1} (control FET) and v_{gs_Q2} (Syn FET) between resonant gate driver and conventional gate driver

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