Novel Digital Controller Improves Dynamic Response and Simplifies Design Process of Voltage Regulator Module

Eric Meyer (Student Member, IEEE), Guang Feng (Member, IEEE) and Yan-Fei Liu (Senior Member, IEEE)
Queen's Power Group, www.queenspowergroup.com
Department of Electrical and Computer Engineering, Queen's University, Kingston, Ontario, Canada, K7L 3N6
eric.meyer@ece.queensu.ca, gfeng@aps.anl.gov, yanfei.liu@queensu.ca

Abstract- **A novel digital controller is presented in this paper that significantly improves the dynamic response of a voltage regulator module (VRM). The controller uses a digital linear scheme during steady-state operation and an innovative non-linear scheme during transient load conditions. The proposed non-linear controller accurately calculates the optimal response to an arbitrary load step variation. This paper demonstrates the design procedure of a VRM using the proposed controller. Since the response to the load variation is predictable, an engineer is able to design (without iteration) a VRM that is guaranteed to meet a set of dynamic response criteria (voltage deviation, recovery time).**

I. INTRODUCTION

As voltage regulation requirements for high-performance digital circuits become increasingly stringent, it has become necessary to rethink the long-perceived concept that analog, linear controllers are the most suitable for DC-DC converters. Bandwidth limitations of conventional controllers have forced power electronics engineers to increase switching frequency, increase output capacitance and/or decrease output inductance to improve the dynamic response of voltage regulator modules (VRMs).

Furthermore, since conventional linear controllers are designed using an approximate small-signal model, it is impossible to precisely predict the converter response to an arbitrary large-signal disturbance (such as a rapid load variation, as observed in typical VRM applications). Output filter design for converters with conventional controllers is usually performed using approximations or trial-and-error procedures.

In order to improve the dynamic response of VRMs and address the bandwidth limitations associated with conventional controllers, several analog non-linear controllers have been presented in [1-4].

A hysteretic controller, based on the output inductor current, is presented in [1]. This type of controller is capable of improving dynamic response by eliminating the need of compensation circuitry. Without the compensator, the bandwidth of the converter is significantly improved. Unfortunately, hysteretic current-mode controllers operate at unpredictable frequencies making electromagnetic compatibility (EMC) design difficult. Furthermore, it is shown in [2] that due to non-idealities of the output capacitor (ESR and ESL) combined with the inherent delay of hysteretic comparators, the steady-state error of current-mode hysteretic converters can be significant. Also, it is very difficult to determine the converter's response (voltage deviation, recovery time) to a rapid load current variation.

Output voltage ripple hysteretic controllers are presented in [3-4]. Like current-mode hysteretic controllers, these controllers improve the dynamic response but are much more intuitive and simpler to implement. Unfortunately, they all possess at least one of the following undesired attributes: 1) Variable switching frequency, 2) Non-zero steady-state error, 3) Operating frequencies largely dependant on the equivalent series resistance (ESR) of the output capacitor. In addition, it is difficult to predict the settling time using these controllers since the converters typically over-compensate for a load current variation.

In [5], an analog control method is presented that combines a conventional linear scheme (for steady-state operation) with a non-linear hysteretic-type scheme (for transient operation). This method successfully improves the dynamic response without sacrificing fixed-frequency operation or zero steady-state error. However, as with output ripple hysteretic converters, this method tends to over-compensate for load current-variations resulting in long, unpredictable settling times.

It is presented in [6], that for a VRM reacting to a rapid load current variation, an "optimal response" exists that can minimize both the voltage deviation and the settling time of a converter. In [6], a method is presented to design a linear controller that attempts to mimic this optimal response. While this controller can produce a near-optimal response, it is impossible for a linear controller to accurately achieve the desired optimal response since the response is, in fact, non-linear.

One of the main advantages to digital control is its ability to perform complex arithmetic in order to implement non-linear control methods. In [7], equations to determine the optimal response to a disturbance are presented. The optimal response, to a large range of disturbances, is calculated using MATLAB offline and programmed into a digital controller. The controller successfully achieves a minimal, predictable settling time to an external disturbance. Unfortunately, the controller is only functional in open-loop configuration and the time instant when

1-4244-0714-1/07/$20.00 ©2007 IEEE.

the disturbance occurs and the magnitude of the load variation must be defined in advance which is an impossible situation for VRMs.

In [8], a novel digital controller is presented that is able to detect a rapid load transient and calculate the optimal response online. Not only does this controller allow the converter to respond to a disturbance with low voltage deviation and low settling time, but the converter's response is predictable within a range. This feature allows a power electronics engineer to design the output filter with certainty that the dynamic response criteria will always be satisfied.

This paper outlines the general controller operation introduced in [8] and derives the settling time and the voltage deviation of an optimally-controlled converter.

This paper presents a typical design example and presents simulation and experimental results verifying the controller operation and design procedure.

II. Controller Operation

The proposed controller uses a traditional linear controller during steady-state conditions and a non-linear controller during transient conditions. When the load current of a VRM changes rapidly, the output voltage of the converter will deviate from the reference voltage. The controller samples the voltage once per switching cycle and compares it with a pre-determined threshold. If the threshold is exceeded, the controller determines that the load current has changed and the controller switches to large-signal, non-linear mode.

The main concept of the optimal controller is to:

i) detect a load transient
ii) initially set the duty cycle to 100% (for a positive load step) or 0% (for a negative load step) for a certain amount of time (to be determined)
iii) change the duty cycle from 100% to 0% (or from 0% to 100%) for a certain amount of time (to be determined)
iv) return to steady-state, linear operation

Figure 1 depicts the conventional response and the optimal response to a positive load current step change. When the load current steps for a Buck converter, the inductor current cannot change instantaneously, therefore the capacitor current must supply the remaining current. This causes the capacitor to discharge and the voltage to deviate from the reference voltage.

By saturating the duty cycle to either 0% or 100% for t_1, the inductor current can travel toward the output current at its maximum slew rate, thereby minimizing the voltage deviation.

To limit the settling time, the inductor current should reach its new steady state value at the exact moment that the output voltage returns to its reference at T_b (see figure 1b). According to the principle of capacitor charge balance, in order for $v_c(T_a)$ (at the beginning of the transient) to equal $v_c(T_b)$ (at the end of the transient), equation (1) must be satisfied.

$$v_c(T_b) - v_c(T_a) = 0 = \frac{1}{T_b - T_a}\int_0^{T_b - T_a}\left[i_L(t) - i_o(t)\right]dt \qquad (1)$$

In other words, the charge delivered to the capacitor must be equal to the charge removed from the output capacitor at the

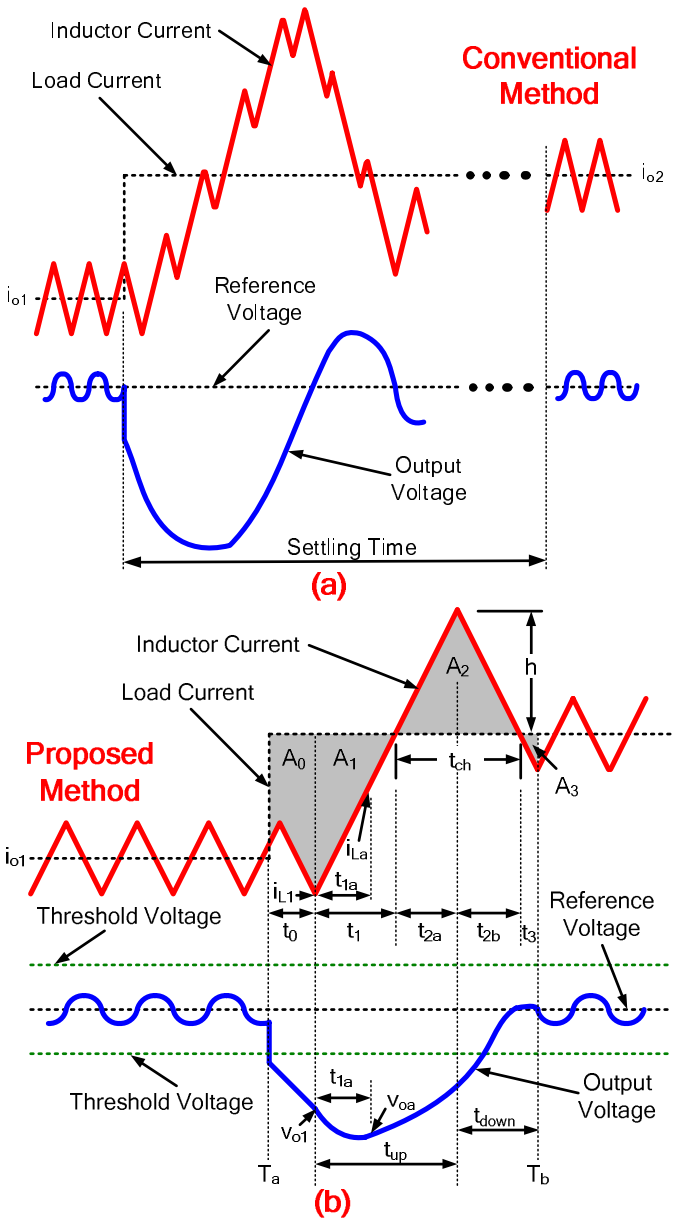

Figure 1: Conventional response to rapid load current transient (a), Optimal response to a load current transient (b)

$$A_0 + A_1 + A_3 = A_2 \qquad (2)$$

end of the transient period. Referring to figure 1b), in order for the output voltage to recover at T_b, (2) must be satisfied.

Since the discharge portion A_1 has been minimized, the recharge portion A_2 is also minimized. The settling time is dependant on the time required to recharge the capacitor. In order to minimize the settling time, the time required to provide charge A_2 must be minimized. Referring to figure 1b), the time required to recharge the capacitor t_{ch}, can be minimized by maximizing the height h (determined by t_{up}) of the A_2 triangle. This is accomplished by setting the duty cycle to 100% for t_{up} and 0% for t_{down}.

The main goal of the proposed controller is to accurately calculate t_{up} and t_{down} such that (2) is satisfied.

A brief description of the controller's calculation method of t_{up} and t_{down} for a positive load current step is as follows:

Step 1: Estimate new load current (i_{o2})

By sampling the output voltage and inductor current response over t_{1a} the new load current can be estimated by (3).

$$i_{o2} \approx \frac{1}{2}(i_{L1} + i_{La}) - \frac{C(v_{oa} - v_{o1}) - C(i_{La} - i_{L1})ESR}{t_{1a}} \quad (3)$$

Step 2: Estimate capacitor discharge portion A_0

The discharge portion A_0 (caused by the controller delay) is estimated using (4).

$$A_0 \approx C\left(V_{ref} - v_{o1} + (i_{L1} - i_{o2})ESR\right) \quad (4)$$

Step 3: Calculate t_1 and A_1

For a Buck converter, the inductor current slew rates are $dI_L/dt=(V_{in}-V_o)/L$ when the control FET is on, and $dI_L/dt=-V_o/L$ when the control FET is off. Therefore, t_1 and A_1 are calculated in (5) and (6) respectively.

$$t_1 = \frac{(i_{o2} - i_{L1})L}{V_{in} - V_o} = \frac{\left(i_{o2} - i_{o1} + \frac{1}{2}i_{rip}\right)L}{V_{in} - V_o} \quad (5)$$

$$A_1 = \frac{1}{2}t_1(i_{o2} - i_{L1}) \quad (6)$$

Step 4: Calculate t_3 and A_3

The inductor ripple current of a Buck converter is estimated in (7).

$$i_{rip} \approx \frac{(V_{in} - V_o)t_s \cdot V_o}{V_{in} \cdot L} \quad (7)$$

t_3 and A_3 are calculated in (8) and (9) respectively.

$$t_3 = \frac{i_{rip} \cdot L}{2V_o} \quad (8)$$

$$A_3 = \frac{1}{4}t_3 \cdot i_{rip} \quad (9)$$

Step 5: Calculate t_{2a} and t_{2b}

Through geometric inspection, it is possible to calculate t_{2a} and t_{2b} such that (2) is satisfied. t_{2a} and t_{2b} are calculated in (10) and (11) respectively.

$$t_{2a} = \sqrt{\frac{A_0 + A_1 + A_3}{\frac{1}{2}\frac{V_{in}}{V_o}\frac{V_{in} - V_o}{L}}} \quad (10)$$

$$t_{2b} = \frac{V_{in} - V_o}{V_o}t_{2a} \quad (11)$$

In order to achieve optimal dynamic response, the rise time $t_{up} = t_1 + t_{2a}$ and the fall time $t_{down} = t_{2b} + t_3$ is calculated.

The controller uses the calculated times to drive the converter to recover in the shortest possible time. At the end of t_3 the converter is considered recovered and switches back to linear operation.

For a negative current step change, the optimal response is calculated in a similar manner and will not be discussed in this paper.

III. Dynamic Response Analysis

In addition to improving the dynamic performance of a converter, the optimal controller also simplifies the design of the output filter since its response to a large-signal load transient is predictable. The only unknown variable is the time instant when the load current changes. Since digital controllers measure the output voltage at a finite sampling frequency, the sampling delay effects the response of the controller and converter, as shown in figure 2.

The best case occurs when the voltage deviation exceeds the threshold immediately before the sampling moment T_{samp1} as shown by the blue curve; therefore, the controller is able to react to the load current change at the next switching period T_{s1}. On the other hand, the worst case occurs when the voltage deviation exceeds the threshold immediately following T_{samp1} as shown by the red curve; therefore, the controller detects the load current change at T_{samp2} and reacts one switching period later at T_{s2}.

For the best case scenario, $t_0 = T_{s1} - T_{samp1}$ (i.e. the sampling delay). For the worst case scenario, $t_0 = T_{s2} - T_{samp1}$ (i.e. the sampling delay plus one switching period). Assuming that the load current step is large compared to the inductor current ripple, A_0 is estimated in (12).

$$A_0 \approx t_0 \cdot (i_{o2} - i_{o1}) \quad (12)$$

Although it is impossible to predict the exact dynamic response to a load current step due to the uncertainty of the load step time, it is possible to derive a range. Prudent designers can therefore use the worst case scenario as a guide to build a Buck converter.

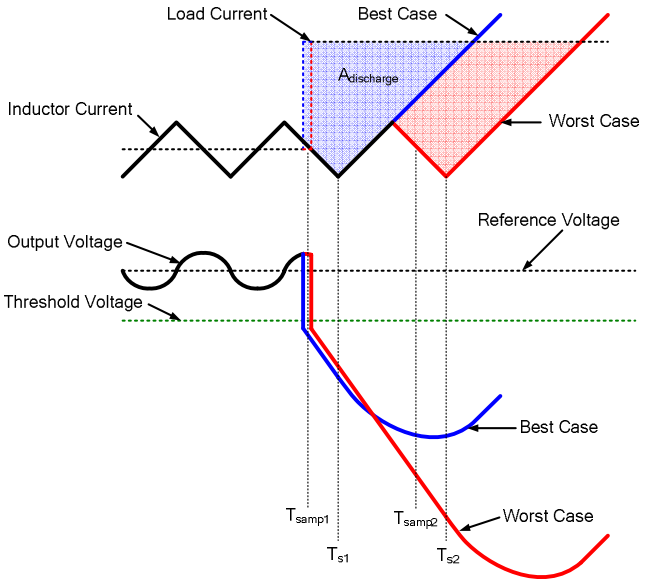

Figure 2: Best Case vs. Worst Case Response for Positive Load Transient

A. Recovery Time

Using equations (5)-(12), it is possible to determine the ideal values for t_{up} and t_{down}. However, the digital controller adjusts the last duty cycle in order to allow the inductor current to reach its new steady-state value in sync with the switching frequency. This is depicted in figure 3.

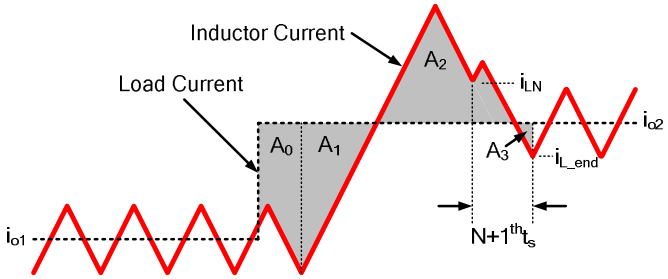

Figure 3: Inductor current in sync with switching period

The last duty cycle is calculated in (13).

$$d_{N+1} = \frac{V_o \cdot t_s + (i_{L\_end} - i_{LN}) \cdot L}{V_{in} \cdot t_s} \tag{13}$$

$i_{Lend} = i_{o2}$-½i_{rip} and t_s equals the switching period. Therefore, the total recovery time is described in (14).

$$t_{recovery} = t_0 + \left\lceil \frac{t_{up} + t_{down}}{t_s} \right\rceil \cdot t_s \tag{14}$$

It is noted that the recovery time of the optimal controller is only dependant on the current step magnitude, the sampling delay and the output inductor. The recovery time is independent from the output capacitance.

B. Voltage Deviation

It is evident in figure 1 that the capacitor is discharging during time periods t_0 and t_1. However, as demonstrated in figure 4, although the capacitor charge is at its minimum at the end of t_1 (T_{c_min}), the maximum output voltage deviation occurs sometime before the end of t_1 due to ESR effects.

The output voltage over the time period t_1 (letting *Point 1* = t = 0) is derived in (15).

$$v_o(t) = V_{ref} - \frac{A_0}{C} - ESR\left(I_1 - \frac{(V_{in} - V_o)t}{L}\right) - \frac{\frac{1}{2}\left(\frac{I_1^2 L}{V_{in} - V_o} - \left(\frac{I_1 L}{V_{in} - V_o} - t\right)\left(I_1 - \frac{(V_{in} - V_o)t}{L}\right)\right)}{C}$$

$$v_o(t) = V_{ref} - \frac{A_0}{C} - \frac{2ESR \cdot C(V_o t + I_1 L - V_{in} t) - t^2(V_{in} - V_o) + 2L \cdot I_1 t}{2L \cdot C} \tag{15}$$

where V_{ref} represents the reference voltage of the converter and I_1 represents the output current step plus one half of the inductor current ripple ($I_1 = \Delta I_o + ½ I_{L\_ripple}$).

In order to determine T_{min}, it is necessary to calculate the derivative of the output voltage with respect to time, as derived in (16).

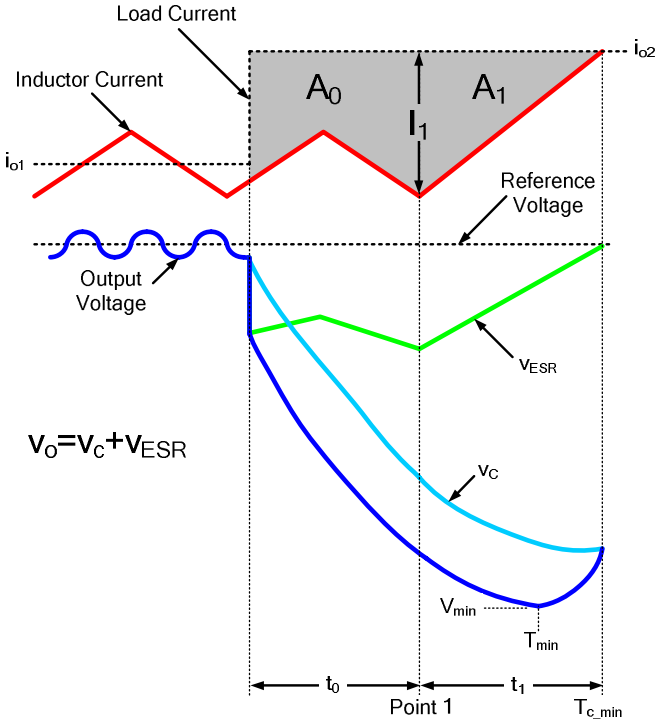

Figure 4: ESR effect on output voltage

$$\frac{dv_o}{dt} = \frac{ESR \cdot C(V_{in} - V_o) + t(V_{in} - V_o) - I_1 L}{L \cdot C} \tag{16}$$

By setting (16) equal to zero and solving for t, T_{min} is calculated in (17).

$$T_{\min} = \frac{ESR \cdot C(V_o - V_{in}) + I_1 L}{V_{in} - V_o} \tag{17}$$

By substituting (17) into (15), V_{min} is solved in (18).

$$V_{\min} = v_o(T_{\min}) = V_{ref} - \frac{A_0}{C} - \frac{ESR^2 \cdot C^2(V_{in}^2 - 2V_{in}V_o + V_o^2) + I_1^2 L^2}{2(V_{in} - V_o)L \cdot C} \tag{18}$$

Therefore, solving for (14) and (18) will determine the settling time and voltage deviation for a given converter and a given load current step.

IV. Design Example

A Buck converter VRM is required with the following parameters: V_{in}=5V, V_{out}=2.5V, F_s=400kHz, ESR=1mΩ I_{rip}=3.2A, Sampling delay = 1.125us. The sampling delay refers to the time between the sampling moment and the next switching cycle. The load steps rapidly at increments of 5A. Using (5)-(12) and (14), the best case and worst case recovery times for a positive 5A step is plotted in figure 5 for a range of inductor values.

For the desired ripple current of 3.2A, an output inductance of 1uH is chosen. It is shown in figure 5 that a 1uH inductance will result in a best case recovery time of 11.25us and a worst case recovery time of 13.75us.

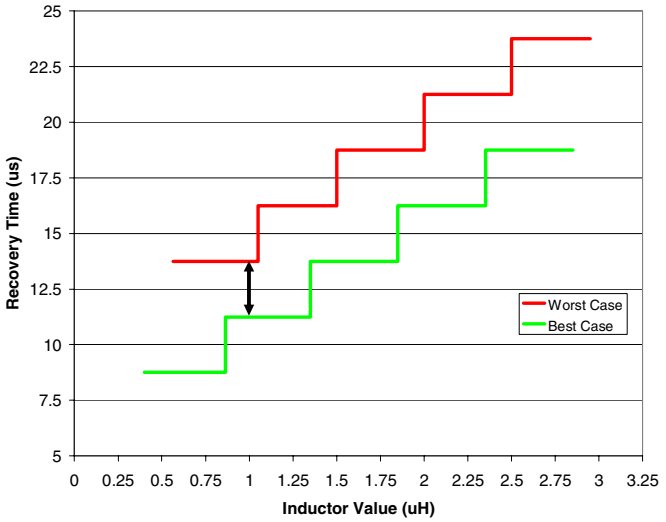

Figure 5: Recovery time of a converter undergoing a positive 5A load step

Using (12) and (18), the voltage dip due to a 5A positive current step change can be calculated. Figure 6 and figure 7 show the best case and worst case voltage dips (for a 5A positive current step) respectively.

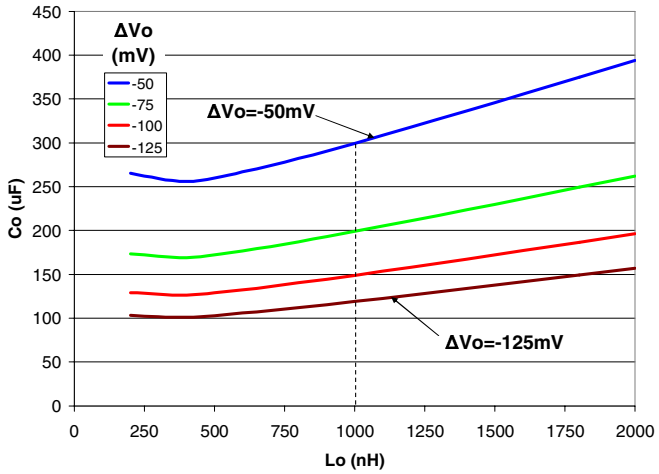

Figure 6: Best case voltage dip for positive 5A current step

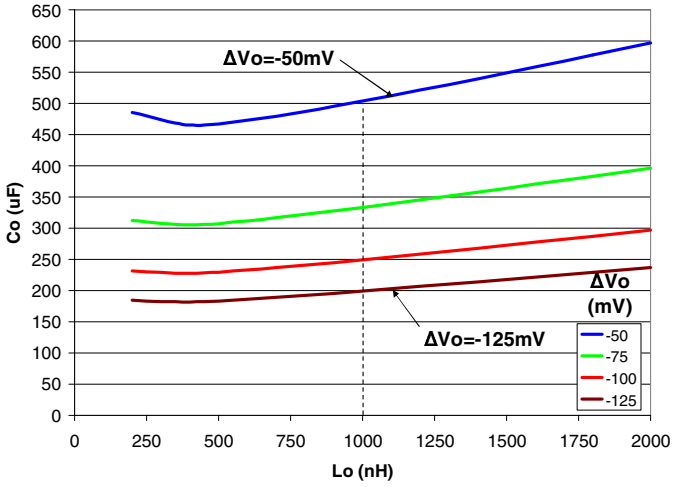

Figure 7: Worst case voltage dip for positive 5A current step

Assuming that a maximum voltage dip of 125mV is allowed, it can be observed from figure 7 that, for an output inductor of 1uH, an output capacitance of 200uF is required. It can be observed from figure 6 that an output capacitance of 200uF will result in a best case voltage dip of 75mV. Without any further iteration, the designer can be confident that the converter will meet the dynamic response criteria.

Figure 8 shows the worst-case output capacitance requirement for various positive current step magnitudes (with an inductor value of 1uH).

For example, in order to limit the voltage deviation to within 100mV under a 10A current step change, the required output capacitance would be 430uF.

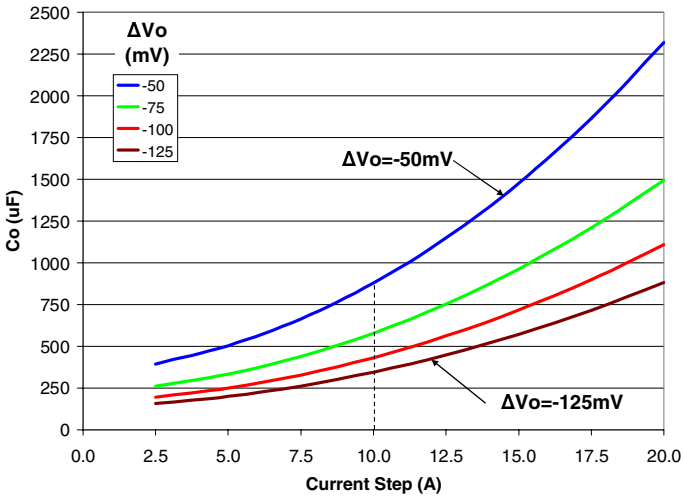

Figure 8: Worst case voltage dip for various positive current steps

In this design example, the sampling frequency was equal to the switching frequency. By increasing the sampling frequency and/or decreasing the sampling delay, the difference between the best case and the worst case scenario would be reduced. This would result in a tighter prediction range of the voltage deviation and recovery time.

V. Simulation Results

In order to verify the derived equations, the converter designed in section IV was simulated using MATLAB. The filter parameters chosen were: L=1uH and C=235uF. According to figure 6 and figure 7, the best case and worst case voltage dips are 65mV and 105mV respectively. The simulated converter was tested with a 5A→10A step change. Figure 9 and figure 10 shows the simulation results for both the best and worst case scenarios respectively.

As shown in figure 9 and figure 10, the simulation results are consistent with the analytical results. It is noted that the worst case simulated voltage dip is slightly less than the calculated voltage dip. This small discrepancy is due to the assumption used to calculate A_0 in (12).

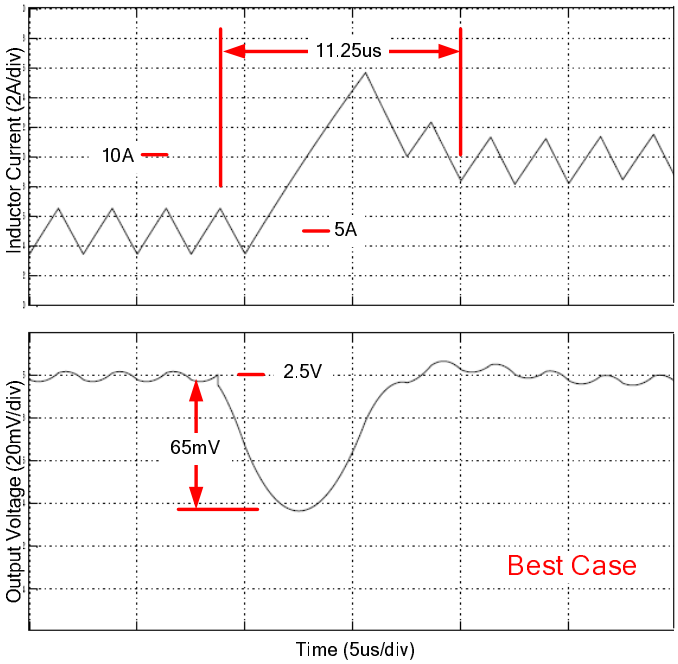

Figure 9: Best case simulation of a 5A→10A load current step change

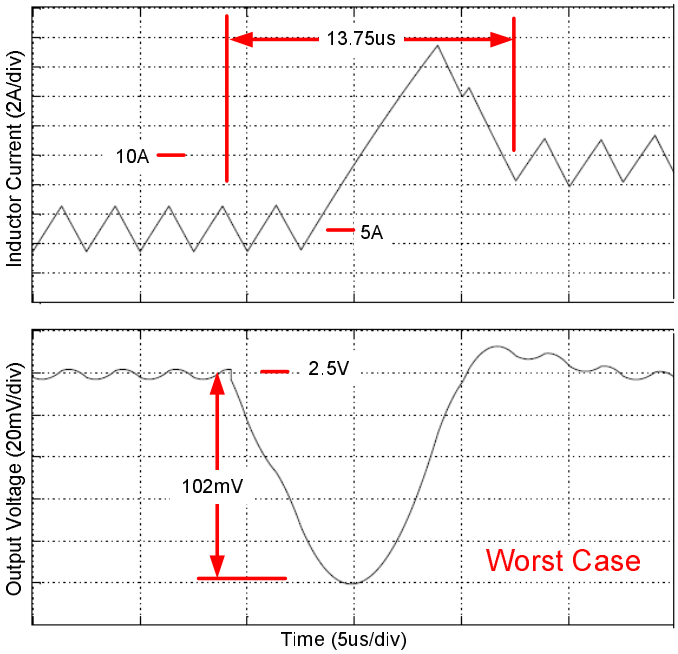

Figure 10: Worst case simulation of a 5A→10A load current step change

It is noted that the optimal controller relies on output filter information. The output filter components may possess a tolerance typically around +/-20%. Figure 11 shows the best-case output voltage response to a positive 5A output current step when the capacitor information is incorrect.

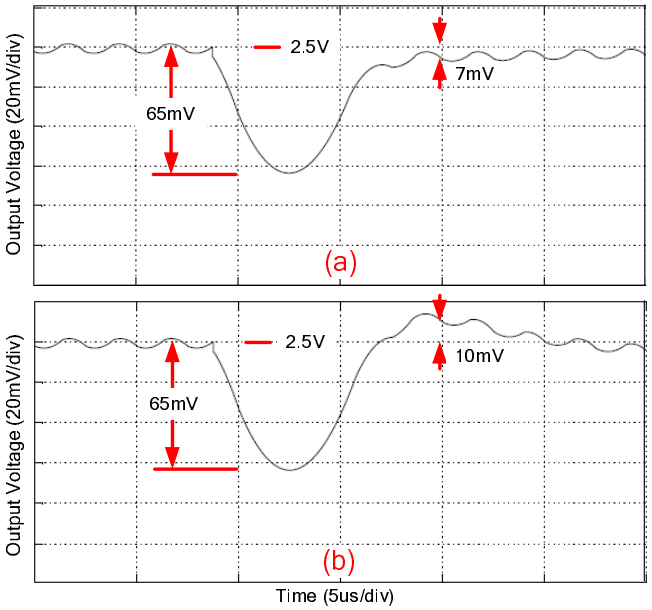

Figure 11: Best case simulation of a 5A→10A load current step change with incorrect capacitor information a) controller C= -20% of nominal b) controller C=+20% of nominal

It is shown in figure 11 that the capacitor tolerance does not affect the voltage dip of the converter. However, it is observed that the voltage does not precisely equal the reference voltage when the controller switches back to steady-state mode. This may result in a couple extra switching cycles before the transient settles (depending on the steady-state controller parameters).

VI. Experimental Results

A buck converter was built and tested with the following parameters: V_{in}=5V, V_{out}=2.5V Rated power=25W, L=1uH, C=235uF, ESR=1mΩ and fs=400kHz. During steady-state conditions, the converter was controlled by a digital current-mode PID controller with a bandwidth of 70kHz and a phase margin of 50º. During transient conditions, the converter was controlled by the optimal controller.

A Xilinx Spartan 2E development board field programmable array (FPGA) with a clock speed of 200MHz was used to implement the optimal control algorithm.

Figure 12 shows the output voltage response of the aforementioned converter undergoing a 0A→5A load step change with the optimal controller disabled (i.e. the dynamic response of the current-mode controller).

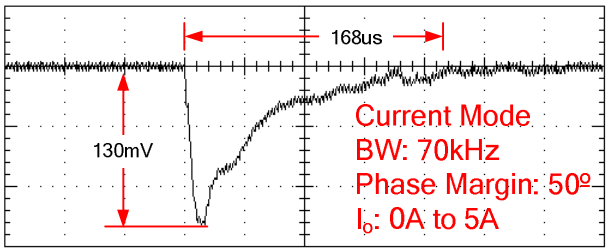

Figure 12: Current-mode PID controller response to a 0A→ 5A load current step (X-axis: 40us/div; Y-axis: 50mV/div)

Figure 13 shows the output voltage response of the converter undergoing a 0A→5A load step change with the optimal controller enabled.

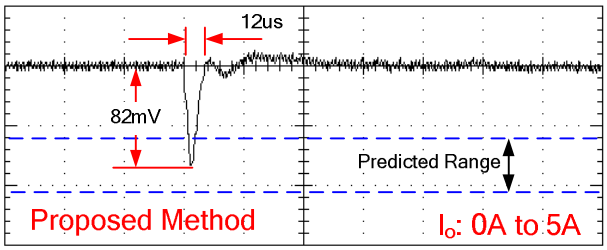

Figure 13: Optimal controller response to a 0A→ 5A load current step (X-axis: 40us/div; Y-axis: 50mV/div)

Figure 13 demonstrates that the dynamic response can be accurately predicted within a range when using the optimal controller. The voltage undershoot of the optimally controlled converter was 82mV. This is within the predicted range of 65mV-105mV. The recovery time of the optimally controlled converter was 12us. This is within the predicted range of 11.25us-13.75us.

Furthermore, it is noted in figure 12 and figure 13 that the voltage undershoot is reduced from 130mV using the PID controller to 82mV using the optimal controller (a reduction of 37%). The recovery time is reduced from 168us using the PID controller to 12us using the optimal controller (a reduction of 93%).

Figure 14 shows the output voltage response of the aforementioned converter undergoing a 5A→10A load step change with the optimal controller disabled (i.e. the dynamic response of the current-mode controller).

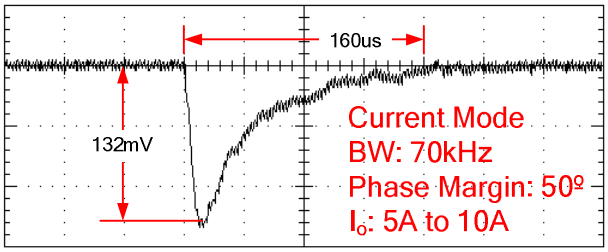

Figure 14: Current-mode PID controller response to a 5A→ 10A load current step (X-axis: 40us/div; Y-axis: 50mV/div)

Figure 15 shows the output voltage of the converter undergoing a 5A→10A load step change with the optimal controller enabled.

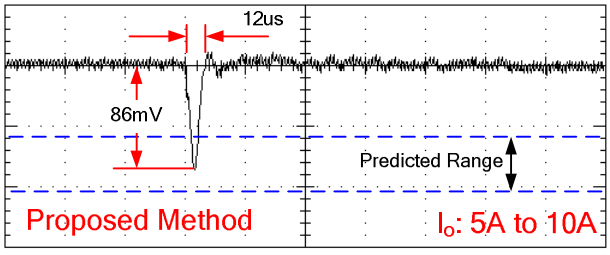

Figure 15: Optimal controller response to a 5A→ 10A load current step (X-axis: 40us/div; Y-axis: 50mV/div)

The voltage undershoot of the optimally controlled converter was 86mV. This is within the predicted range of 65mV-105mV. The recovery time of the optimally controlled converter was 12us. This is within the predicted range of 11.25us-13.75us.

It is noted in figure 14 and figure 15 that the voltage undershoot is reduced from 132mV using the PID controller to 86mV using the optimal controller (a reduction of 35%). The recovery time is reduced from 160us using the PID controller to 12us using the optimal controller (a reduction of 92%).

VII. Conclusion

A novel combination linear and non-linear digital controller is demonstrated in this paper. The controller significantly improves the dynamic response of a Buck converter by calculating, in real time, the optimal response to a load current step.

Since the converter response to a load current step change is predictable under the proposed digital controller, it is possible to simply and accurately design a converter to meet arbitrary dynamic response requirements. It is proven, through simulation and experimentation, that the dynamic response of a converter will always operate within the best case and worst case calculated range. This greatly simplifies the design process since the designer can predict the best case and worst case response of a closed loop system.

VIII. References

[1] S. B. Arbetter, D. Maksimovic, "DC-DC Converter with Fast Transient Response and High Efficiency for Low-Voltage Microprocessor Loads", IEEE 13th Annual Aplied Power Electronics Conference and Exposition (APEC 98), Vol. 1, pp. 156-162

[2] C. Song, J.L. Nilles, "Accuracy Analysis of Hysteretic Current-Mode Voltage Regulator", IEEE 20th Annual Applied Power Electronics Conference and Exposition (APEC 05) IEEE, Vol. 1 pp. 276 – 280

[3] J. Abu-Qahouq, H. Mao, I. Batarseh "Multiphase Voltage-Mode Hysteretic Controlled DC-DC Converter with Novel Current Sharing" IEEE Transactions on Power Electronics, Vol. 19, No. 6, Nov 2004, pp. 1397 – 1407

[4] J. Zhao, T. Sato, T. Nabeshima, T. Nakano, "Steady-state and Dynamic Analysis of a Buck Converter using a Hysteretic PWM Control", IEEE 35th Power Electronics Specialists Conference (PESC 04), Vol. 5 pp. 3654 – 3658

[5] A. Barrado, J. Quintero, A. Lazaro, C. Fernandez, P. Zumel, E. Olias, "Linear-Non-Linear Control Applied in Multiphase VRM", IEEE 36th Annual Power Electronics Specialists (PESC 05), pp. 904 – 909

[6] A. Soto, P. Alou, J.A. Oliver, J.A. Cobos, J. Uceda, "Optimal Control Design of PWM-Buck Topologies to Minimize Output Impedance", IEEE 17th Annual Applied Power Electronics Conference and Exposition (APEC 2002), pp. 426 – 432

[7] A. Soto, A. de Castro, P. Alou, J.A. Cobos, J, Uceda, A. Lofti, "Analysis of the Buck Converter for Scaling the Supply Voltage of Digital Circuits", IEEE 18th Annual Applied Power Electronics Conference and Exposition (APEC 2003), pp. 711 - 717

[8] G. Feng, E. Meyer, Y-F. Liu, "High Performance Digital Control Algorithms for DC-DC Converters Based on the Principle of Capacitor Charge Balance", IEEE 37th Power Electronics Specialists Conference (PESC 2006), TuA4-1.