

# A Novel Non-Isolated Full Bridge Topology for VRM Applications

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**Abstract** - In this paper a new topology is introduced to solve the narrow duty cycle and hard switching problems of the interleaved Buck converter voltage regulator module. The new topology is called the non-isolated full bridge (NFB). In comparison to the interleaved Buck converter, it operates with a significantly wider duty cycle and can achieve zero voltage switching at turn on for the high side MOSFETs. The NFB can significantly reduce the input peak current and transfers a portion of the primary side energy directly to the load thereby reducing the stress on the synchronous rectifiers and filter inductors. Experimental results and analysis demonstrate that the new non-isolated full bridge can significantly improve the performance of a VRM.

## I. INTRODUCTION

With the continued improvements in integrated circuit technology, next generation CPUs will operate at much higher clock frequencies, and consume more power. In the future, to reduce power consumption, CPUs will operate at supply voltages below 1V, with tight voltage tolerance, large current demand (above 100A), and require fast dynamic response (above 100A/ $\mu$ s) [1].

To meet these requirements for next generation CPUs, the voltage regulation modules (VRMs) will need to achieve, 1) high efficiency at high switching frequency, 2) fast dynamic response and 3) low component cost. The most popular topology for this application is the multi-phase interleaved Buck. The major obstacle for the multi-phase Buck to achieve these three goals is its extremely narrow duty cycle at output voltages approaching 1V and below.

To solve the aforementioned problems several new topologies have been proposed. The topologies proposed in [2]-[7] are Buck based topologies that use a coupled-inductor to extend the duty cycle. The major drawback of these topologies is that the voltage stress of the control MOSFET is higher than the input voltage, so an auxiliary circuit is often required to limit the voltage stress on the switches. Furthermore, these topologies operate in hard switching mode, so switching losses prevent them from being suitable candidates at very high switching frequencies.

To solve the problems of the conventional Buck and coupled inductor Buck topologies, In this paper a new non-isolated full bridge (NFB) topology is proposed with significant advantages, including soft-switching, reduced synchronous rectifier voltage stress and current stress. Compared with the topologies proposed in [9], the NFB has reduced current stress for the synchronous rectifiers and output inductors since a portion of the energy is transferred directly to the load. The new topology is presented and analyzed in the following sections.

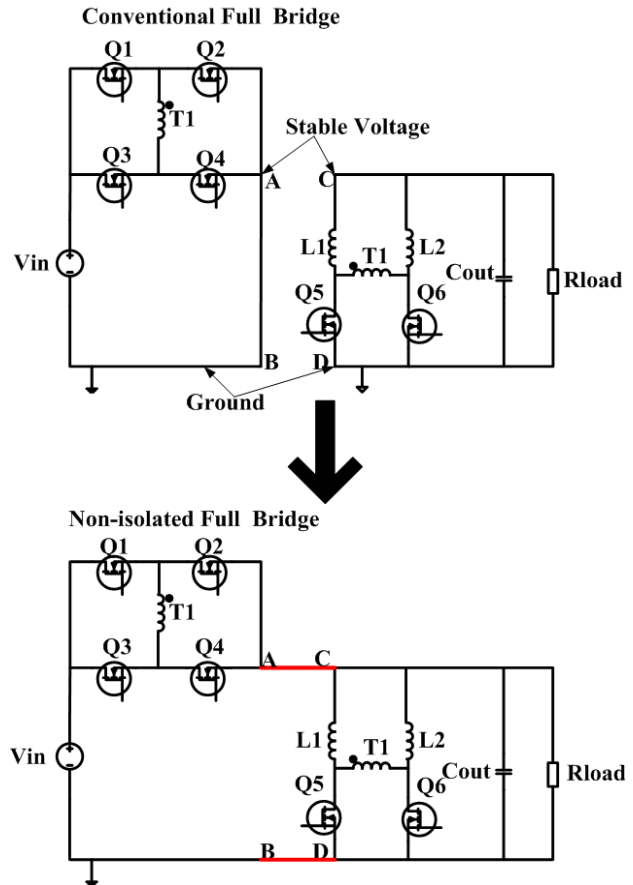


Fig 1 Evolution of the conventional full bridge to the new non-isolated full bridge

## II. DERIVATION AND OPERATION OF THE NON-ISOLATED FULL BRIDGE

The conventional full bridge and proposed non-isolated full bridge are shown in Fig 1 which illustrates the evolution of the new topology. For the conventional full bridge, the voltage at points A and C are stable DC voltages. The points B and D are primary and secondary ground, respectively. Since A and C are stable DC voltages, we can remove the connection between point A and B and connect A to C, and B to D, yielding the new non-isolated full bridge topology. There are three significant benefits of these topology changes:

- 1) The input current conducts directly to the load side, so the current stress on the synchronous rectifiers and inductors are reduced.
- 2) A portion of the load energy is not transferred by the transformer, so its associated losses decrease.
- 3) When the two primary low side MOSFETs, Q2, Q4, is turned off, their gate voltage is  $-V_o$ , so they can be

turned off faster with reduced turn off loss.

The modes of operation of the NFB operating in phase-shift mode are presented in the following sub-sections. The key waveforms illustrating the five modes from T0-T5 are illustrated in Fig 2. And the output voltage is defined by (1) ( $D=T_{on}/T_s$ ,  $N=N_p/N_s$ )

$$V_o = \frac{V_{in} D}{2N + D} \quad (1)$$

From (1) we can see that after add a transformer, we can easily adjust the duty cycle, for example when  $V_{in}=12V$ ,  $V_o=1V$ ,  $N=3$ ,  $D=0.545$ , compare with Buck the duty cycle increase 5 times.

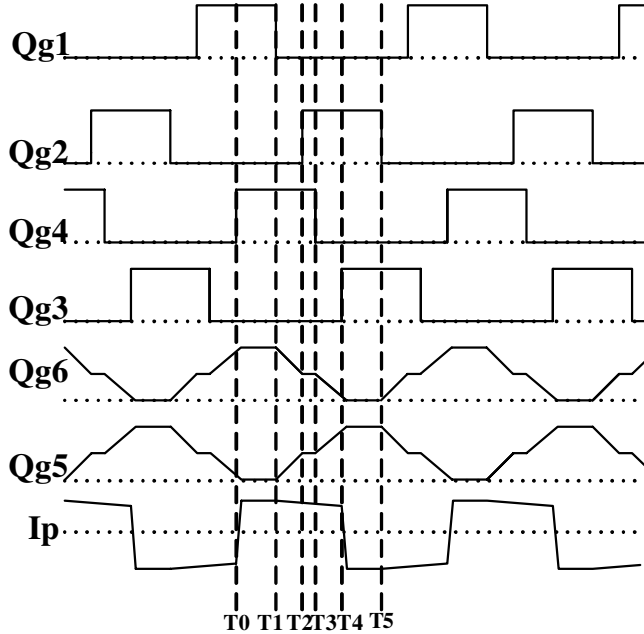


Fig 2 Key waveforms of the five modes of operation

#### A. Mode 1 [T0~T1]

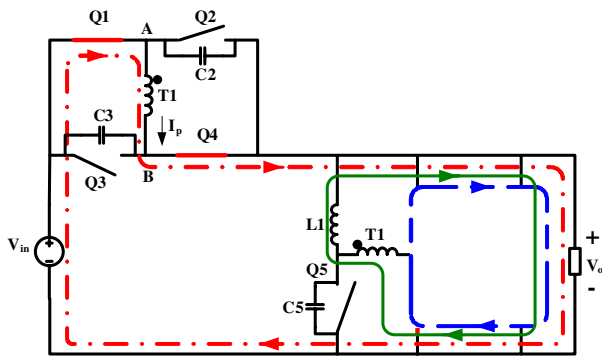


Fig 3 The operation mode of NFB during time interval T0-T1.

The first mode is illustrated in Fig 3. From time T0 to T1, Q1, Q4 and Q6 are on. Q2, Q3 Q5 are off; the voltage across Q2 and Q3 is  $V_{in}-V_o$ . The current in L1 increases and the current in L2 decreases. Energy flows from the input to the load. In Fig 3 we can see that the input current goes directly to

the load side, and the current stress of the synchronous rectifier is reduced as a result.

#### B. Mode 2 [T1~T2]

The second mode is illustrated in Fig 4. From time T1 to T2, Q1 is turned off at T1 to prepare the zero voltage turn on of Q2. The current reflected from the secondary side charges C1 and discharges C2. The currents decrease in both L1 and L2. During this time interval, the voltage at point A decreases from  $V_{in}$  to  $V_o$ . When the voltage at point A decreases to  $V_o$ , the voltage across Q2 is zero. If Q2 is turned on at this time, zero voltage turn on can be achieved. Q5 also is turned on during this transition, and it begins to share the load current after the voltage across Q2 is reduced to zero. If the self-driven circuit proposed in [8] is used, Q5 is turned on before it begins to conduct the inductor current, so its body diode does not conduct during this transition. During this time interval the current reflected from the secondary side is used to charge and discharge the output capacitors of Q1 and Q2, it is easier for Q1 and Q2 to achieve ZVS compared to the lagging leg (Q3 and Q4).

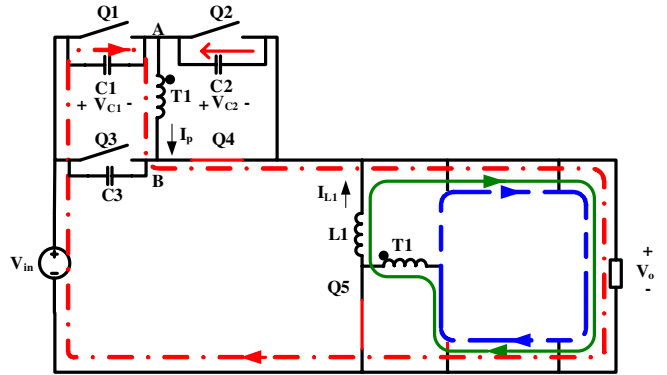


Fig 4 The operation mode of NFB during time interval T1-T2.

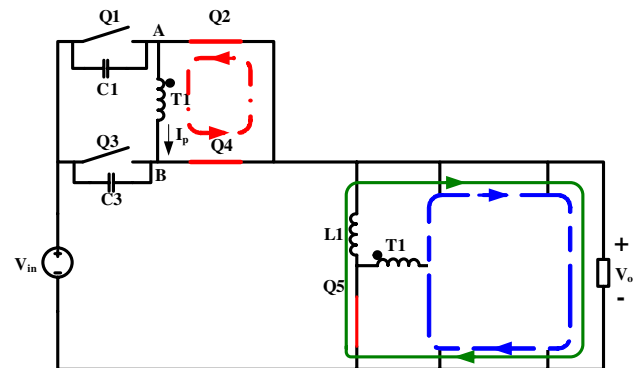


Fig 5 The operation mode of NFB during time interval T2-T3

#### C. Mode 3 [T2~T3]

The third mode is illustrated in Fig 5, for time T2 to T3. After the voltage across Q2 reaches zero, Q2 is turned on at T2. Since at this time the secondary side of the transformer is shorted, the primary and secondary

sides of the transformer are decoupled, and the current in both inductors decreases. The load energy is provided by the output capacitance and output inductors.

#### D. Mode 4 [T3~T4]

The fourth mode is illustrated in Fig 6. From time T3 to T4, Q4 is turned off at T4 to prepare the zero voltage turn on of Q3. The energy stored in the leakage inductance of the transformer charges C4 and discharges C3, and voltage at point B increases from  $V_o$  to  $V_{in}$ . After the voltage increase to  $V_{in}$ , Q3 can achieve ZVS turn on. In order to achieve ZVS turn on of Q3, the energy stored in the leakage inductance must be sufficient to charge C4 to  $(V_{in}-V_o)$  and discharge C3 to zero volts.

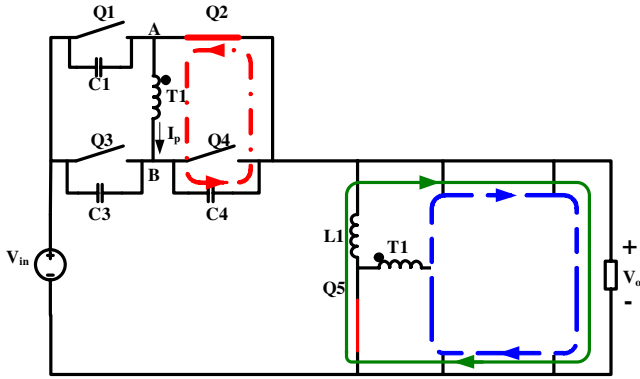


Fig 6 The operation mode of NFB during time interval T3-T4

#### E. Mode 5 [T4~T5]

The final mode is illustrated in Fig 7. From time T4 to T5, once the voltage across Q3 becomes zero, Q3 is turned on at T4. The primary current can not change direction instantly due to the transformer leakage inductance. During the interval, the primary current increases in the opposite direction of  $I_p$ , and the current in Q5 begins to increase and current in Q6 begins to decrease. If Q6 is turned off before the primary current changes from  $I_p$  to  $-I_p$ , its body diode begins to conduct. After the primary current changes from  $I_p$  to  $-I_p$ , the primary side begins to provide energy to the secondary side, and Q5 begins to conduct the full current in L1 and L2 and Q6 is turned off. At the end of T5, one switching period is complete.

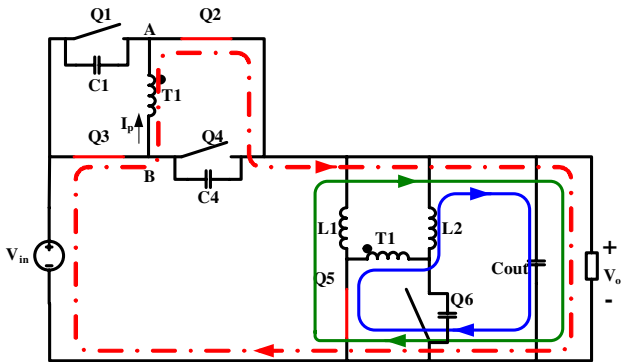


Fig 7 The operation mode of NFB during time interval T4-T5

### III. ZERO VOLTAGE SWITCHING ANALYSIS

In this section, the zero voltage switching requirements for the non-isolated full bridge are analyzed in detail for the leading and lagging legs.

#### A. Leading Leg Transition: Mode 2 [T1-T2]

$$t_{dead\_Q12} > \frac{2C1(V_{in} - V_o)N}{I_{L1}} \quad (2)$$

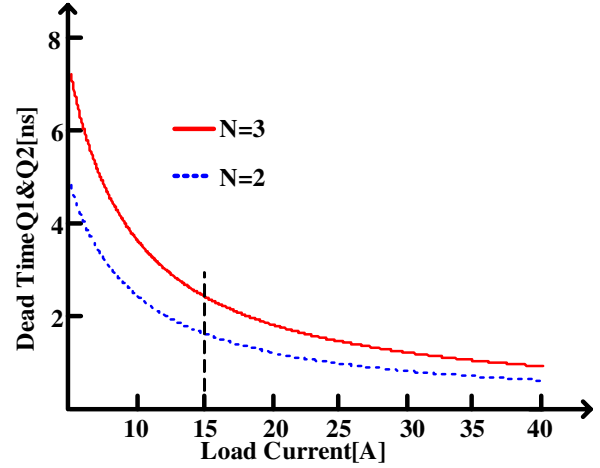


Fig 8 Dead time between Q1&Q2 required to achieve ZVS for the leading bridge leg as a function of load current

The transition paths of the leading leg are shown in Fig 4. Q1 is turned off to prepare for the zero voltage turn on of Q2. The current reflected from the secondary side charges C1 and discharges C2. During this transition the time needed to charge C1 to  $V_{in}-V_o$  and discharge C2 from  $V_{in}-V_o$  to zero voltage is dependent on the load current. Since this time interval is very short we can assume the charge current is constant during the transition. In Fig 8, the minimum dead time is calculated using (2) as a function of load current with  $V_{in}=12V$ ,  $N_p:N_s=3:1$  and  $N_p:N_s=2:1$ ,  $C1=250pF$ . Equation (2) is derived based on the assumption that during the transition of the Mode 2 [T1~T2], the current is constant to charge charges C1 and discharges C2. From Fig 8 we can observe that heavy load and a low turn's ratio can help the NFB achieve ZVS and at 15A load,  $T_d=2.4ns$  for  $N=3$  and  $1.6ns$  for  $N=2$

#### B. Lagging Leg Transition: Mode 4 [T3-T4]

The transition paths of the lagging leg are shown in Fig 6. Initially, Q4 is turned off to prepare the zero voltage turn on of Q3. If the energy stored in the leakage inductance of the transformer is sufficient to charge C4 to  $V_{in}-V_o$  and discharge C3 from  $V_{in}-V_o$  to zero, Q3 can achieve zero voltage turn on.

In this transition the leakage inductance resonates with C3 and C4. The equivalent circuit is shown in Fig 9. If the voltage at point B can be charged to  $V_{in}$ , the body diode of Q3 will turn on and clamp the voltage to  $V_{in}$ . In order to achieve ZVS turn on, Q3 must turn on before the current through the leakage inductance decreases to zero. Fig 10 shows the

minimum dead time between Q3 and Q4 calculated using (4), with  $V_{in}=12V$ ,  $V_o=1V$ ,  $C_3=250pF$ ,  $L_{Leakage}=30nH$ . It is clear that it is more difficult for the lagging leg to achieve zero voltage turn on in comparison to the leading leg.

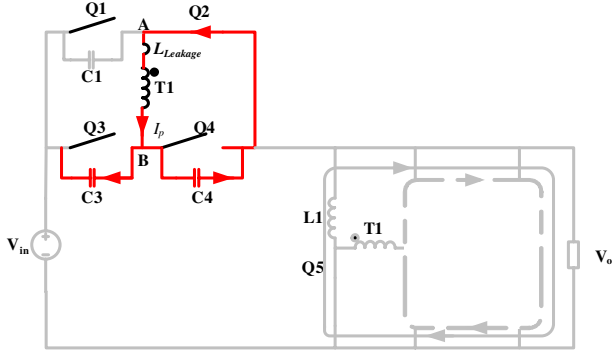


Fig 9 Equivalent circuit for lagging leg

$$Z_o = \sqrt{L_{Leakage} / 2C_3}$$

$$\omega = 1 / \sqrt{2L_{Leakage} C_3} \quad t_x = \frac{1}{\omega} \sin^{-1} \left( \frac{V_{in} - V_o}{Z_o} \right) \quad (3)$$

$$\left\{ \begin{array}{l} Z_o I_{Leakage \min} > (V_{in} - V_o) \\ \frac{1}{\omega} \sin^{-1} \left( \frac{V_{in} - V_o}{Z_o I_{Leakage}} \right) < t_{dead\_Q34} < \frac{(I_{Leakage} L_{Leakage}) \cos \alpha t_x}{(V_{in} - V_o)} + t_x \end{array} \right. \quad (4)$$

$$I_{Leakage} = I_{Lavg} / N \quad (5)$$

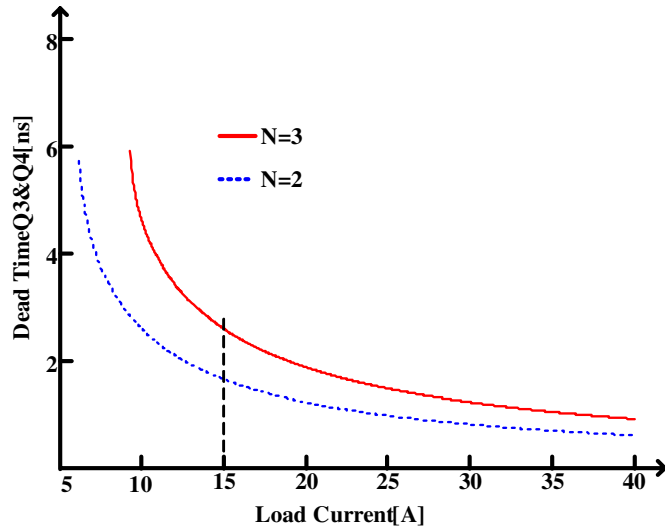


Fig 10 Lagging leg dead time between Q3 and Q4

Form Fig 10 we can see that at 15A load  $T_d=3.1ns$  for  $N=3$  and  $1.7ns$  for  $N=2$ .

#### IV. LOSS ANALYSIS AND COMPARISON

In this section, the losses of a two-phase synchronous Buck converter and the NFB are compared. It is demonstrated that

NFB is able to achieve higher efficiency than a two-phase Buck. In the comparison, the components used for the two-phase Buck and NFB and their operating conditions are the same.

#### A. Switching Loss Saved by Zero Voltage Switching and Duty Cycle Extension

In comparison to the two-phase Buck, the NFB operates with extended the duty cycle, so the primary peak current through the MOSFETs is significantly reduced thereby also reducing the switching loss. Fig 11 illustrates an example with the input voltage at 12V, output at 1V/40A, output inductor of 100nH and  $N_p:N_s=3:1$ . From the example, it is clear that the primary peak current is reduced from 24.5A for the Buck to 7.2A for the NFB. Furthermore, the voltage stress of the synchronous rectifiers is reduced from 12V for the Buck to 3.7V for the NFB.

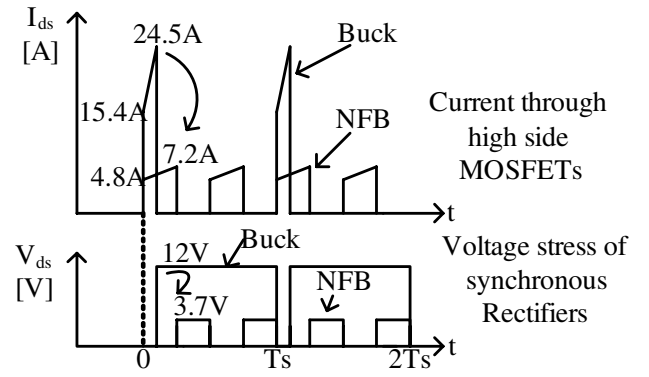


Fig 11 Peak current and voltage stress reduced by extend the duty cycle

As previously discussed, when operated in phase shift mode and if the control circuit is properly designed, the primary MOSFETs of NFB can achieve ZVS at turn on. Another benefit of the ZVS turn on is that the gate driving loss can be reduced since the  $Q_{gd}$  charge is eliminated. This can reduce the gate loss by at least 30% for the primary MOSFETs. It is expected that the switching loss of NFB is much less than the two-phase Buck when they operate at the same power level and switching frequency.

For example if we assume the turn on time is 14ns and the turn off time is 10ns then the switching loss for a two-phase Buck is 5.527W and 1.584W for the NFB calculated as follows:

$$P_{SW\_BUCK} = 0.5(1MHz)(12V)[(15.4A)(14ns) + (24.5A)(10ns)](2) = 5.527W$$

$$P_{SW\_NFB} = 0.5(1MHz)(12V-1V)(7.2A)(10ns)(4) = 1.584W$$

#### B. Synchronous Rectifier Body Diode Loss Savings

With the conventional Buck, a dead time must be added between the primary control MOSFET and synchronous MOSFET to prevent a short circuit. For the NFB, when self-driven synchronous rectification is used, the body diode conduction loss is significantly reduced since there is no need

to add dead time to prevent a short circuit. To drive the synchronous rectifiers, the self-driven circuit proposed in [8] was used for the NFB.

In the following sub-sections, the body diode conduction loss of the two-phase Buck and NFB are compared.

### 1) Leading Leg Transition for Rectification

The first mode is shown in Fig 12 corresponding to the transitions in Fig 4. The transition time of this interval is determined by the load current and can be calculated by using (3). When the primary winding voltage is zero, the secondary winding voltage is zero and Q5 begins to share the current initially handled by Q6, so the current in Q5 begins to increase, while the current in Q6 begins to decrease. Since Q5 is turned on before it begins to take over the current in Q6, its body diode does not conduct during this interval.

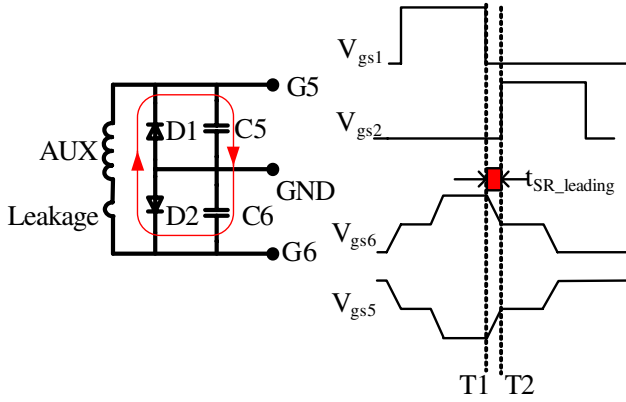


Fig 12 Leading leg transition for the self-driven synchronous rectifiers

### 2) Lagging Leg Transition for Rectification

The second mode is shown in Fig 13. Q4 is turned off to prepare for the ZVS turn on of Q3. The states of this mode are shown in Fig 6 and Fig 7. The energy stored in the leakage inductance of the transformer charges C4 and discharges C3. Since the two synchronous rectifiers are conducting, the primary windings and secondary windings are decoupled. After Q3 is turned on,  $V_{gs5}$  begins to increase and  $V_{gs6}$  begins to decrease. Meanwhile, the current in Q5 begins to increase and the current in Q6 begins to decrease while the primary side current begins to change direction. Before the primary current changes from  $I_p$  to  $-I_p$ ,  $V_{in}-V_o$  is applied across the leakage inductance reflected to primary. The body diode of Q6 begins to conduct when its gate voltage is reduced below the threshold voltage. After the primary side current changes to  $-I_p$ , the current in Q6 is reduced to zero and Q5 begins to conduct the full inductor current.

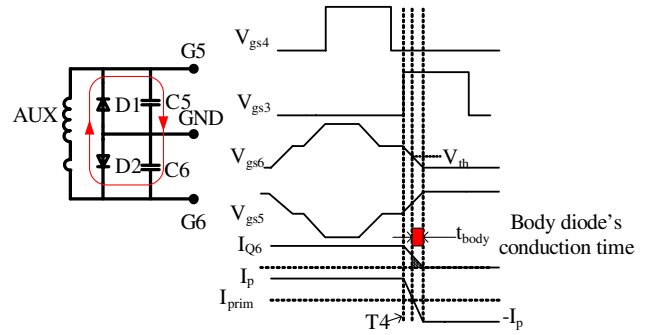


Fig 13 Lagging leg transition for the self-driven synchronous rectifiers

To simplify the analysis we will assume the gate voltage of Q5 and Q6 change linearly, which is valid as long as the synchronous rectifier gate resistances and the leakage inductance of the AUX winding can be neglected. Based on this assumption, when the primary side current linearly changes from  $I_p$  to  $-I_p$ ,  $V_{gs6}$  changes linearly from  $(V_{in}-V_o)N_{AUX}/2N_p$  to zero. Then, (6) can be used to calculate the body diode's conduction time.

$$t_{body} = \frac{2V_{th}(I_o - I_{in})L_{leak}N_s}{N_{AUX}(V_{in} - V_o)^2} \quad (6)$$

If a two-phase Buck operates at 1MHz, 1V/40A load, the body diode's forward voltage drop is 0.7V and the dead time between top and bottom switch is 20ns, total conduction loss for the body diode is:

$$P_{diode\_Buck} = (20A)(2)(20ns)(0.7V)(1MHz) = 0.56W$$

For the NFB, the threshold voltage is  $V_{th}=0.9V$ , and other parameters are,  $L_{leak}=30nH$ ,  $I_o=40A$ ,  $I_{in}=3.4A$ ,  $N_s=1$ ,  $N_{AUX}=3$ , then the conduction time for the body diode is 4.3ns as calculated by (6).

$$P_{diode\_Buck} = (18.35A)(2)(4.3ns)(0.7V)(1MHz) = 0.11W$$

From the calculation 0.45W energy is saved on the body diode's conduction loss.

### C. Summary

From the analysis in the previous sub-sections, the major advantages of new topology are that it can reduce switching loss and body diode's conduction loss yielding improved efficiency.

The efficiencies of the two-phase Buck and NFB have been calculated. The efficiency curves are shown in Fig 14. In the calculations, IRF7821 was used for the primary MOSFETs and FDS6162N7 was used for the synchronous rectifiers. The output is 1V/40A. As shown in Fig 14, the NFB is able to achieve the same efficiency, 84.6% as a two phase Buck but at more than double the switching frequency (i.e. 430kHz for the Buck and 1MHz for the NFB).



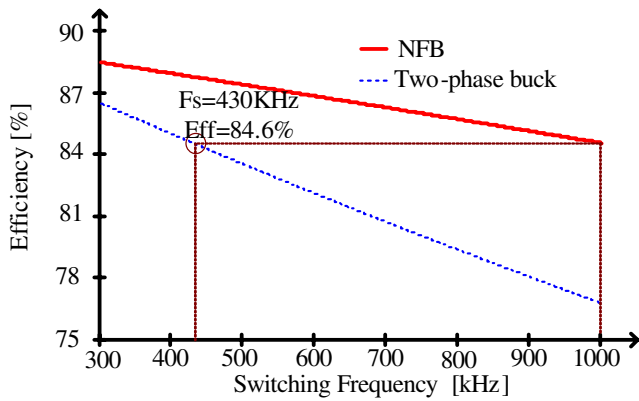


Fig 14 Calculated efficiency of a two-phase Buck and NFB at 1V/40A

### V. EXPERIMENTAL RESULTS

Prototypes of the NFB and two-phase synchronous Buck at 12V input 1V/40A output were designed and built to operate at frequencies between 500kHz and 1MHz. The NFB prototype was built on a 1.41 inch by 1.41 inch, 12 layer, 2oz copper printed circuit board. A photo of the prototype is shown in Fig 15. In order to demonstrate the advantages of this topology, the efficiency of the new topology is measured at 1V, 500kHz, 700kHz and 1MHz switching frequency.

The high side MOSFETs used in the design were IRF7821 since they have very low gate charge to minimize switching loss. The synchronous rectifier MOSFETs used were FDS6162N7 since they have very low on resistance which minimizes conduction loss.

Waveforms of the synchronous rectifier gate signals are shown in Fig 16. From the testing results shown in Fig 17 and Fig 18, we can see that the both leading leg and lagging leg are able to achieve ZVS turn on.

The efficiency as a function of load for the NFB is illustrated in Fig 19 for switching frequencies of 500kHz, 700kHz and 1MHz. A comparison is made for the efficiency as a function of load for the NFB and a two-phase synchronous Buck as illustrated in Fig 20 at 500kHz switching frequency for the Buck and 1MHz for the NFB. From the test results shown in Fig 19 and Fig 20 it is observed that at 30A load the non-isolated full bridge can achieve 82% efficiency at 1MHz, but the two-phase Buck can only achieve 79% efficiency at 500kHz. Therefore, 3% efficiency improvement is achieved with the NFB at double the switching frequency, which is a very significant improvement. Furthermore, at 500kHz and 30A a 5% efficiency improvement is achieved.

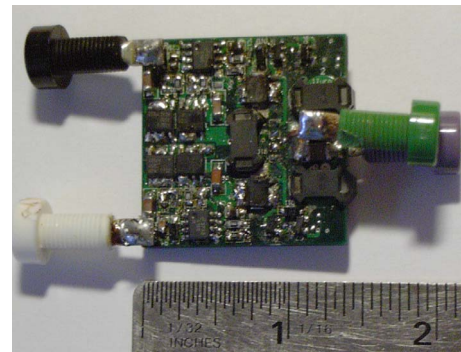


Fig 15 Photo of the prototype; size 1.41"x1.41" (3.6x3.6cm)

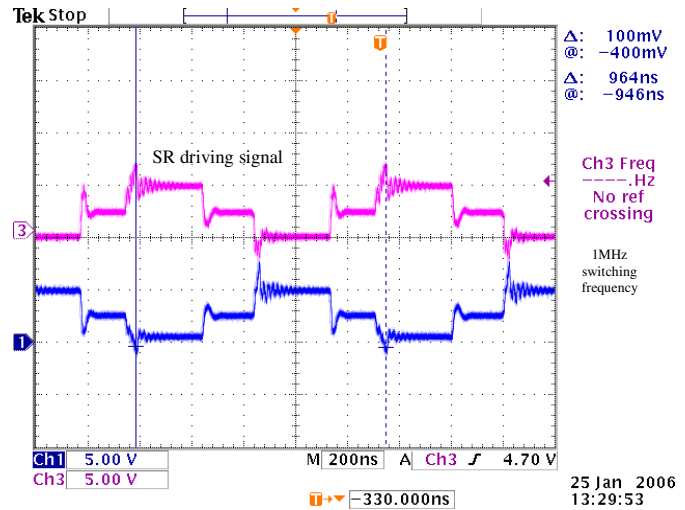


Fig 16 Gate drive signals of the synchronous rectifiers at 1MHz switching frequency

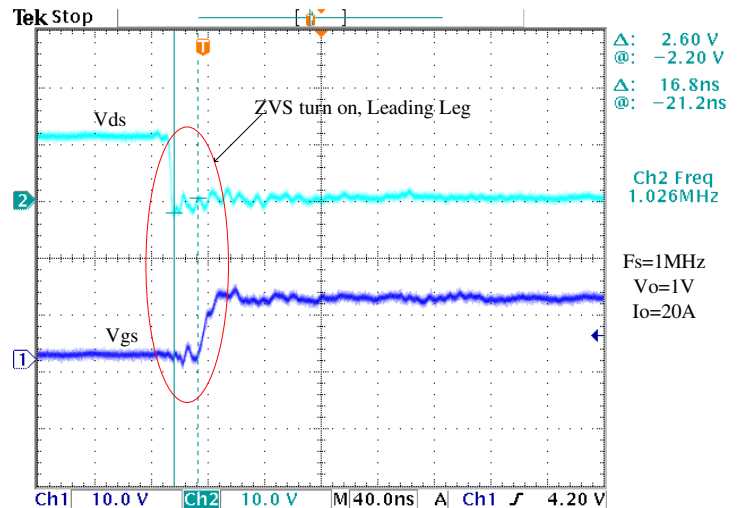


Fig 17 Drain voltage (top) and gate voltage (bottom); ZVS achieved at turn on for the leading leg at 1V/20A load and 1Mhz switching frequency

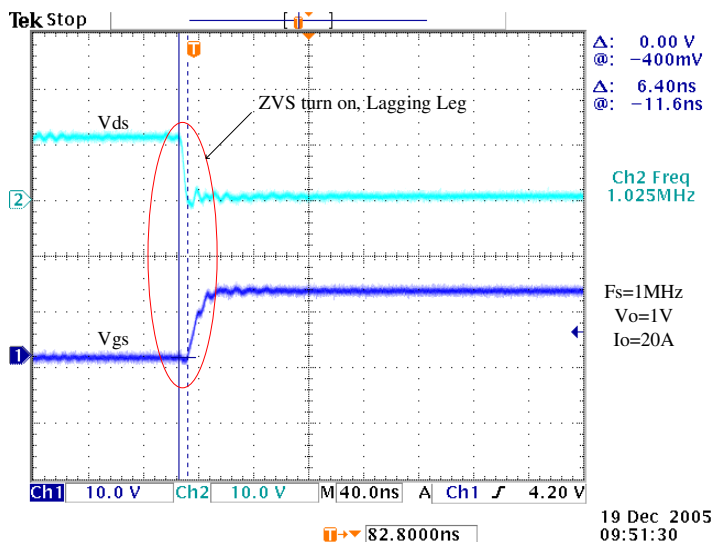


Fig 18 Drain voltage (top) and gate voltage (bottom); ZVS achieved at turn on for the lagging leg at 1V/20A load and 1MHz switching frequency

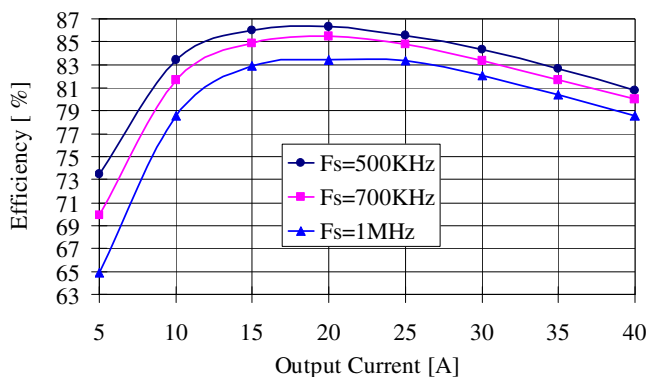


Fig 19 NFB efficiency as a function of load at 1V output

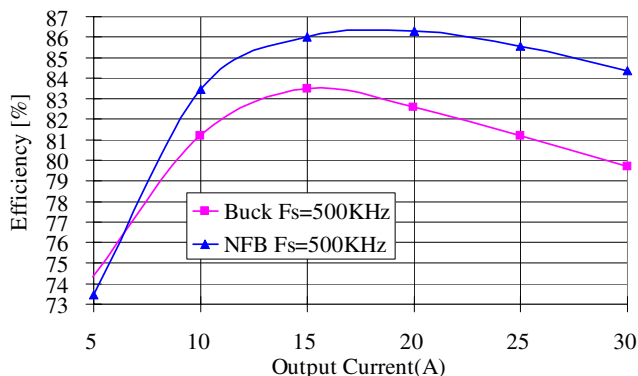


Fig 20 Efficiency comparison as a function of load between the NFB and the two-phase Buck operating at 500kHz and 1V output

## VI. CONCLUSIONS

A new non-isolated full bridge topology was proposed. The

primary side of this topology is derived from the full bridge, however the bottom points of the primary side are connected directly to the positive point of the output. This topology improvement allows the input current to flow directly to the load without going through the transformer, so the current stress of synchronous rectifiers and filter inductors are both reduced.

Compared with the traditional multi-phase buck topology, the switching loss of NFB can be dramatically reduced since it operates with extended duty cycle. Furthermore, zero voltage switching can be achieved when the primary side is operated in phase shift mode. These advantages enable the NFB to achieve higher efficiency than a two-phase synchronous buck. These lower losses can also permit the NFB to operate at much higher switching frequencies than the buck. In addition, smaller output inductors and capacitors can be used to improve the dynamic response and reduce the component cost.

To demonstrate the advantages of this topology, a VRM module has been built and tested at 12V input and 1V output. At 30A load and 500kHz switching frequency, the NFB achieves a 5% efficiency improvement. When the NFB operates at 1MHz, it achieves a 3% efficiency improvement in comparison to the buck operating at 500kHz.

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