A Quick Capacitor Charge Balance Control Method to Achieve Optimal Dynamic Response for Buck Converters

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Abstract – A novel control method is presented in this paper which utilizes the concept of capacitor charge balance to achieve optimal dynamic response for Buck converters undergoing a rapid load change. The proposed charge balance method is implemented with analog components and is cheaper and more effective than its digital counterparts since complex arithmetic and sampling delay is eliminated. The proposed controller will consistently cause the Buck converter to recover from an arbitrary load transient with the smallest possible voltage deviation in the shortest possible settling time. Since the controller is non-linear during transient conditions, it is not limited by bandwidth/switching frequency. Unlike conventional linear controllers, the dynamic response (voltage deviation, settling time) of the proposed controller can be accurately predicted using a set of equations. This greatly simplifies the design process of the output filter. Simulation and experimental results show the functionality of the controller and demonstrate the superior dynamic response over that of a conventional linear controller.

I. INTRODUCTION

Traditionally, linear analog controllers (such as voltage-mode and current-mode schemes) have been utilized to control Buck converters. These controllers offer benefits such as zero steady-state error and predictable switching frequency. However, the dynamic response of linear controllers is limited by their bandwidth. Therefore, numerous non-linear controllers have been proposed to overcome bandwidth limitations. Hysteretic voltage and current mode controllers are presented in [1-4]. While these controller schemes significantly improve the dynamic response of a Buck converter over that of linear controllers, they all suffer from at least one of the following drawbacks: 1) Variable switching frequency, 2) Non-zero steady-state error, 3) Operating frequencies largely dependant on the equivalent series resistance (ESR) of the output capacitor.

It is proposed in [5], that by combining linear and non-linear controller schemes, the dynamic response can be improved while not sacrificing synchronous switching frequency operation or zero steady-state error. This method proves effective, however the controller tends to "over-compensate" for load current variations, causing the output voltage to sometimes over-shoot after it recovers from a voltage drop, thereby resulting in long settling times.

It is presented in [6], that for a Buck converter reacting to a rapid load current variation, an "optimal response" exists that can minimize both the voltage deviation and the settling time of a converter. In [6], a method is presented to design a linear controller that attempts to mimic this optimal response. While this controller can produce a near-optimal response, it is impossible for a linear controller to accurately achieve the desired optimal response since the response is, in fact, non-linear.

In [7], equations to determine the optimal response to a disturbance are presented. The optimal response, to a large range of disturbances, is calculated using MATLAB offline and programmed into a digital controller. The controller successfully achieves a minimal, predictable settling time to an external disturbance. Unfortunately, the controller is only functional in open-loop configuration and the time instant when the disturbance occurs and the magnitude of the load variation must be defined in advance which is an impossible situation for most applications.

In [8], a digital controller is presented which can calculate the optimal response to an arbitrary load variation "on-the-fly". The digital controller significantly improves the dynamic response of a converter undergoing a fast load transition. However, the controller performs multiplication, division and square-root operations resulting in costly implementation. Furthermore, it is determined that the response of [8] could further be improved if the sampling delay were eliminated.

In this paper, a novel analog controller is presented which causes a Buck converter to achieve optimal dynamic response (as claimed in [8]), yet can be implemented using a low-cost analog scheme. Also, since the controller is analog, the sampling delay is removed resulting in faster reaction to a transient event. This paper will describe the controller concept, mathematical analysis and provide simulation and experimental results of the controller's operation.

II. CONTROLLER CONCEPT

The principle of capacitor charge balance has been utilized extensively for the purpose of steady-state modeling and analysis of DC-DC converters. The principle of capacitor charge balance states that, in steady state, the average of the capacitor current over one switching period must be equal to zero. This condition must be satisfied in order for the output

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voltage to be equal at the beginning and the end of a switching cycle. Equation (1) represents the principle of capacitor charge balance for a Buck converter under steady state.

$$v_c(T_s) - v_c(0) = \tfrac{1}{C} \cdot i_{c\,avg} = 0 \rightarrow \frac{1}{T_s} \int_0^{T_s} i_c(t)dt = 0 \qquad (1)$$

By recognizing that the integral period of (1) may be extended over the total transient time of a DC-DC converter, equation (2) is developed.

$$v_c(t_b) - v_c(t_a) = \tfrac{1}{C} \cdot i_{c\,avg} = 0 \rightarrow \frac{1}{t_b - t_a} \int_a^{t_b} i_c(t)dt = 0 \qquad (2)$$

where t_a represents the beginning of the transient period and t_b represents the end of the transient period. Thus, if at t_b the inductor current i_L equals the load current and (2) has been satisfied, the output voltage will have returned to its reference voltage and, therefore, the converter has recovered from the transient event. This concept can be used to minimize the voltage deviation and settling time of a converter undergoing a load current step change.

A. Minimize Voltage Deviation

Referring to Fig. 1, immediately following a positive load current step, the inductor current cannot change instantaneously to supply the load. Therefore, a portion of the load current must be supplied by the output capacitor. This, in turn, causes the output capacitor to lose charge and causes the output voltage to decrease. The output capacitor will finish discharging when the inductor current reaches the new load current (at t_1). In order to minimize the output voltage undershoot, the inductor current must be allowed to vary at its maximum slew rate (d = 100%) for T_0.

Referring to Fig. 2, following a negative load current step, the capacitor must absorb the excess inductor current until it equals the new load current (at t_1). This causes the capacitor to charge and causes the output voltage to increase. In order to minimize the output voltage overshoot, the inductor current must be allowed to vary at its maximum slew rate (d = 0%) for T_0.

B. Minimize Settling Time

Referring to Fig. 1, the output capacitor will start to recharge and the output voltage increase when the inductor current begins to exceed the new load current. In order to minimize the time required to recharge the capacitor, the duty cycle will remain at 100% for T_1. At t_2, the duty cycle will be set to 0% causing the inductor current to decrease at its maximum slew rate. t_2 should be such that at the instant that the inductor current returns to the new load current (at t_3), $A_{discharge}$ equals A_{charge}. At this point, the output voltage and the inductor current are at their steady-state values and the converter will have fully recovered from the positive load step.

Referring to Fig. 2, for a negative load step, the duty cycle will remain at 0% for T_1 in order to minimize the time

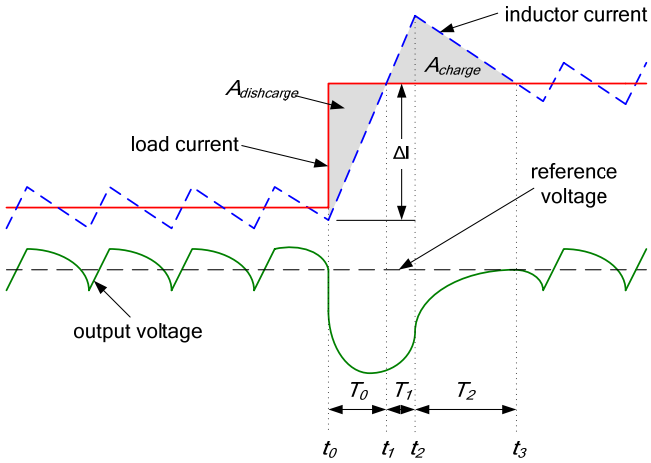

Fig. 1 Proposed controller response to a positive load current step

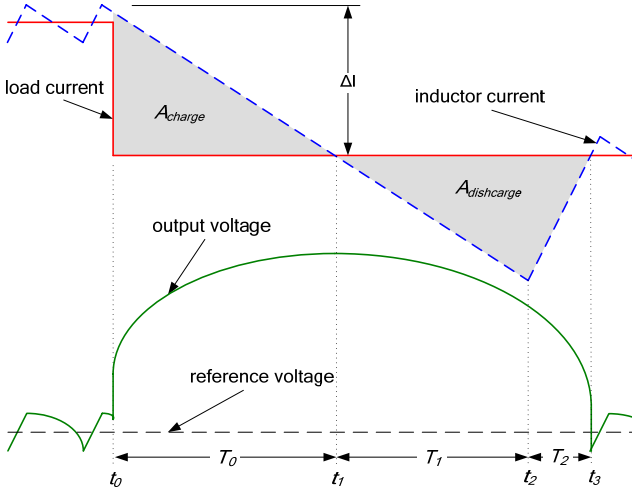

Fig. 2 Proposed controller response to a negative load current step

required to remove the necessary charge from the capacitor. At t_2, the duty cycle will be set to 100% causing the inductor current to increase at its maximum slew rate. As above, t_2 should be such that at the instant that the inductor current returns to the new load current (at t_3), $A_{discharge}$ equals A_{charge}.

In summary, the two key points of the proposed control method are:

1. Immediately detect the load current step change and react by setting the duty cycle to its maximum value (for a positive step change) or to its minimum value (for a negative step change).
2. Set the duty cycle to its minimum value (for a positive load step) or its maximum value (for a negative load step) at t_2. t_2 should be such that A_{charge} will equal $A_{discharge}$ at time t_3. This will cause the output voltage to equal the reference voltage at the exact moment that the inductor current equals the load current.

III. Mathematical Analysis of the Proposed Controller Response

Fig. 3 illustrates the charge and discharge areas for a positive load current step change.

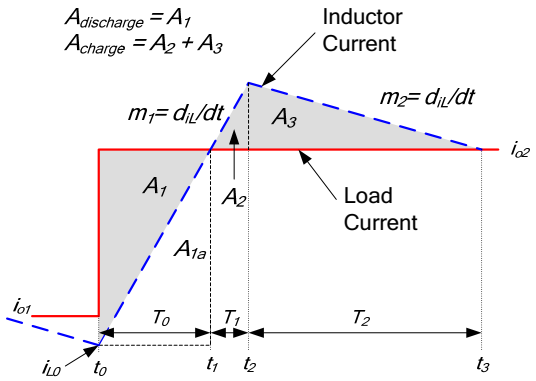

Fig. 3 Proposed inductor current response to a positive load step

Time period T_0:

It is apparent in Fig. 3, that the total discharge area A_1 is equal to A_{1a}, thus (3) is true.

$$A_1 = \int_{t0}^{t1}[i_{o2} - i_L(t)]dt = A_{1a} = \int_{t0}^{t1}[i_L(t) - i_{L0}]dt \tag{3}$$

m_1 represents the rate at which $i_L(t) - i_{L0}$ is increasing, such that (4) and (5) are true.

$$m_1 = \frac{d[i_L(t) - i_{L0}]}{dt} \tag{4}$$

$$i_L(t) - i_{L0} = \int_{t0}^{t} m_1 dt \tag{5}$$

Therefore, by combining (3) and (5), the total discharge area $A_{discharge}$ can be expressed in (6).

$$A_{discharge} = A_1 = A_{1a} = \iint_{T0} m_1 (dt)^2 \tag{6}$$

Time period T_1:

The charge area A_2 is expressed in (7).

$$A_2 = \int_{t1}^{t2}[i_L(t) - i_{o2}]dt \tag{7}$$

By inspection, it is obvious that m_1 also represents the rate that $i_L(t)$-i_{o2} is increasing, as expressed in (8) and (9).

$$m_1 = \frac{d[i_L(t) - i_{o2}]}{dt} \tag{8}$$

$$i_L(t) - i_{o2} = \int_{t1}^{t} m_1 dt \tag{9}$$

Therefore, by combining (7) and (9), the charge area A_2 can be expressed as (10).

$$A_2 = \iint_{T1} m_1 (dt)^2 \tag{10}$$

Using basic geometry, a relationship for A_2 and A_3 is found in (11), in terms of the rising and falling slew rates of the inductor current.

$$\frac{A_3}{A_2} = \frac{m_1}{-m_2} \tag{11}$$

Thus, by combining (10) and (11), an expression for the total charge area A_{charge} is presented in (12).

$$\begin{aligned} A_{charge} = A_2 + A_3 &= \iint_{T1} m_1 (dt)^2 + \iint_{T1} \frac{m_1^2}{-m_2}(dt)^2 \\ &= \iint_{T1} \frac{m_1 m_2 - m_1^2}{m_2}(dt)^2 \end{aligned} \tag{12}$$

By using (12), it is possible to predict the total charge area at time t_2. In order to satisfy the principle of capacitor charge balance at t_3, (13) must be true.

$$\begin{aligned} A_{discharge} - A_{charge} &= 0 \\ \iint_{T0} m_1 (dt)^2 - \iint_{T1} \frac{m_1 m_2 - m_1^2}{m_2}(dt)^2 &= 0 \\ \iint_{T0} (dt)^2 - \frac{m_2 - m_1}{m_2} \iint_{T1} (dt)^2 &= 0 \end{aligned} \tag{13}$$

The inductor current slew rates of a Buck converter are known ($m_1 = (V_{in}-V_o)/L$; $m_2 = -V_o/L$) and are substituted into (13) to yield (14).

$$\begin{aligned} A_{discharge} - A_{charge} &= 0 \\ \iint_{T0} (dt)^2 - \frac{\frac{-V_o}{L} - \frac{(V_{in} - V_o)}{L}}{\frac{-V_o}{L}} \iint_{T1} (dt)^2 &= 0 \\ \iint_{T0} (dt)^2 - \frac{V_{in}}{V_o} \iint_{T1} (dt)^2 &= 0 \end{aligned} \tag{14}$$

Since analog division is costly, the equation is simplified by multiplying V_o to both sides, as expressed in (15).

$$\begin{aligned} A_{discharge} - A_{charge} &= 0 \\ V_o \iint_{T0} (dt)^2 - V_{in} \iint_{T1} (dt)^2 &= 0 \end{aligned} \tag{15}$$

Using equation (15), it is possible to use an analog double integrator, to calculate the time t_2 that will allow $A_{charge} - A_{discharge}$ to equal zero when the inductor current reaches the new load current (at t_3). The aforementioned concept is illustrated in Fig. 4.

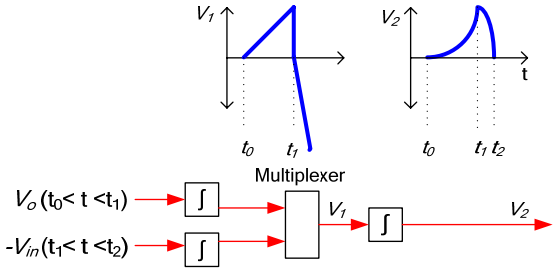

Fig. 4 Proposed double integrator to predict t_2

In the case of a positive load current step, the duty cycle would be set to 0% when V_2 equals zero (at time t_2). This will allow the inductor current to fall and reach the output current at the exact moment that the charge previously removed from the capacitor equals the charge delivered to the capacitor.

A similar analysis is performed for a negative current step change. The result of the analysis is expressed in (16).

$$\begin{aligned} A_{charge} - A_{discharge} &= 0 \\ (V_{in} - V_o) \iint_{T0} (dt)^2 - V_{in} \iint_{T1} (dt)^2 &= 0 \end{aligned} \tag{16}$$

IV. Operation of Proposed Control Method

Fig. 6 illustrates the block diagram of the proposed control method. The operation of the controller and its logic is described below.

The converter switches from its conventional controller to the proposed controller immediately following a load step change. The controller operation can be described in 4 steps.

Step 1: Detect Load Current Step Change (t_0)

The controller indirectly senses the capacitor current using a non-invasive trans-impedance amplifier, connected to the output voltage (as shown in Fig. 6).

When the capacitor current exceeds a predetermined threshold, the controller will immediately change the duty cycle to 100% (for a positive load step), or 0% (for a negative load step).

The controller logic will release the "reset" switch of integrator 1a and integrator 2. The output of integrator 1a will begin to increase linearly with a slope of V_o (for a positive step change), or Vin-Vo, (for a negative step change). The output of integrator 2 will begin to increase exponentially. (See Fig. 5.)

Step 2: Detect Capacitor Current Cross-over (t_1)

A comparator, fed by the capacitor current sensor, is used to determine the point at which the capacitor current changes direction. This point indicates that the inductor current has reached the new load current as illustrated in Fig. 5 at point t_1. At this point, integrator 1a will be "reset" and integrator 1b will be activated. The output of integrator 1b will begin to decrease linearly with a slope of $-V_{in}$. The output of integrator 2 will begin to decrease exponentially, as shown in Fig. 5.

Step 3: Alter Duty Cycle (t_2)

At the moment that the output of integrator 2 returns to zero (at t_2), the duty cycle will be set to 0% (for a positive load step change) or 100% (for a negative load step change). At this point, the inductor current will be at its maximum (in the case of a positive load step change) or its minimum (in the case of a negative load step change). The inductor current will begin to decrease toward the new load current in the case of a positive load step change. In the case of a negative load step change, the inductor current will begin to increase toward the new load current.

Step 4: De-activate Controller (t_3)

At t_3, the inductor current reaches the new load current (determined by a second capacitor current switchover) and the output voltage returns to its reference value. At this point, the controller deactivates and the conventional controller resumes control of the converter.

The controller operation for a positive load current step change is illustrated in Fig. 5.

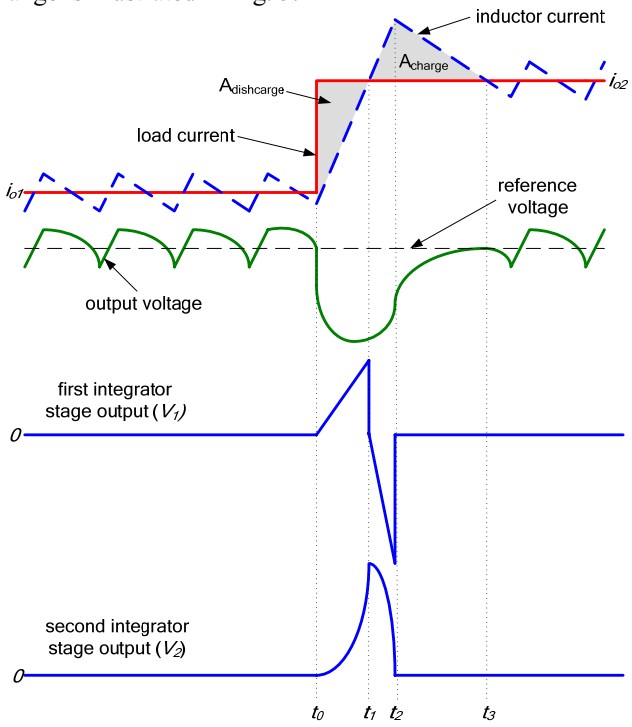

Fig. 5 Response to a positive load current step change

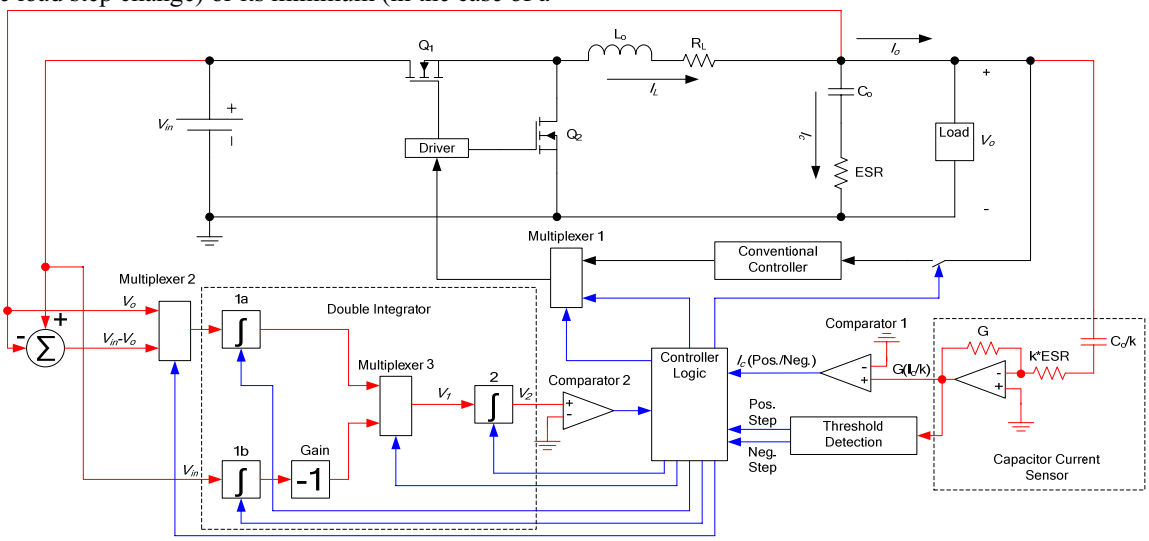

Fig. 6 Block diagram of proposed controller

V. Theoretical Voltage Deviation and Settling Time

In addition to improving the dynamic performance of a Buck converter, the proposed controller also simplifies the design of the output filter since its response to a large-signal load transient is predictable. It is possible to calculate the dynamic response (settling time, voltage deviation) to a converter experiencing an arbitrary load variation.

Referring to Fig. 1, T_0 and $A_{discharge}$ (for a positive load step) are calculated using (17) and (18) respectively.

$$T_0 = \Delta I \frac{L}{V_{in} - V_o} \tag{17}$$

$$A_{discharge} = \frac{1}{2} T_0 \Delta I = \Delta I^2 \frac{L}{2(V_{in} - V)_o} \tag{18}$$

For a positive load step, A_{charge} is calculated using (19).

$$A_{charge} = T_1^2 \frac{V_{in}(V_{in} - V_o)}{2 V_o L} \tag{19}$$

In order for (2) to be satisfied, $A_{discharge}$ must equal A_{charge}. Therefore, (18) can be substituted into (19) and T_1 can be isolated as shown in (20).

$$T_1 = \sqrt{\frac{V_o L^2 \Delta I^2}{V_{in}(V_{in} - V_o)^2}} = \frac{L \Delta I}{V_{in} - V_o} \sqrt{\frac{V_o}{V_{in}}} \tag{20}$$

A relationship between T_1 and T_2 is defined in (21).

$$T_2 = \frac{V_{in} - V_o}{V_o} T_1 \tag{21}$$

Therefore, the total settling time for a positive load step is calculated in (22).

$$T_{set\_pos} = T_0 + T_1 + T_2 = \frac{L \Delta I}{(V_{in} - V_o)} \left(1 + \frac{V_{in}}{V_o} \sqrt{\frac{V_o}{V_{in}}} \right) \tag{22}$$

Similarly, the settling time for a negative load step is calculated in (23).

$$T_{set\_neg} = T_0 + T_1 + T_2 = \frac{L \Delta I}{V_o} \left[1 + \left(\frac{V_{in}}{V_{in} - V_o} \right) \sqrt{\frac{(V_{in} - V_o)}{V_{in}}} \right] \tag{23}$$

Fig. 7 illustrates the theoretical settling times for a Buck converter controlled by the quick capacitor charge balance method.

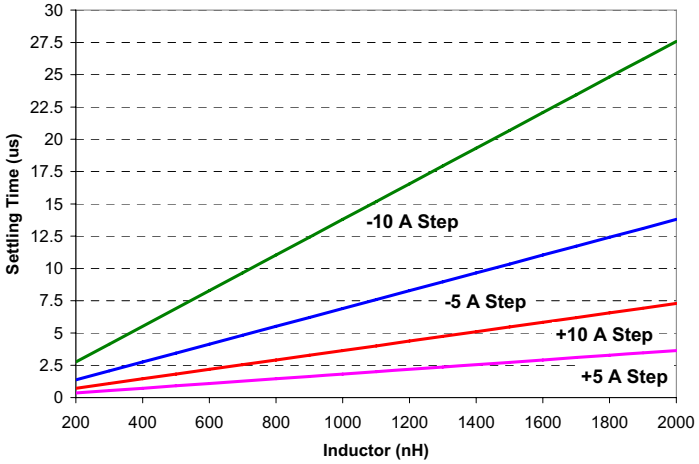

Fig. 7 Theoretical settling time for converter under proposed control method (V_{in} = 12V, V_o = 1.5V)

Under the proposed controller, it is also possible to precisely calculate the voltage deviation due to an arbitrary load current step change.

For a positive step change, it is evident in Fig. 1 that the capacitor is discharging during time period T_0. The output voltage over the time period T_0 (letting $t_0 = t = 0$) is derived in (24).

$$v_o(t) = V_{ref} - ESR\left(\Delta I - \frac{(V_{in} - V_o)t}{L} \right) - \frac{\frac{1}{2}\left(\frac{\Delta I^2 L}{V_{in} - V_o} - \left(\frac{\Delta I \cdot L}{V_{in} - V_o} - t \right) \left(\Delta I - \frac{(V_{in} - V_o)t}{L} \right) \right)}{C} \tag{24}$$

$$v_o(t) = V_{ref} - \frac{2ESR \cdot C(V_o t + \Delta I \cdot L - V_{in} t) - t^2 (V_{in} - V_o) + 2L \cdot \Delta I \cdot t}{2L \cdot C}$$

In order to determine the time at which the voltage is at its minimum (t_{min}), it is necessary to calculate the derivative of the output voltage with respect to time, as derived in (25).

$$\frac{dv_o}{dt} = \frac{ESR \cdot C(V_{in} - V_o) + t(V_{in} - V_o) - \Delta I \cdot L}{L \cdot C} \tag{25}$$

By setting (25) equal to zero and solving for t, t_{min} is calculated in (26).

$$t_{\min} = \frac{ESR \cdot C(V_o - V_{in}) + \Delta I \cdot L}{V_{in} - V_o} \tag{26}$$

By substituting (26) into (24), Δv_o_pos is solved in (27).

$$\Delta v_{o\_pos} = -\frac{ESR^2 \cdot C^2 (V_{in}^2 - 2V_{in}V_o + V_o^2) + \Delta I^2 L^2}{2(V_{in} - V_o)L \cdot C} \tag{27}$$

Similarly, the overshoot for a negative current step is calculated in (28).

$$\Delta v_{o\_neg} = \frac{ESR^2 \cdot C^2 \cdot V_o^2 + \Delta I^2 L^2}{2V_o \cdot L \cdot C} \tag{28}$$

Fig. 8 and Fig. 9 illustrate the theoretical voltage deviation for a Buck converter controlled by the quick capacitor charge balance method.

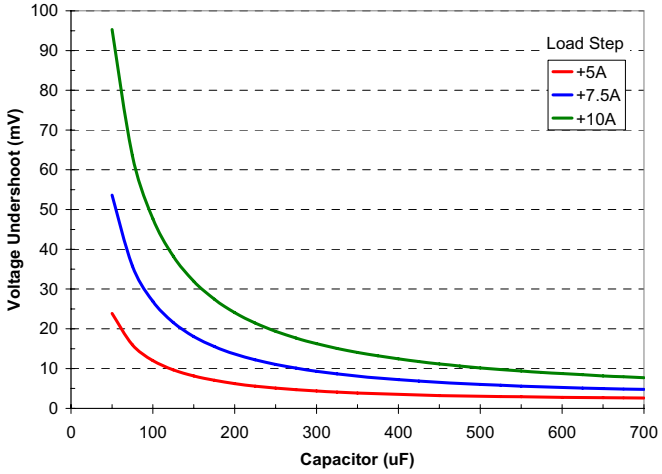

Fig. 8 Theoretical undershoot for a Buck converter under the proposed control method (V_{in} = 12V, V_o = 1.5V, L = 1uH, ESR = 0.5mΩ)

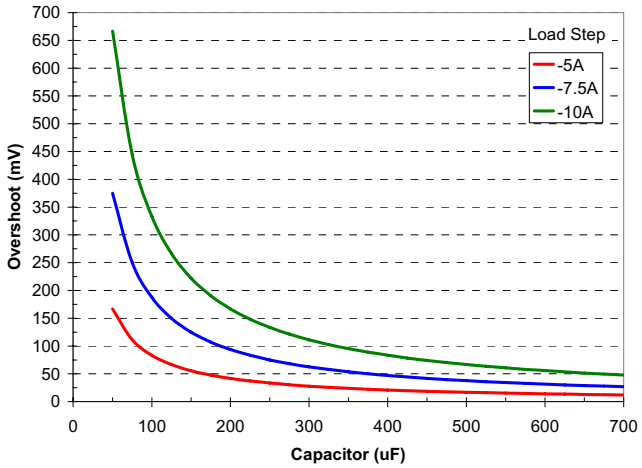

Fig. 9 Theoretical overshoot for a Buck converter under the proposed control method (V_{in} = 12V, V_o = 1.5V, L = 1uH, ESR = 0.5mΩ)

VI. Simulation Results

In order to verify the functionality of the quick capacitor charge balance method, a Buck converter, undergoing a load current step, was simulated. The parameters of the simulated Buck converter were as follows: V_{in}=12V, V_{out}=1.5V, f_s=400kHz, L=1uH, C=181uF, ESR=0.5mΩ, ESL = 50pH.

Fig. 10 shows a voltage-mode controlled Buck converter undergoing a 0A→10A load step change. The bandwidth of the controller was designed to be 71kHz and the phase margin was 42º. Fig. 11 shows the quick capacitor charge balance control method response to a 0→10A load step change.

Fig. 12 shows the voltage-mode controlled converter undergoing a 10A→0A load step change. Fig. 13 shows the quick capacitor charge balance control method response to a 10A→0A load step change.

It is demonstrated through simulation that (for a positive load step) the settling time of the converter with proposed controller is improved by 90% compared to that of the voltage-mode controlled converter.

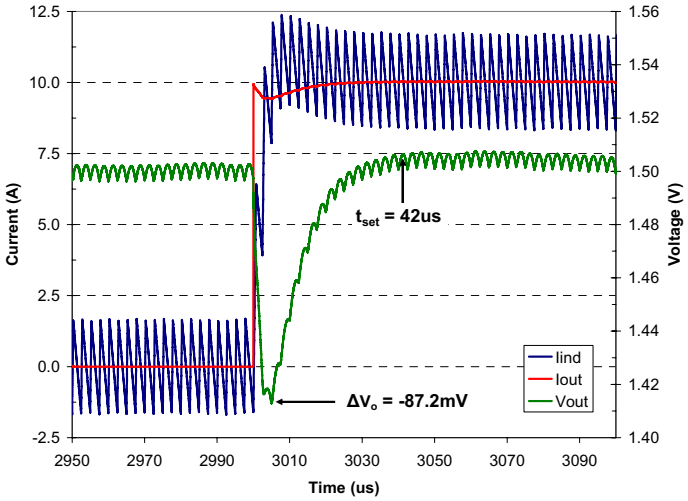

Fig. 10 Simulated voltage-mode controller response to a 0A→ 10A load current step change

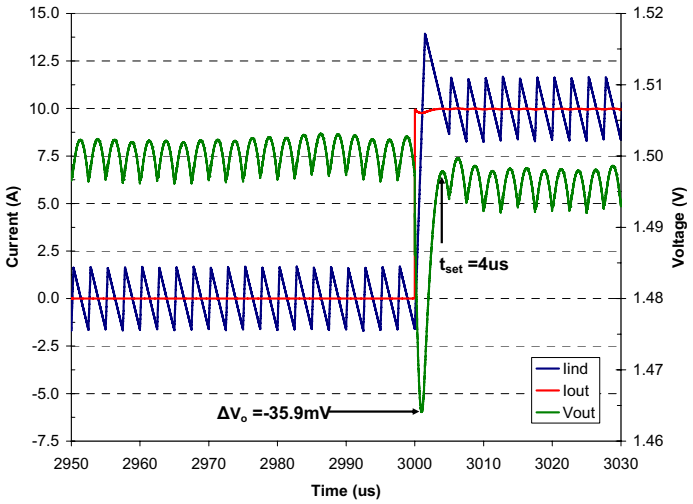

Fig. 11 Simulated proposed controller response to a 0A→ 10A load current step change

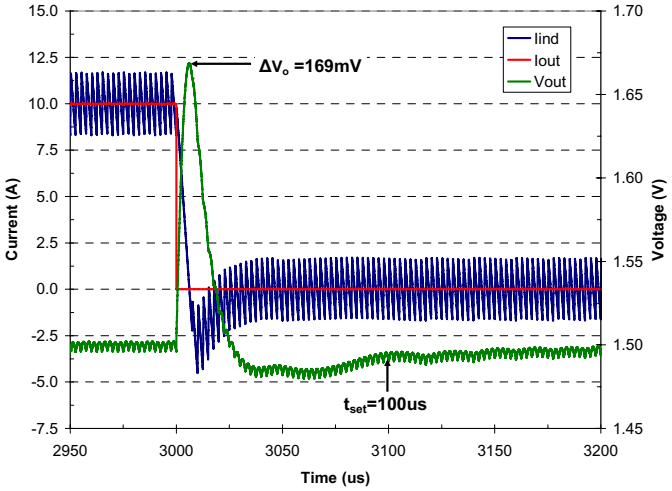

Fig. 12 Simulated voltage-mode controller response to a 10A→ 0A load current step change

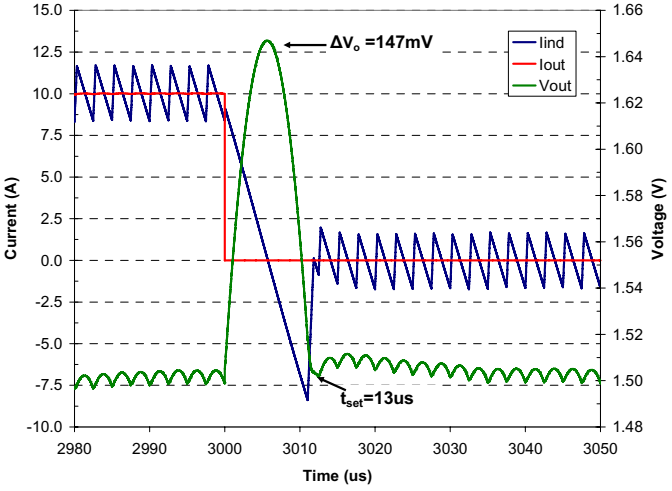

Fig. 13 Simulated proposed controller response to a 10A→ 0A load current step change

It is also shown that the voltage undershoot of the converter with the proposed controller is improved by 59% compared to that of the voltage-mode controlled converter. The simulation results of the proposed controller are in correspondence with the theoretical results calculated in (22) and (27).

For a negative load step, the settling time of the converter with the proposed controller is improved by 87% compared to that of the voltage-mode controlled converter. It is also shown that the voltage overshoot of the converter with the proposed controller is improved by 13% compared to that of the voltage-mode controlled converter. The simulation results of the proposed controller are also in correspondence with the theoretical results calculated in (23) and (28).

VII. Experimental Results

A prototype of the quick capacitor charge balance control method was designed and implemented with the aforementioned converter. Fig. 14 and Fig. 15 show a voltage-mode controlled Buck converter (with a bandwidth of approximately 50kHz) and the proposed controller undergoing a 10A→0A load step change respectively.

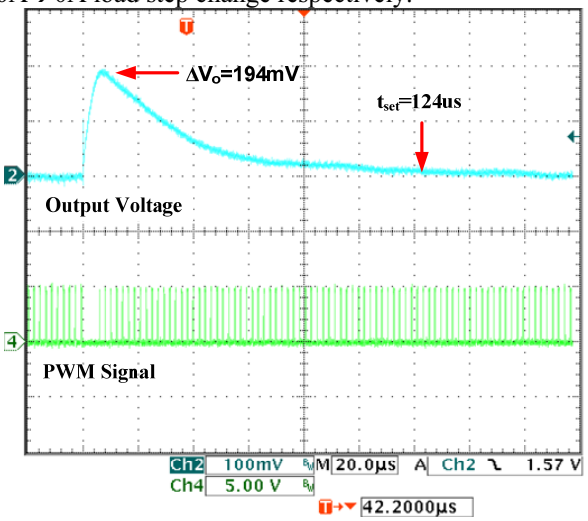

Fig. 14 Voltage-mode controller response to a 10A→ 0A load current step change

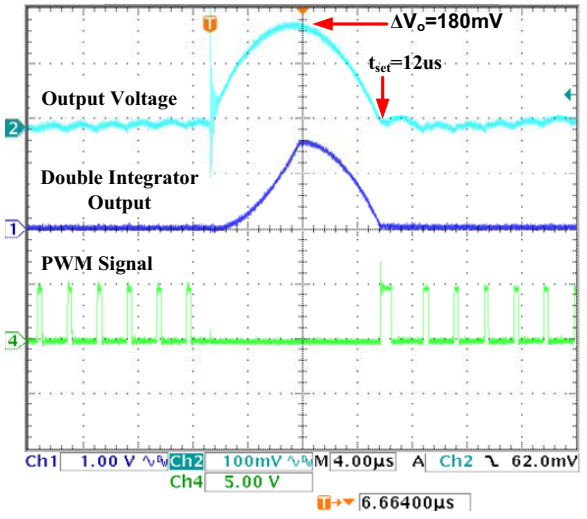

Fig. 15 Proposed controller response to a 10A→ 0A load current step change

It is demonstrated through experimentation that the settling time of the converter with the proposed controller is improved by 90% compared to that of the voltage-mode controlled converter. It is also shown that overshoot of the converter with the proposed controller is improved by 7% compared to that of the voltage-mode controlled converter.

VIII. Conclusions

A novel quick capacitor charge balance control method has been presented that significantly improves the dynamic response of a Buck converter. The combined linear/non-linear nature of the controller allows the controller to operate immediately (without bandwidth limitations) while not sacrificing zero steady-state error and/or stability.

The controller is far superior to conventional linear methods and simpler and more cost-effective than digitally-implemented charge balance methods.

It has been shown that the voltage deviation and settling time can be accurately calculated when using the proposed method, greatly simplifying the design of the converter.

For a positive load current step, simulation results demonstrate a 59% improvement of undershoot and a 90% improvement of settling time compared to that of a voltage-mode controller.

For a negative load current step, simulation and experimental results demonstrate more than a 7% improvement of overshoot and more than a 87% improvement of settling time compared to that of a voltage-mode controller.

The proposed controller will allow for a significant output capacitor reduction for a Buck converter (for fixed regulation requirements), thereby greatly reducing the cost of the Buck.

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