A High Efficiency Synchronous Buck VRM with Current Source Gate Driver

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Abstract – In this paper, a new current source gate drive circuit is proposed for high efficiency synchronous buck VRMs. The proposed circuit achieves quick turn-on and turn-off transition times to reduce switching loss and conduction loss in power MOSFETS. The driver circuit consists of two sets of four control switches and two very small inductors (typically 50nH-300nH each at 1MHz). It drives both the control MOSFET and synchronous MOSFET in synchronous buck VRMs. An analysis, design procedure, optimization procedure and experimental results are presented for the proposed circuit. Experimental results demonstrate an efficiency of 86.6% at 15A load and 81.9% at 30A load for 12V input and 1.3V output at 1MHz.

I. INTRODUCTION

The multi-phase synchronous buck converter is used nearly exclusively as the voltage regulator module (VRM) to power microprocessors due to its simplicity and low component count. In order to reduce the size of the VRM passive components and to improve the dynamic response, the switching frequency has increased beyond 500kHz and is approaching the MHz range. However, as the switching frequency increases, the switching loss in the control MOSFET and gate loss in the control and synchronous MOSFETs increase. These two frequency dependent loss components can significantly degrade converter efficiency when switching at and beyond 1MHz. In existing multi-phase buck VRMs, a conventional complementary pair driver is used almost exclusively.

A conventional gate drive circuit is illustrated in Fig. 1. With these drivers, all of the power MOSFET gate energy is dissipated. However, the problems of the conventional gate driver extend beyond the gate drive circuit loss. Since these drivers operate with RC type charging and discharging, switching speed is limited. The MOSFET gate current is limited to a value significantly less than the peak driver current during the turn-on and turn-off times which occur during the plateau and threshold regions of the MOSFET gate-to-source voltage. Furthermore, the rise and fall times are both inversely proportional to the gate current, so the switching losses can be reduced by increasing gate current. However, in conventional gate drivers, this is generally not possible since the peak current is already limited by the current handling capability of the driver switches. This problem is even more severe when MOSFET source inductance is considered. During turn-on, or turn-off, the gate current spike through the source inductance induces a voltage reducing the gate-to-source voltage which further increases the switching loss.

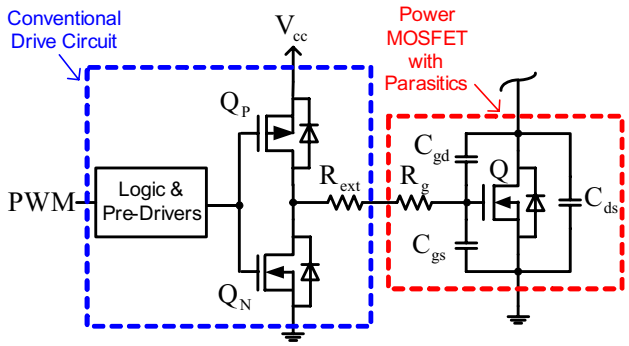

Fig. 1 Conventional gate drive circuit with power MOSFET and its associated parasitics

In order to recover a portion of the gate energy otherwise lost in conventional drivers, several papers have been published proposing resonant gate drive techniques. Of the methods previously proposed, none of them exploit switching loss savings and all of them suffer from at least one of six driver specific problems:

1) Only low side, ground referenced drive [1]-[5],[7]-[9].
2) High circulating current in the driver control switches during the power MOSFET on and off states resulting in excessive conduction loss [1],[10].
3) Peak driver current dependent on duty cycle, or switching frequency resulting in switching times and gate loss that varies with the operating point [1],[10].
4) Large inductance [1],[10], bulky transformer, or coupled inductance [2]-[6].
5) Slow turn-on and/or turn-off transition times, which increases both conduction and switching losses in the power MOSFET due to charging the power MOSFET gate beginning at zero current [2]-[8].
6) The inability to actively clamp the power MOSFET gate to the line during the on time and/or to ground during the off time, which can lead to undesired false triggering of the power MOSFET gate, i.e. lack of Cdv/dt immunity [2]-[6],[8].

To solve the problems inherent to conventional drivers and the six problems above for resonant drivers, and most importantly, to reduce switching loss, in the following section, a new current source gate drive circuit is proposed for the synchronous buck converter. The proposed driver features very small inductors (typically 50-300nH at 1MHz compared to 2.2μH in [10]) and a peak current (and therefore, switching time) that is independent of duty cycle. It is shown that the driver can improve the efficiency of a synchronous buck VRM by reducing high side MOSFET switching loss and synchronous rectifier gate loss.

II. Proposed Synchronous Buck Current source Gate Drive Circuit and Operation

A. Proposed Circuit

The proposed synchronous buck current source gate drive circuit is illustrated in Fig. 2 and its associated waveforms are given in Fig. 3. The circuit consists of the synchronous buck and two current source drivers. Each driver has two very small inductors that carry a discontinuous current which minimizes conduction loss and allows the driver to work effectively over a wide duty cycle range. The driver for the control MOSFET Q1 contains a bootstrap diode D_b and capacitor C_b. The operation of the driver is essentially the same for Q1 and Q2 since each driver operates with control signals derived from the independent inputs, PWM1 and PWM2.

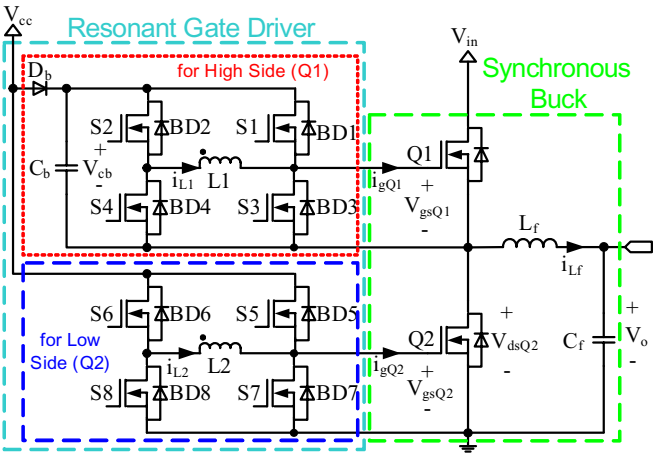

Fig. 2 Proposed synchronous buck current source gate drive circuit

The key idea of the driver operation is the control of the driver switches and body diodes to generate the discontinuous inductor current waveforms. A portion of the inductor current waveform at its peak is then used to charge the power MOSFET gate as a nearly constant current source. This concept is illustrated in Fig. 4, for the high side driver (Q1) from Fig. 2.

A comparison of gate current waveform for the proposed current source driver and a conventional driver is given in Fig. 5. The key advantage of the current source driver is that it maintains a high and nearly constant current during the plateau of the switching transitions. This is noted as i_{g_on} and i_{g_off} for the current source driver in the figure. On the other hand, for the conventional gate driver, the gate current has decayed significantly to i_{pl_on} and i_{pl_off} from its peak values. A second advantage is that the gate current of the current source driver has a very small $\Delta i/\Delta t$ ($=\Delta i_{L1}/t_{on}$) during the complete switching transition. In contrast, the conventional gate driver has a $\Delta i/\Delta t$ equal to the peak gate current over t_{on}. This $\Delta i/\Delta t$ induces a voltage in the MOSFET/driver common source inductance that tends to work against the driver. Fortunately, since the current source driver operates as a current source and not a voltage source, this problem is negated.

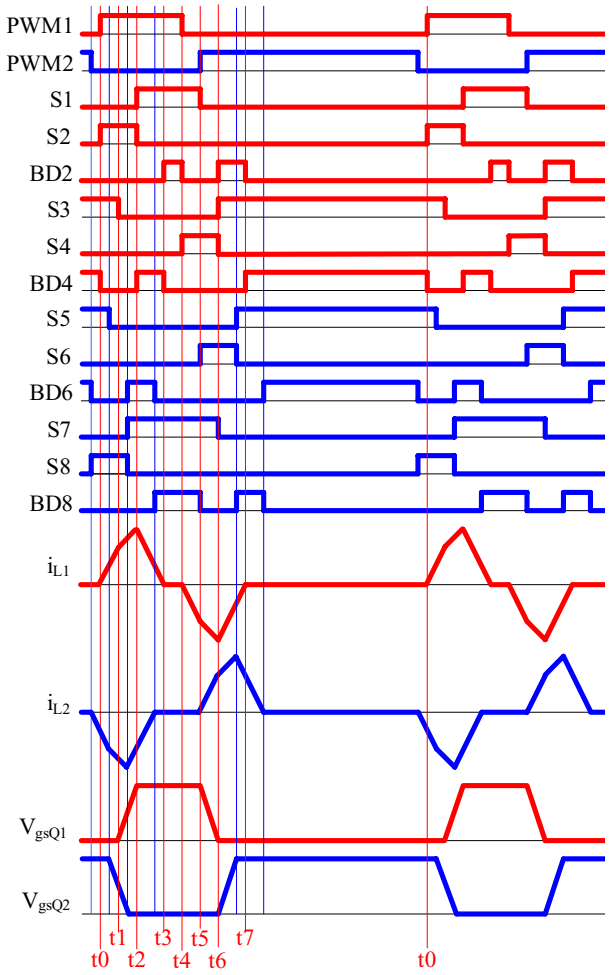

Fig. 3 Proposed driver waveforms

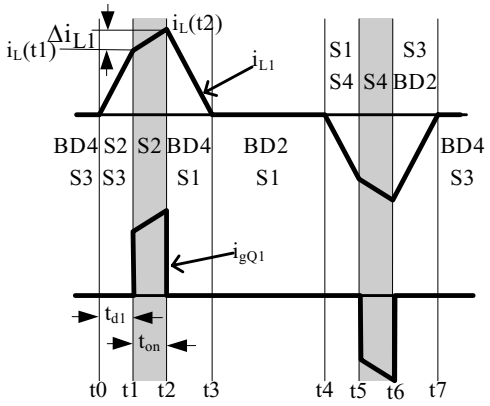

Fig. 4 Current source driver inductor (top) and gate (bottom) current waveforms for the high side MOSFET (Q1)

B. Detailed Operation

The operation of the circuit is explained for the control MOSFET, Q1 as follows. Initially it is assumed that the power MOSFET is in the off state before time t0. For the control switches, the high regions indicate the on-state, so initially only switches S3 and S4 are on and the gate-to-source of Q1 is clamped to zero volts.

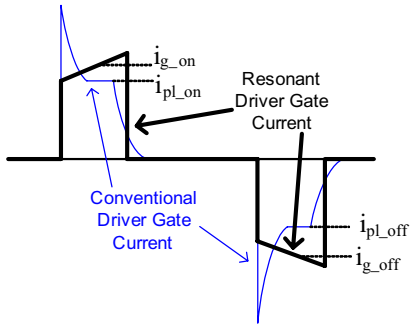

Fig. 5 Comparison of gate current waveforms for the proposed current source driver (bold) and conventional gate driver

t0-t1: At t0, BD4 turns off with ZCS and S2 turns on (with ZCS) allowing the inductor current to ramp up. The current path during this interval is S2-L1-S3 as shown in Fig. 6. Since S3 is in the on state, the gate-to-source of Q1 is clamped low. The interval ends at t1.

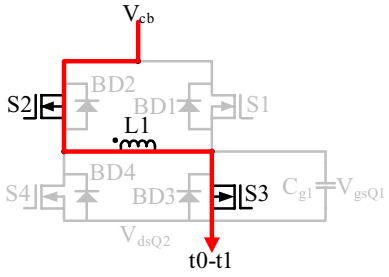

Fig. 6 High side driver operation during t0-t1

t1-t2: At t1, S3 turns off, allowing the inductor current to begin to charge the gate of Q1. The inductor current continues to ramp up, but at a reduced slope as the voltage across the gate capacitance increases. The current path during this interval is S2-L1-C_{g1} as shown in Fig. 7, where C_{g1} represents the equivalent gate capacitance of Q1. This interval ends at t2, when V_{gsQ1} reaches V_{cb} (assuming C_b maintains a constant voltage of V_{cb}).

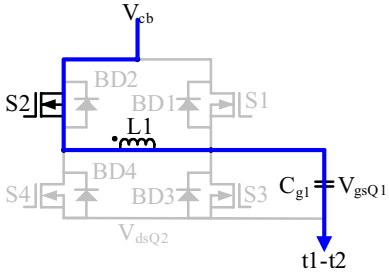

Fig. 7 High side driver operation during t1-t2

t2-t3: At t2, S2 turns off and S1 turns on with ZVS and BD4 turns on, allowing the inductor current to conduct into the dot through the path BD4-L1-S1 as shown in Fig. 8. Most importantly, during this interval when the stored energy in the inductor is returned to the line. During this interval, the inductor voltage has become reverse biased, so the inductor current quickly ramps down towards zero. During this interval, the gate-to-source voltage of Q1 remains clamped to V_{cb}. The interval ends when the inductor current reaches zero at t3.

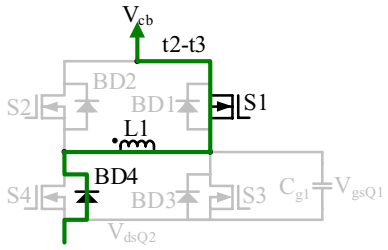

Fig. 8 High side driver operation during t2-t3

t3-t4: At t3, BD4 turns off (with ZCS) and BD2 turns on, which allows any residual inductor current to freewheel through S1-L1-BD2 as shown in Fig. 9. During this interval, the gate-to-source voltage of Q1 remains clamped to V_{cb}. The interval ends at t4 when the pre-charging interval for the turn off cycle begins as dictated by the PWM signal.

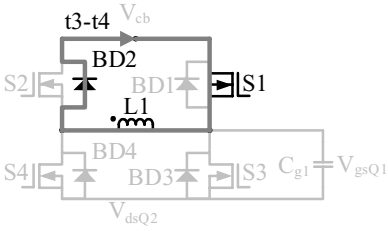

Fig. 9 High side driver operation during t3-t4

t4-t5: At t4, the turn off pre-charging interval begins. BD2 turns off (with ZCS) and S4 turns on (with ZCS). Since S1 was previously on, the inductor current begins to ramp negative out of the dot through the path S1-L1-S4 as shown in Fig. 10. During this interval, the gate-to-source voltage of Q1 remains clamped to V_{cb}. The interval ends at t5.

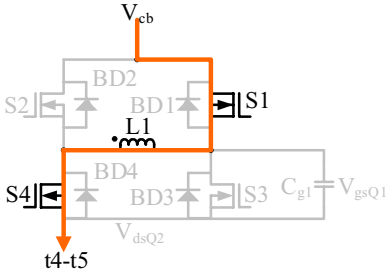

Fig. 10 High side driver operation during t4-t5

t5-t6: At t5, S1 turns off, allowing the inductor current to begin to discharge the power MOSFET gate. The inductor current continues to ramp negative at a reduced slope as the voltage across the gate capacitance decreases. The current path during this interval is C_{g1}-L1-S4 as shown in Fig. 11. The interval ends at t6, when V_{gsQ1} reaches zero.

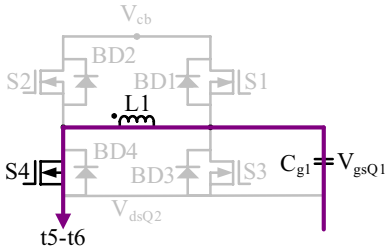

Fig. 11 High side driver operation during t5-t6

t6-t7: At t6, S4 turns off and BD2 turns on and S3 turns on

(with ZVS) allowing the inductor current to conduct out of the dot through the path S3-L1-BD2 as shown in Fig. 12. Most importantly, during this interval when the gate discharging energy is returned to the line. Also, during this interval, the inductor voltage has become reverse biased, so the inductor current quickly ramps down positive towards zero. During this interval, the gate-to-source voltage of Q1 remains clamped to its source voltage. The interval ends when the inductor current reaches zero at t7.

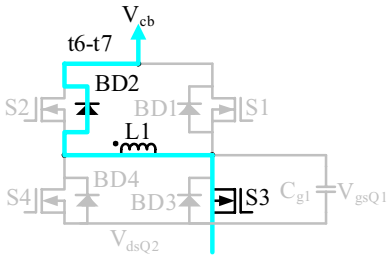

Fig. 12 High side driver operation during t6-t7

t7-t0: At t7, BD2 turns off (with ZCS) and BD4 turns on, which allows any residual inductor current to freewheel through BD4-L1-S3 as shown in Fig. 13. During this interval, the gate voltage of Q1 remains clamped low. The interval ends at t0 when the pre-charging interval for the turn on cycle begins and the entire process repeats.

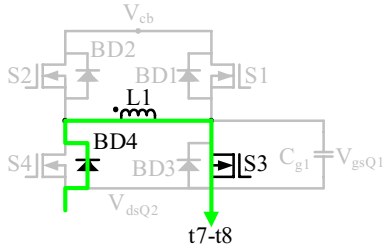

Fig. 13 High side driver operation during t7-t8

The operation of the low side driver for Q2 is the same as for Q1, given an input signal PWM2 for S5-S8.

III. Driver Design Procedure

The power MOSFET turn-on transition time, t_{on}, (from 0V to V_{cb}) is not calculated, but must be chosen by the designer for the given application. For the designer, there is a tradeoff between speed, which translates into switching loss savings, and gate energy recovery. Smaller values of t_{on} reduce switching loss, but require greater peak current in the driver and therefore suffer from greater conduction loss in the driver. Typically, t_{on} should be less than 10% of the switching period. After selecting t_{on}, the turn on inductor pre-charge time, t_{d1} should be selected. This is illustrated in Fig. 4 from t0-t1, of the inductor current waveform during the turn on interval. Typically, t_{d1} should be less than t_{on}. Larger values of t_{d1} yield a larger required inductance and add more delay in the control loop. On the other hand, if t_{d1} is too small, the gate energy recovery is limited, or the pre-charge current level is small. A typical starting value of t_{d1} is half of t_{on}.

In order to calculate the required resonant inductance, (1)-(3), must be used. Equation (1) is derived assuming that there is no resistive loss in the drive circuit during t_{d1}.

$$L_1 = \frac{V_{cb} t_{d1}}{i_{L1}(t_1)} \tag{1}$$

Equation (2) is derived using an approximation. The equivalent resonant circuit during t_{on} is complex to solve, but since the power MOSFET gate capacitor voltage increases from zero to V_{cb} during t_{on}, then the average capacitor voltage during the interval is $V_{cb}/2$. Using this approximation, the ripple current component, Δi_L, is approximated as (2).

$$\Delta i_{L1} \approx \frac{V_{cb}}{2} \frac{t_{on}}{L_1} \tag{2}$$

The current at time t_1 is then approximated by (3).

$$i_{L1}(t_1) \approx \frac{Q_g}{t_{on}} - \frac{\Delta i_{L1}}{2} \tag{3}$$

Using (1)-(3), the required resonant inductance can be calculated using (4), where Q_g represents the total gate charge of the power MOSFET.

$$L_1 = \frac{V_{cb} t_{on}}{Q_g} \left(\frac{t_{on}}{4} + t_{d1} \right) \tag{4}$$

IV. Driver Optimization

An optimization procedure and analysis has been completed for the proposed driver. For the control MOSFET, Q1, this involves a tradeoff between switching loss reduction and gate loss. For the synchronous rectifier MOSFET, Q2, this involves a tradeoff between body diode conduction loss and gate loss. Using these curves, the optimal gate drive current can be selected to minimize loss.

A procedure to calculate the total gate and driver loss (P_{drive}) was given in [9]. The turn-on switching loss is given by (5), where the rise time, t_r, is given by (6) and the reverse recovery current, I_{rrQ2} is given by (7). In (5), V_{Ls1} is the voltage across the common source inductance, which is typically about 2V during the switching transition. The inductances L_{d1} and L_{s1} for Q1 and L_{d2} and L_{s2} for Q2 can be estimated using the values published in [11] for various board mounted package types. It is noted that the values published in [11] are the total board mounted package inductance, so it can be assumed that L_d and L_s are each one half of the published inductance values.

$$P_{onQ1} = \frac{1}{2} f_s \left[I_o - \frac{1}{2} \Delta i_f + I_{rrQ2} \right] \left[V_{in} - V_{Ls1} \left(1 + \frac{L_{d1}}{L_{s1}} + \frac{L_{d2}}{L_{s1}} + \frac{L_{s2}}{L_{s1}} \right) \right] t_r \tag{5}$$

$$t_r = I_o \frac{L_{s1}}{V_{Ls1}} + \frac{Q_{gdQ1} + Q_{plQ1} - Q_{thQ1}}{I_{gQ1}} + \frac{1}{2} t_{rrQ2} \tag{6}$$

$$I_{rrQ2} = \sqrt{\frac{V_{Ls1}}{L_{s1}} Q_{rrQ2}} \tag{7}$$

In (6), the reverse recovery time, t_{rrQ2}, is given by (8).

$$t_{rrQ2} = 2 \sqrt{\frac{L_{s1}}{V_{Ls1}} Q_{rrQ2}} \tag{8}$$

In (7) and (8), the reverse recovery charge, Q_{rrQ2}, is given by (9), where Q_{rr} and I_{rr} are the data sheet values.

$$Q_{rrQ2} = \frac{Q_{rr}}{I_{rr}} I_o \tag{9}$$

The turn-off switching loss is given by (10), where the fall time, t_f, is given by (11).

$$P_{offQ1} = \frac{1}{2} f_s \left[I_o + \frac{1}{2}\Delta i_f \right] \left[V_{in} + V_{Ls1}\left(1 + \frac{L_{d1}}{L_{s1}} + \frac{L_{d2}}{L_{s1}} + \frac{L_{s2}}{L_{s1}}\right)\right] t_f \quad (10)$$

$$t_f = I_o \frac{L_{s1}}{V_{Ls1}} + \frac{Q_{gdQ1} + Q_{plQ1} - Q_{thQ1}}{I_{gQ1}} \quad (11)$$

The switching loss for Q1 is the sum of the turn-on and turn-off loss in (5) and (10) and is given by (12).

$$P_{swQ1} = P_{onQ1} + P_{offQ1} \quad (12)$$

Using P_{drive} given in [9], and P_{swQ1} given by (12), the sum of the two loss components can be plotted and the optimal gate current, I_{gQ1} can be determined from the graph (at $P_{optQ1min}$). For the given application and parameters in the experimental results section, the curves are given in Fig. 14. In Fig. 14, the P_{optQ1} curve is very flat near its minimum value, so a gate current of 3A was selected as the optimal value to minimize current stress on the proposed current source driver.

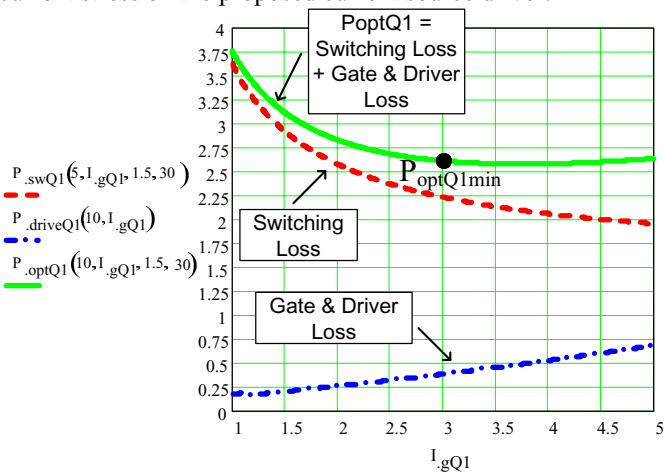

Fig. 14 Optimization curves for the control MOSFET Q1; power loss vs. gate current, IgQ1

Optimization of the SR gate current involves a tradeoff between body diode conduction, which occurs during the deadtime and switching time and the driver loss. The body diode conduction loss can be estimated using (13).

$$P_{bodyQ2} = V_{bodyQ2} I_o f_s t_{body} \quad (13)$$

In (13), the time t_{body} can be estimated using (14). Equation (14) assumes that the deadtime has been minimized to one clock cycle of the CPLD deadtime controller (explained in the following section). It also assumes that the body diode will conduct during the interval when the gate voltage is between the threshold and until the gate voltage is large enough so that the SR R_{dson} is less than about 20mOhms. The values for $Q_{gQ2}(V_{20mohm})$ and $Q_{gQ2}(V_{thQ2})$ can be estimated using the MOSFET manufacturer datasheet.

$$t_{body} = 2\left[\frac{Q_{gQ2}(V_{20mohm}) - Q_{gQ2}(V_{thQ2})}{I_{gQ2}}\right] + t_{clk} \quad (14)$$

Using P_{drive} given in [9], and P_{bodyQ2} given by (14), the sum of the two loss components can be plotted and the optimal gate current, I_{gQ2} can be determined from the graph (at $P_{optQ2min}$). For the given application and parameters in the experimental results section, the curves are given in Fig. 15. In Fig. 15, the optimal gate current is 1.3A.

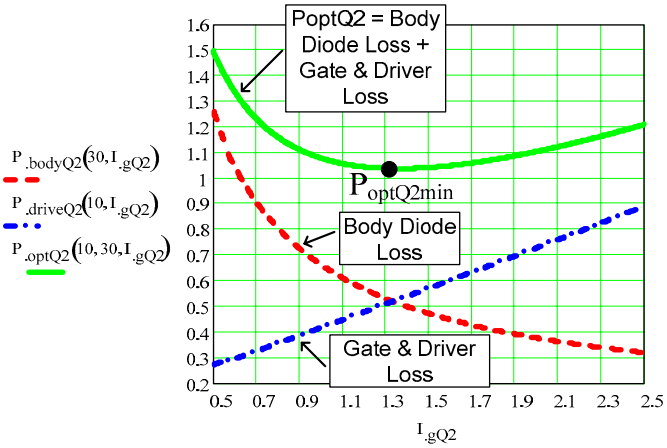

Fig. 15 Optimization curves for the synchronous rectifier MOSFET Q2; power loss vs. gate current, IgQ2

V. Logic and Level Shift Circuits

The logic required to generate the gating signals for the control switches, S1-S4 and S5-S8 is very simple. The logic was implemented using an Altera MaxII EPM240 complex programmable logic device (CPLD). An alternate discret logic implementation was presented in [9]. A block diagram of the CPLD implementation is shown in Fig. 16. It consists of edge detector (ED) and digital delay (T_del) cells that are illustrated in Fig. 17 and Fig. 18, respectively. The CPLD takes the PWM signal (PWM1) as an input and then generates the rising and falling edges for the eight control switches, S1-S8. The user configures the deadtime through the T_del blocks in the Fixed Deadtime Conrol Block, which internally generates PWM2. A 400MHz asynchronous ring oscillator clock was used for the counter and comparator within the digital delay cells.

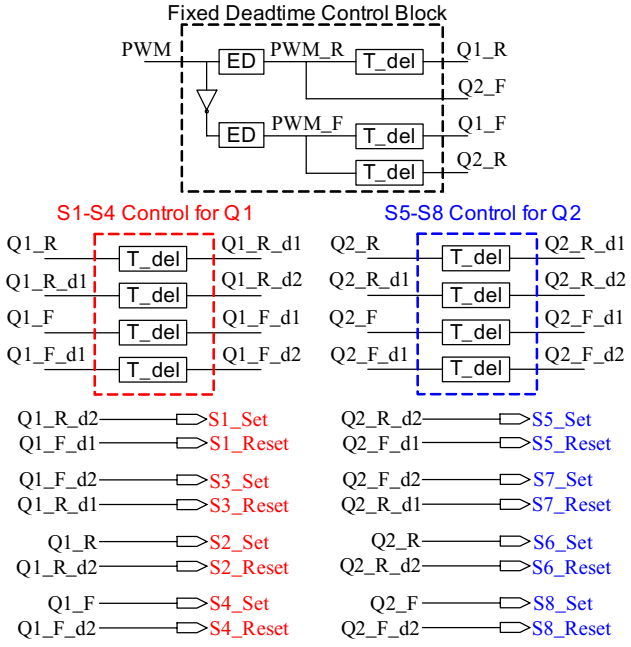

Fig. 16 Block diagram of logic implementation using the Altera MaxII EPM240

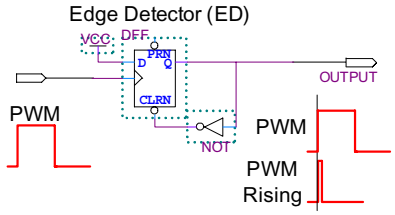

Fig. 17 CPLD implementation of the PWM edge detector

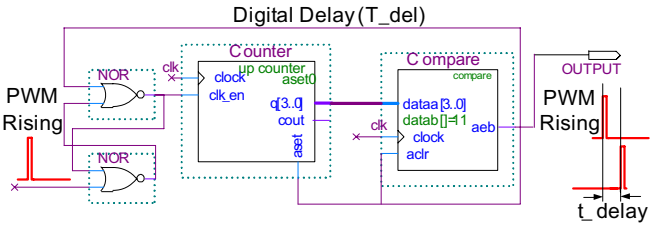

Fig. 18 CPLD implementation of the delay function

A modified version of the pulse filter level shift circuit presented in [12] was used to drive the control MOSFETs, S1-S4 and S5-S8. The level shift circuit is illustrated in Fig. 19.

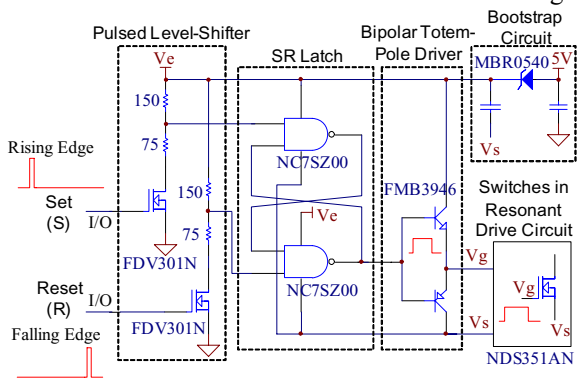

Fig. 19 Level shift circuit

VI. Experimental Results

A single phase prototype of the synchronous buck with current source gate driver was built on a 6 layer printed circuit board (PCB) as given in Fig. 20. The Q1 and Q2 gate to source waveforms and driver inductor current waveform for L1 are given in Fig. 21. The driver was built using discrete components with an Altera MaxII EPM240 CPLD used to generate the control signals. The eight control switches for the driver were NDS351AN from Fairchild. Coilcraft air core inductors (68nH for Q1 and 307nH for Q2) were used for the drivers. The synchronous buck power MOSFETs were IRF6617 for Q1 and IRF6691 for Q2 from International Rectifier. The converter was operated at 12V input and 1.3V output at 1MHz with 10V driving voltage for the MOSFETs. The buck inductor was IHLP5050FD, 330nH from Vishay.

The synchronous buck with current source gate driver was compared to an identical synchronous buck with the TI UCC27222 driver. The efficiency as a function of load is given for both drivers in Fig. 22. The converter with current source driver achieved an efficiency of 86.6% at 15A load and 81.9% at 30A load, compared to 83.8% and 77.9%, respectively for the UCC27222 driver.

The total power loss including powertrain and gate drive loss for both converters is given in Fig. 23. It is noted that at 30A load, the proposed current source gate driver saves approximately 2.5W (or 22%) compared to the conventional driver. This loss savings is significant for a multi-phase VRM. For example, in a five phase VRM, the total loss savings would be 12.5W. Another interesting observation is that if the power loss per phase is limited to 9W, the Buck converter with conventional gate drive can only provide 23A output current, while the Buck converter with current source gate driver can provide 30A (an improvement of 30%). In other words, if the total output current is 120A, we need 6 phases (120A/23A per phase) for the conventional gate driver and only 4 phases (120A/30A per phase) for the current source gate driver. This will yield a significant cost savings.

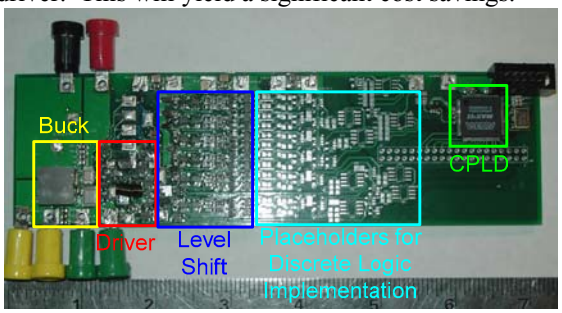

Fig. 20 Photo of the experimental prototype

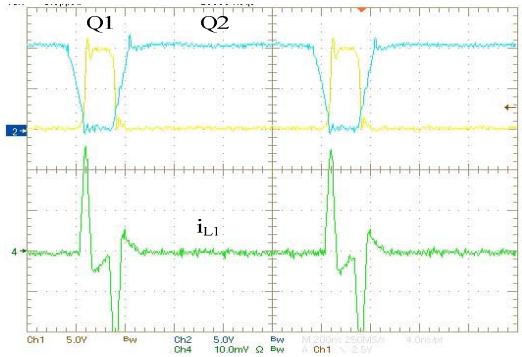

Fig. 21 Top: Current source driver control switch Q1 and SR Q2 gate signals at 1MHz (Y-axis: 5V/div and X-axis 200ns/div); Bottom: Driver current source inductor current (Y-axis: 1A/div)

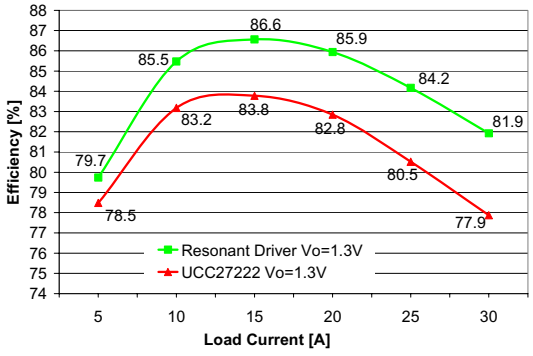

Fig. 22 Efficiency as a function of load for the current source gate driver and UCC27222 predictive gate driver at 1.3V output and 1MHz switching frequency

The proposed driver with Buck VRM was also tested at 1.5V ouput. An efficiency comparison of state of the art 12V VRMs operating at 1MHz and 1.5V output is given in Table I. The proposed current source driver achieves an efficiency of 87.3% compared to 84% for the tapped-inductor (TI) buck

converter in [13] at 12.5A. It is also noted that an efficiency improvement of 1.9% is achieved in comparison to the Toshiba synchronous buck Multi Chip Module using a semiconductor integration approach to minimize the common source inductance, which is one of the greatest contributors to switching loss.

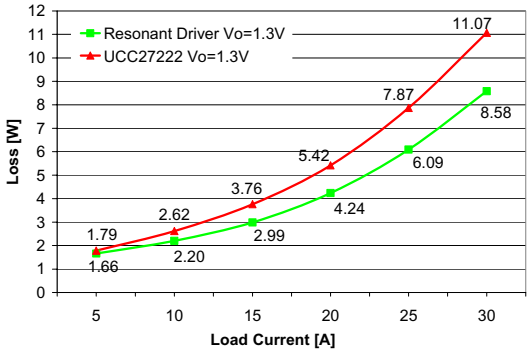

Fig. 23 Total measured loss as a function of load for the current source gate driver and UCC27222 predictive gate driver at 1.3V output and 1MHz switching frequency

Table 1 Efficiency comparison between the proposed current source driver and other state of the art VR approaches at 12V input, 1.5V output and 1MHz switching frequency

VRM Topology	Output Current/ Phase [A]	Efficiency [%]
Proposed current source driver	12.5	87.3
	20	86.9
Tapped-inductor (TI) buck converter	12.5	84
Toshiba synchronous buck Multi Chip Module (TB7001FL)	20	85

A second efficiency comparison is given in Table II for 1.3V output. The proposed current source driver achieves an efficiency of 86.3% compared to 82% for the phase-shift buck (PSB) converter in [14] at 17.5A. The current source driver achieves almost the same efficiency as the self-driven soft-switching buck-derived multiphase converter in [15] at 25A, but in terms of power density and cost, the current source driver approach has significant advantages, since the self-driven soft-switching buck requires an additional transformer.

In addition to the above performance advantages, it should be noted that the current source driver does not require a change in the multiphase buck architecture of today's VRMs, which feature low cost and simple control.

Table 2 Efficiency comparison between the proposed current source driver and other state of the art VR approaches at 12V input, 1.3V output and 1MHz switching frequency

VRM Topology	Output Current/ Phase [A]	Efficiency [%]
Proposed current source driver	17.5	86.3
	25	84.2
Soft-switching phase-shift buck (PSB) converter	17.5	82
Self-driven soft-switching buck-derived multiphase converter	25	84.7

VII. Conclusions

A new current source gate drive circuit has been proposed for high efficiency synchronous buck VRMs. The proposed circuit achieves quick turn-on and turn-off transition times to reduce switching loss and conduction loss. The circuit consists of two sets of four control switches and two small current source inductors (68nH and 307nH) and it can drive both the control MOSFET and synchronous MOSFET in synchronous buck VRMs. The current through the current source inductance is discontinuous in order to minimize circulating current conduction loss present in other methods. An analysis, design procedure, optimization procedure and experimental results have been presented for the proposed circuit. Experimental results demonstrate an efficiency of 86.6% at 15A load and 81.9% at 30A load for 12V input and 1.3V output at 1MHz. If implemented in a 120A multiphase VRM, the proposed driver would eliminate 2 of the required phases, yielding a significant potential cost savings.

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