A Design Method for PI-like Fuzzy Logic Controllers for DC–DC Converter

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***Abstract*—This paper proposes a novel design procedure of proportional and integral (PI)-like fuzzy logic controller (FLC) for dc–dc converters that integrates linear control techniques with fuzzy logic. The design procedure allows the small signal model of the converter and linear control design techniques to be used in the initial stages of FLC design. This simplifies the small signal design and the stability assessment of the FLC. By exploiting the fuzzy logic structure of the controller, heuristic knowledge is incorporated in the design, which results in a nonlinear controller with improved performance over linear PI controllers.**

***Index Terms*—Digital control, digital pulsewidth modulation (DPWM), dynamic response, fuzzy logic control (FLC), pulsewidth modulation (PWM), switching converter.**

I. Introduction

FUZZY logic control (FLC) has been successfully applied to a wide variety of engineering problems, including dc-to-dc converters [1]–[8]. It has been shown that fuzzy control can reduce development costs and provide better performance than linear controllers [9], [10]. With advances in digital hardware and digital control techniques, it is becoming feasible to implement control schemes such as fuzzy logic for power converters [11]–[14].

Fuzzy control is an attractive control method because its structure, which consists of fuzzy sets that allow partial membership and "if... then..." rules, resembles the way human intuitively approaches a control problem. This makes it easier for a designer to incorporate heuristic knowledge of a system into the controller. Fuzzy control is of great value for problems where the system is difficult to model due to complexity, nonlinearity, and/or imprecision. DC–DC converters fall into this category because they have a time-varying structure and contain elements that are nonlinear and have parasitic components.

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Despite its advantages, there are some problems with FLC. The most significant one is that trial and error method is usually needed to design a fuzzy controller [1]–[3]. There is no systematic procedure for the design of a fuzzy controller [15]–[17]. The performance of an FLC is usually not known until the design is finished. Consequently, the stability analysis is difficult [18]–[22]. For example, we will not know the bandwidth and gain/phase margin of an FLC dc-to-dc switching converter by using the FLCs proposed in [1]–[4], [15], and [16].

On the other hand, using linear control techniques, the bandwidth and gain/phase margin [23], [24] can be determined with the small signal transfer function, and the stability of the system can be satisfied.

Therefore, it is desirable to explore a design method for FLC that can achieve a predetermined small signal transfer function. In this way, the small signal characteristics of the FLC are known, and the large signal characteristics of the FLC can be designed to be better than the conventional linear control methods.

In this paper, a method that integrates the advantages of linear control techniques and FLC is developed. With this method, linear models and linear control techniques are used in the initial design of the fuzzy controller. This initial controller has exactly the same response as a linear controller, such as proportional–integral (PI) controller, proportional–integral–differential (PID) controller, or proportional–differential (PD) controller. As a result, its stability and small signal dynamic performance can be assessed using linear control techniques and the small signal model of the converter.

By capitalizing on the fuzzy logic implementation of the controller, heuristic knowledge can be incorporated. This can give an improved nonlinear controller that outperforms its linear counterpart initially designed. The improvement can be made so that it does not compromise the stability or performance of the controller for small signals. In addition, better large signal dynamic performance can be achieved. The major advantage of the proposed design method for FLC is that compared to other methods [1]–[3], [25], the trial and error effort in the design procedure is greatly reduced. In addition, the small signal performance/stability of the proposed system is already known before the design is finished. In this paper, this methodology is developed using PI controllers as an example. A similar methodology can also be used for PD and PID controllers.

The organization of this paper is as follows: Section II discusses a simple relationship between FLC and linear PI

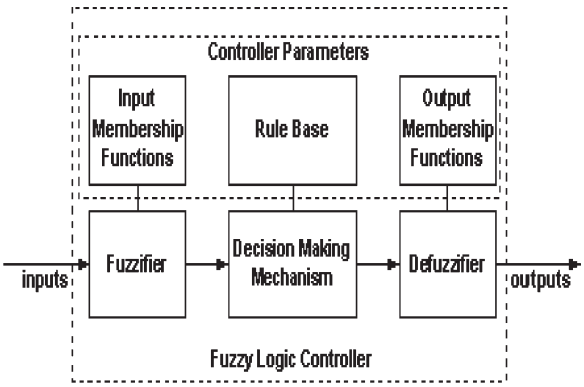

Fig. 1. Block diagram of FLC.

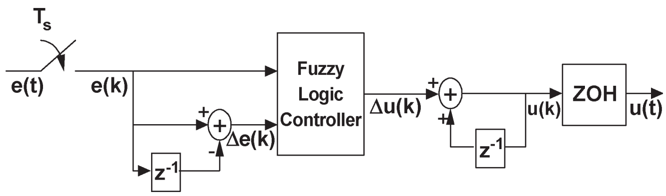

Fig. 2. Digital implementation of a PI-like FLC.

control. Section III uses this relationship to develop a design procedure for FLCs that combines the benefits of linear control techniques and FLC. Section IV will give a design example using this procedure, and simulation/experimental results are given. Conclusions are summarized in Section V.

II. Relationship Between PI-Like FLC and Linear PI Controller

This section discusses the relationship between a PI-like FLC and a digital linear PI controller. The analysis shows that the FLC can be designed to have exactly the same performance as a digital PI controller.

The block diagram for an FLC is given in Fig. 1.

In this paper, a PI-like FLC is used as an example. The inputs of the FLC are the error and the change of error. The output is the incremental change of the control signal. Usually, an FLC is implemented using digital hardware such as a digital signal processor or field-programmable gate arrays [1]. The block diagram for a digital implementation of a PI-like FLC is given in Fig. 2.

The error signal e is sampled with a sample period T_s. The change of error Δe is computed as

$$\Delta e(k) = e(k) - e(k-1) \tag{1}$$

where k is the sample number, and z^{-1} represents the unit time delay. The error $e(k)$ and the change of error $\Delta e(k)$ are fed into the FLC shown in Fig. 2. The output of the FLC is an incremental change of the control signal $\Delta u(k)$. Using a digital approximation for integration, the control signal $u(k)$ is obtained as

$$u(k) = \Delta u(k) + u(k-1). \tag{2}$$

A zero-order hold is assumed between samples to obtain the continuous control output $u(t)$.

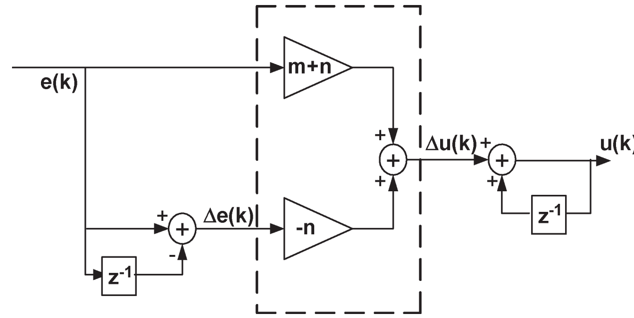

Fig. 3. Block diagram representation of (8).

This controller will now be compared to a digital PI controller to obtain a relationship between controllers. The transfer function for a continuous PI controller $C(s)$ with parameters a and G is given by

$$C(s) = \frac{U(s)}{E(s)} = G\frac{a \cdot s + 1}{s}. \tag{3}$$

Various methods exist for finding the discrete equivalent of a continuous controller [11]. It should be noted that there is no exact digital equivalent for a continuous controller because a continuous controller has access to the complete time history of the error signal while a digital controller has access only to samples of this signal [26].

The bilinear transformation

$$s = \frac{2}{T_s}\left(\frac{1-z^{-1}}{1+z^{-1}}\right) \tag{4}$$

is one method to find a discrete equivalent of a continuous controller.

Applying the bilinear transformation, a discrete equivalent $C(z)$ for $C(s)$ will be derived as

$$C(z) = \frac{U(z)}{E(z)} = \frac{m \cdot z + n}{z - 1} \tag{5}$$

where the parameters m and n are given by

$$m = G\left(a + \frac{T_s}{2}\right) \tag{6}$$

$$n = G\left(\frac{T_s}{2} - a\right). \tag{7}$$

The transfer function of (2) can be expressed as a difference equation

$$u(k) = (m+n)e(k) - n\left(e(k) - e(k-1)\right) + u(k-1). \tag{8}$$

A block diagram representation of this difference equation is illustrated in Fig. 3. The difference between Figs. 2 and 3 is that the dashed box in Fig. 3 is replaced by a two-input single-output FLC in Fig. 2. It is noted that this dashed box in Fig. 3 has the relationship

$$\Delta u(k) = (m+n)e(k) - n \cdot \Delta e(k). \tag{9}$$

Considering a fuzzy controller with the following constraints, the input membership functions are triangular except

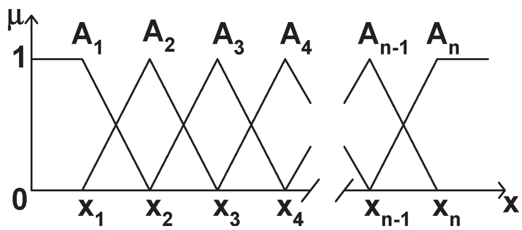

Fig. 4. Input membership functions of FLC.

for the leftmost and rightmost membership functions, as shown in Fig. 4.

The variable x in this figure is a generic variable; in the case of the PI-like FLC given in Fig. 2, x could represent the error e or the change in error Δe. The membership functions are not necessarily evenly distributed, as illustrated in Fig. 4, and are arranged so that at most two have nonzero membership (are active) for any value of the input. Furthermore, the sum of the membership for all active fuzzy sets is exactly one.

With this description of the membership functions, if $x_1 < x < x_n$, membership can be calculated as

$$\mu_{Ak+1}(x) = \frac{x - x_k}{x_{k+1} - x_k} \quad (10)$$

$$\mu_{Ak}(x) = 1 - \frac{x - x_k}{x_{k+1} - x_k} = 1 - \mu_{Ak+1}(x) \quad (11)$$

where μ_{Ak} is the membership of x to A_k, μ_{Ak+1} is the membership of x to A_{k+1}, x_k is the point where x has full membership to A_k, and x_{k+1} is the point where x has full membership to A_{k+1}. There are two exceptions where (10) and (11) cannot be used to calculate membership. If $x < x_1$, then $\mu_{A1}(x) = 1$, and membership is zero for all the other fuzzy sets. If $x > x_n$, then $\mu_{An}(x) = 1$, and membership is zero for all the other fuzzy sets.

The proposed fuzzy controller is defined to be a Sugeno-type FLC. This means that the output membership functions are singletons (crisp values). This fuzzy controller has rules of the form "If e is A_k, and Δe is B_k, then $\Delta u = \Delta u_{AkBk}$," where A_k and B_k are fuzzy sets on the error and change of error inputs, respectively. The "and" operation in the rule antecedent is performed by multiplication. Active rules are combined by the "or" operation, which is accomplished by addition. For example, $(e, \Delta e)$ is the input to the controller, where e belongs to A_k and A_{k+1}, and Δe belongs to B_k and B_{k+1}. Because for each input at most two fuzzy sets have nonzero membership, at most four rules are activated. These rules are as follows:

1) If e is A_k, and Δe is B_k, then $\Delta u = \Delta u_{AkBk}$.
2) If e is A_{k+1}, and Δe is B_k, then $\Delta u = \Delta u_{Ak+1Bk}$.
3) If e is A_k, and Δe is B_{k+1}, then $\Delta u = \Delta u_{AkBk+1}$.
4) If e is A_{k+1}, and Δe is B_{k+1}, then $\Delta u = \Delta u_{Ak+1Bk+1}$.

The output of this FLC is the weighted sum of all the activated rules and is given by

$$\begin{aligned}\Delta u = &(\mu_{Ak} \cdot \mu_{Bk}) \cdot \Delta u_{AkBk} + (\mu_{Ak+1} \cdot \mu_{Bk}) \cdot \Delta u_{Ak+1Bk} \\ &+ (\mu_{Ak} \cdot \mu_{Bk+1}) \cdot \Delta u_{AkBk+1} \\ &+ (\mu_{Ak+1} \cdot \mu_{Bk+1}) \cdot \Delta u_{Ak+1Bk+1}. \end{aligned} \quad (12)$$

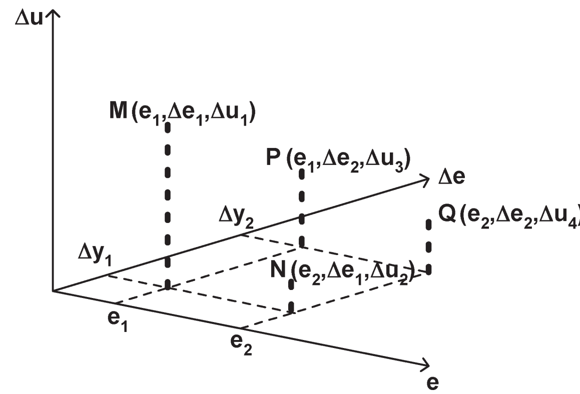

Fig. 5. Points in 3-D space.

In the case of a two-input single-output fuzzy controller, the input–output relationship of the controller can be visualized as a control surface in 3-D. These constraints result in an FLC with two properties.

Property 1: Each rule gives the controller output when the inputs to the controller have full membership to the fuzzy sets in the antecedent of that rule. The controller output in this case is equal to the consequent of the rule. If the input–output relationship of the controller is visualized as a control surface, this means that each rule will define a specific point on the control surface.

Property 2: If the consequent of each of the four active rules lies in a plane on the control surface, then all points calculated by the controller using these rules will lie in that same plane.

Proof of Property 1: Consider the rule "If e is A_k, and Δe is B_k, then $\Delta u = \Delta u_{AkBk}$." At $e = e_k$, e has full membership to A_k, and at $\Delta e = \Delta e_k$, Δe has full membership to B_k. It can be seen from (12) that if the input is $(e_k, \Delta e_k)$, then $\mu_{Ak} = 1$, $\mu_{Bk} = 1$, and $\mu = 0$ for all the other fuzzy sets. Then, the output is just $\Delta u = \Delta u_{AkBk}$, because all the other terms in (12) are zero. In terms of a control surface, this means that the point $(e_k, \Delta e_k, \Delta u = \Delta u_{AkBk})$ is a point on the surface. This is also true for all the other rules. This property arises from the restrictions placed on the membership functions that implied that when membership is equal to 1 for one fuzzy set, it is zero for all the others.

Proof of Property 2: Consider a plane defined by three points in 3-D space defined by the variables e, Δe, and Δu. The points are called M$(e_1, \Delta e_1, \Delta u_1)$, N$(e_2, \Delta e_1, \Delta u_2)$, and P$(e_1, \Delta e_2, \Delta u_3)$.

As illustrated in Fig. 5, using linear algebra, this plane can be described by

$$\begin{aligned}\Delta u = \Delta u_1 &+ \frac{e - e_1}{e_2 - e_1}(\Delta u_2 - \Delta u_1) \\ &+ \frac{\Delta e - \Delta e_1}{\Delta e_2 - \Delta e_1}(\Delta u_3 - \Delta u_1). \end{aligned} \quad (13)$$

We now try to find a fourth point Q, which also lies in the plane described by (13). It is assumed that Q lies at $e = e_2$ and $\Delta e = \Delta e_2$, and has a Δu coordinate Δu_4. To make Q lie in the plane, by using (13), we can find that $\Delta u_4 = \Delta u_2 + \Delta u_3 - \Delta u_1$.

Now, we consider an FLC with the constraints on its membership functions and inference mechanism as described above. The output of this FLC can be calculated by (10)–(12). Assuming for each input x, $x_1 < x < x_n$, so that (10) and (11) can be used. Without loss of generality, we can assume that $e_1 < e < e_2$ and $\Delta e_1 < \Delta e < \Delta e_2$. In terms of notation in (10)–(12), this means that $e_k = e_1$, $e_{k+1} = e_2$, $\Delta e_k = \Delta e_1$, $\Delta e_{k+1} = \Delta e_2$, $A_k = A_1$, $A_{k+1} = A_2$, $B_k = B_1$, and $B_{k+1} = B_2$. Substituting this notation and (11) into (12), we can get

$$\Delta u = \Delta u_{A1B1} + \mu_{A2}(-\Delta u_{A1B1} + \Delta u_{A2B1}) + \mu_{B2}(-\Delta u_{A1B1} + \Delta u_{A1B2}) + \mu_{A2}\mu_{B2} \times (\Delta u_{A1B1} - \Delta u_{A2B1} - \Delta u_{A1B2} + \Delta u_{A2B2}). \quad (14)$$

From (10), we obtain

$$\mu_{A2} = \frac{x - x_1}{x_2 - x_1} \quad (15)$$

$$\mu_{B2} = \frac{y - y_1}{y_2 - y_1}. \quad (16)$$

Assuming the points M, N, P, and Q are defined by the active rules (this is possible according to Property 1), in this case, $\Delta u_{A1B1} = \Delta u_1$, $\Delta u_{A2B1} = \Delta u_2$, $\Delta u_{A1B2} = \Delta u_3$, and $\Delta u_{A2B2} = \Delta u_4$. Substituting these values into (14), we can get

$$\Delta u = \Delta u_1 + \frac{e - e_1}{e_2 - e_1}(-\Delta u_1 + \Delta u_2) + \frac{\Delta e - \Delta e_1}{\Delta e_2 - \Delta e_1}(-\Delta u_1 + \Delta u_3) + \frac{e - e_1}{e_2 - e_1} \cdot \frac{\Delta e - \Delta e_1}{\Delta e_2 - \Delta e_1} \times (\Delta u_1 - \Delta u_2 - \Delta u_3 + [\Delta u_2 + \Delta u_3 - \Delta u_1]). \quad (17)$$

Since the last term of (17) is zero, it is simplified to

$$\Delta u = \Delta u_1 + \frac{e - e_1}{e_2 - e_1}(\Delta u_2 - \Delta u_1) + \frac{\Delta e - \Delta e_1}{\Delta e_2 - \Delta e_1}(\Delta u_3 - \Delta u_1). \quad (18)$$

As can be observed, (18) represents a plane. The input–output relationship of the linear PI controller [shown in (9)] also represents a plane. Equation (18) is exactly the same as (13) for the plane. This means that if the consequent of each of the four active rules lies in a plane on the control surface, then all points calculated by the controller using these rules will lie in that plane.

It is noted that the dashed box in the block diagram of Fig. 3 describes a plane because (9) has the form of the equation for a plane. Therefore, from Property 1, we can assign the rules of the fuzzy controller to have points that lie in the same plane as (9). This can be achieved by the following method: for the rule "If e is A_k, and Δe is B_k, then $\Delta u = \Delta u_{AkBk}$," the value for Δu_{AkBk} is initialized as $\Delta u_{AkBk} = e_k(m + n) + \Delta e_k(-n)$.

This observation shows that an FLC can be made to give the same control output as described by (9), which is the digital PI controller of (5). Therefore, an FLC can designed to match the small signal characteristics of a digital PI controller. The significance of the proposed design method is that linear control techniques and the small signal model can be used to design an FLC. This avoids the use of trial and error, and gives FLC with predictable small signal stability and performance. In addition, this illustrated that the FLC has at least the same performance as a linear PI controller.

III. Design Methodology

A flowchart of the design procedure is shown in Fig. 6. This procedure consists of three basic steps. In the first step, a conventional linear digital controller is designed. The second step transfers this controller to a fuzzy logic implementation. In the third step, this fuzzy logic implementation is exploited to incorporate heuristic knowledge resulting in a controller with improved performance.

Step 1 of Fig. 6 shows two possibilities for designing a digital controller. These two techniques include direct digital design and design by emulation. As many designers are accustomed to designing controllers in the continuous time domain, the design by emulation technique is adopted in this paper. In the case of design by emulation, the gain and zero of a continuous PI controller of (3) are chosen to provide the desired response. The bilinear transformation (4) is then used to find a digital equivalent, which results in the digital compensator of (5). Considering frequency response, this digital compensator approximates its continuous counterpart very well for frequencies below 1/10th of the sampling frequency [11].

Once a digital controller has been designed, it can be transferred to the fuzzy controller, as described in Section II. This is Step 2 of the design procedure. The first property of FLC is used. In order to meet the requirement of Property 2, $x_1 < x < x_n$, which means that the values of x_1 and x_n should be wide enough so that Property 2 will hold over the range of inputs expected by the controller. The number and distribution of the membership functions are chosen based on experience. More membership functions give more controller parameters and thus more freedom to shape the control surface. Putting membership functions closer together means that there are more parameters to describe that region of control surface and therefore more freedom to shape that region.

In Step 3, heuristic knowledge of the system and trial and error are used to improve the performance of the controller. For example, for the buck converter, the following heuristic knowledge rules can be used.

1) If the error is far from zero, the change in duty cycle should be large.
2) If the error is near zero, then the change in duty cycle should be small.
3) If the error is near zero, but the change in error is large, the duty cycle should be changed to prevent overshoot.
4) If the change in error is in the direction such that the output is approaching zero error, but the error is not close to zero, then the change in duty cycle need not be as large as if the change in error were in the opposite direction.

This knowledge can be included by altering the input membership functions or the consequence of the rules (output

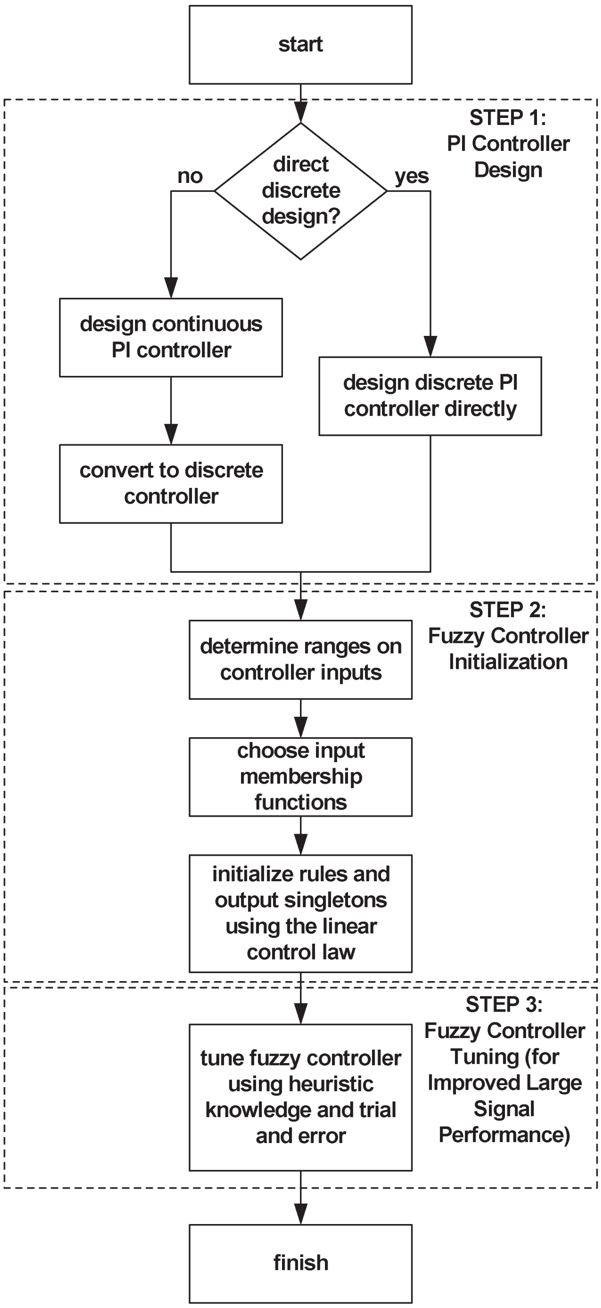

Fig. 6. Design procedure.

singletons). If the membership functions and rules are unaltered in a small region on the control surface near the zero error and zero change in error point, then the input–output relationship of the controller will remain unchanged in this region. This means the performance of the controller for inputs constrained in this region will be the same as for the initial controller and can be predicted using the small signal models and linear control techniques.

IV. Simulation and Experimental Results

The above design procedure can be applied to a buck converter. The parameters of this converter are $V_{in} = 5$ V, $V_o = 2.5$ V, $L = 1$ μH, $C = 220$ μF, RL (the resistance of inductor) $= 2$ mΩ, and ESR (equivalent series resistance) $= 1$ mΩ. The switching frequency is 400 kHz. A 10-bit ADC is used in the experiment.

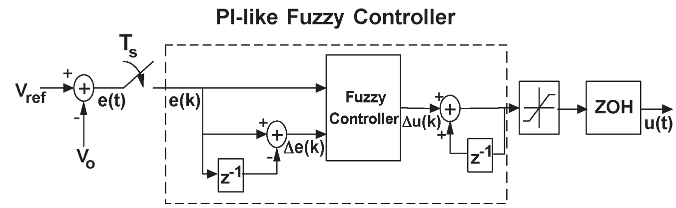

Fig. 7. PI-like FLC.

TABLE I
VALUES OF e_1 THROUGH e_9

e_1	e_2	e_3	e_4	e_5	e_6	e_7	e_8	e_9
-6	-1	-0.1	-0.016	0	0.016	0.1	1	6

TABLE II
VALUES OF Δe_1 THROUGH Δe_9

Δe_1	Δe_2	Δe_3	Δe_4	Δe_5	Δe_6	Δe_7	Δe_8	Δe_9
-6	-1	-0.1	-0.016	0	0.016	0.1	1	6

A continuous PI controller with a transfer function shown in the following equation is designed to achieve 50° phase margin and 13-kHz crossover frequency for the open-loop buck converter system with PI controller:

$$C(s) = \frac{2000(1 + 0.0001 \cdot s)}{s}. \tag{19}$$

Block diagrams of the digital PI-like fuzzy controllers are given in Fig. 7. The saturation blocks limit the duty cycle between 5% and 95%.

For the error input e, nine membership functions were designated A_1 through A_9. For the change of error input Δe, nine input membership functions were designated B_1 through B_9. Note that e_i is the point where $\mu_{Ai} = 1$, and Δe_i is the point where $\mu_{Bi} = 1$. Using the procedure provided in Fig. 6, in order to realize the small signal transfer function of (19), the values of e_1 through e_9 and Δe_1 through Δe_9 are given in Tables I and II, respectively. The rule table for the fuzzy controller in this paper is given in Table III.

The membership functions are illustrated in Figs. 8 and 9. Each entry gives the change of duty cycle Δu when membership is full to both the corresponding fuzzy sets in the rule antecedent. For instance, the entry in row 2, column 4 of Table III gives the normalized change of duty cycle if membership is full to the membership function A_2 on the error input and the membership function B_4 on the change of error input.

The rules were initialized as discussed in Section III. For example, for the rule "If e is A_2, and Δe is B_4, then $\Delta u =$

TABLE III
RULE TABLE FOR FUZZY CONTROLLER GIVING CHANGE IN DUTY CYCLE

		Change in Error								
		B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9
Error	A_1	-1.215	-0.2275	-0.0498	-0.0331	-0.0300	-0.0269	-0.0103	0.1675	1.1550
	A_2	-1.190	-0.2025	-0.0248	-0.0081	-0.0050	-0.0019	0.0147	0.1925	1.1800
	A_3	-1.185	-0.1980	-0.0203	-0.0036	-0.0005	0.0026	0.0193	0.1970	1.1845
	A_4	-1.185	-0.1976	-0.0198	-0.0032	-0.0001	0.0030	0.0197	0.1974	1.1849
	A_5	-1.185	-0.1975	-0.0198	-0.0031	0	0.0031	0.0198	0.1975	1.1850
	A_6	-1.185	-0.1974	-0.0197	-0.0030	0.0001	0.0032	0.0198	0.1976	1.1851
	A_7	-1.185	-0.1970	-0.0193	-0.0026	0.0005	0.0036	0.0203	0.1980	1.1855
	A_8	-1.180	-0.1925	-0.0147	0.0019	0.0050	0.0081	0.0248	0.2025	1.1900
	A_9	-1.155	-0.1675	0.0103	0.0269	0.0300	0.0331	0.0498	0.2275	1.2150

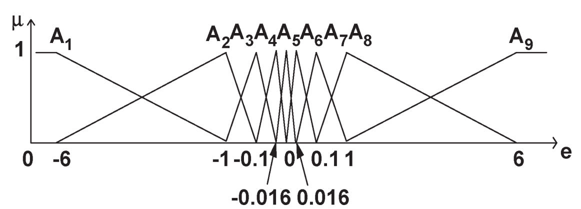

Fig. 8. Membership functions for the error.

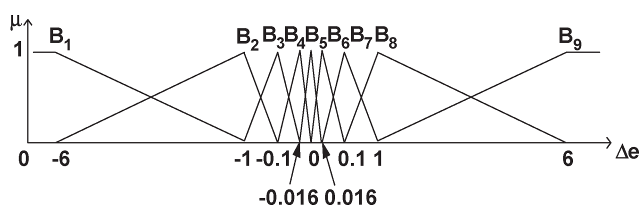

Fig. 9. Membership functions for the change of error.

u_{A2B4}," the value for u_{A2B4} is initialized to

$$\begin{aligned} u_{A2B4} &= e_2(m+n) + \Delta e_4(-n) \\ &= -1\,(0.2025 + (-0.1975)) \\ &\quad + (-0.016) * (-(-0.1975)) \\ &= -0.00816 \end{aligned}$$

where m and n can be obtained from (5)–(7).

It is expected that the FLC described in Tables I–III will provide the same small signal transfer function as shown in (19).

In order to further improve the large signal dynamic performance of the closed-loop system, the above fuzzy logic rules can be modified based on heuristic knowledge base. Rules 1 and 2 in Section III state that the gain should be increased further from the zero error point. This knowledge was included into the design by changing the definitions of the input membership functions shown in Tables I and II. New input membership functions are obtained as shown in Tables IV and V. Comparing Tables I, II, IV, and V, it can be observed that for the small signal region $-0.016 \leq e \leq 0.016$ and $-0.016 \leq \Delta e \leq 0.016$, the parameters of the FLC are unchanged after Step 3. Therefore, the small signal performance such as phase margin and crossover frequency is kept the same as designed in Step 2.

Comparison of the small signal loop response (power converter plus controller) between the digital PI controller and the proposed FLC was done by computer simulation, as shown in

TABLE IV
VALUES OF e_1 THROUGH e_9 FOR IMPROVED PERFORMANCE

e_1	e_2	e_3	e_4	e_5	e_6	e_7	e_8	e_9
-1	-0.3	-0.05	-0.016	0	0.016	0.05	0.3	1

TABLE V
VALUES OF Δe_1 THROUGH Δe_9 FOR IMPROVED PERFORMANCE

Δe_1	Δe_2	Δe_3	Δe_4	Δe_5	Δe_6	Δe_7	Δe_8	Δe_9
-1	-0.3	-0.05	-0.016	0	0.016	0.05	0.3	1

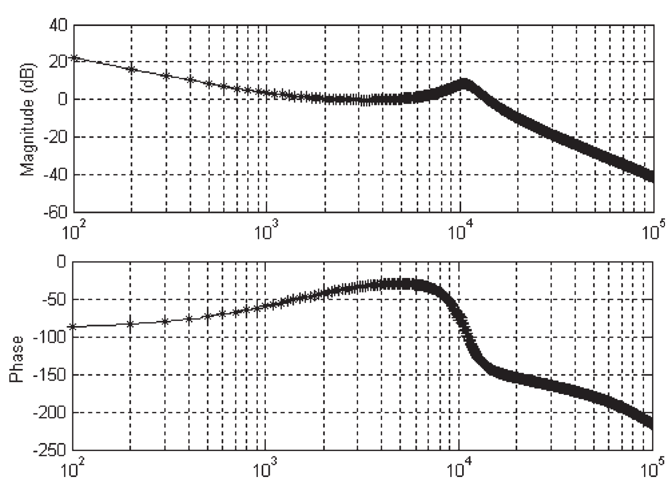

Fig. 10. Bode plots of loop response under (solid line) FLC and (star line) digital PI controller, x-axis: Hz.

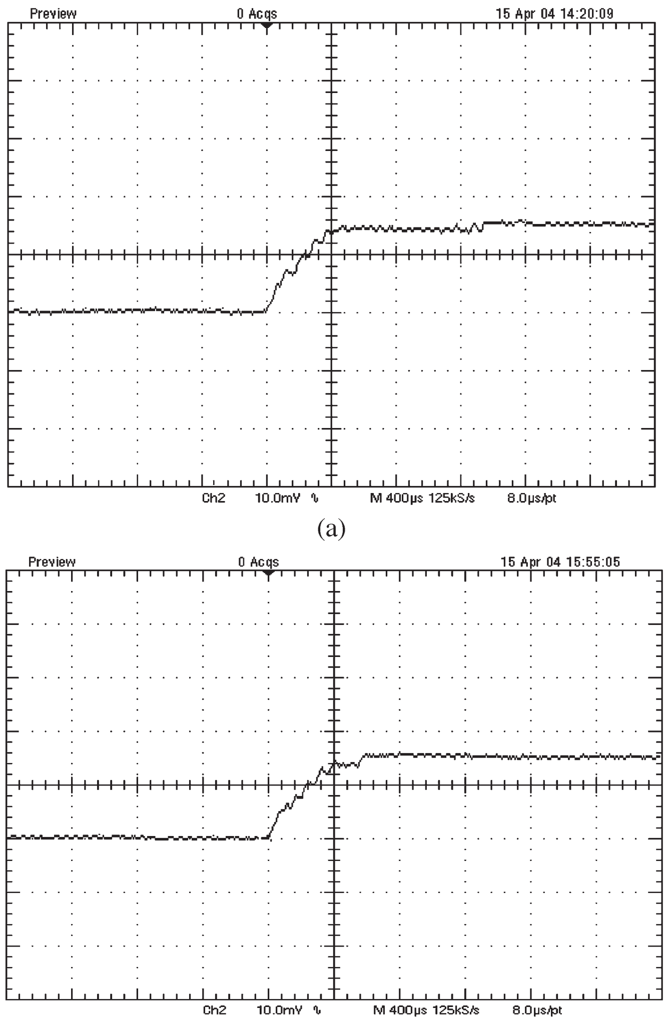

Fig. 11. Experimental results of output voltage response to small step reference change (x-axis: 400 μs/div, y-axis: 10 mV/div). (a) Digital PI controller. (b) FLC.

Fig. 10. The bode plot of the loop response using digital FLC and that using digital PI controller matches with each other very well. Their crossover frequency and phase margin are the same. Therefore, it can be concluded that these two controllers have the same small signal frequency response.

Fig. 11 shows the time-domain output voltage response when the reference voltage has a small step change (from 2.5 to 2.516 V). It is shown that the behavior of the fuzzy controller and the original digital PI controller is the same for small signals and can be predicted by the small signal model.

For large signal response, the response of the output voltage is simulated for input voltage change (as shown in Fig. 12), load current change (as shown in Fig. 13), and reference voltage change (as shown in Fig. 14). It is shown in these figures that the improved FLC has better dynamic response than the digital PI controller under large signal changes.

It can be seen from Fig. 12 that, using the digital PI controller, the overshoot due to input voltage change is 430 mV. Using the proposed FLC, the overshoot is reduced to 320 mV, which is 74% of that using the PI controller. FLC also has a short recovery time.

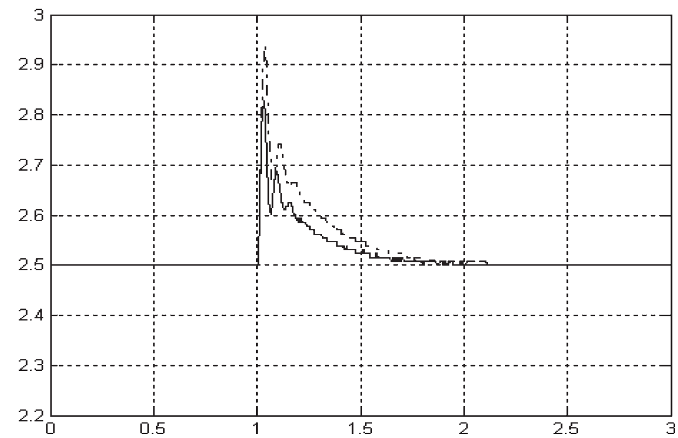

Fig. 12. Simulation results of output voltage response to input voltage change from 5 to 6 V (load current = 10 A). Solid line: FLC, dashed line: digital PI controller. x-axis: 0.5 ms/div, y-axis: 100 mV/div.

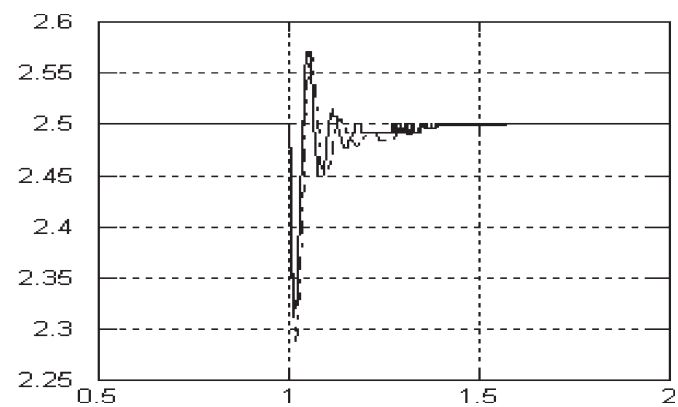

Fig. 13. Simulation results of output voltage response to load current change from 5 to 10 A. Solid line: FLC, dashed line: digital PI controller. x-axis: 0.5 ms/div, y-axis: 50 mV/div.

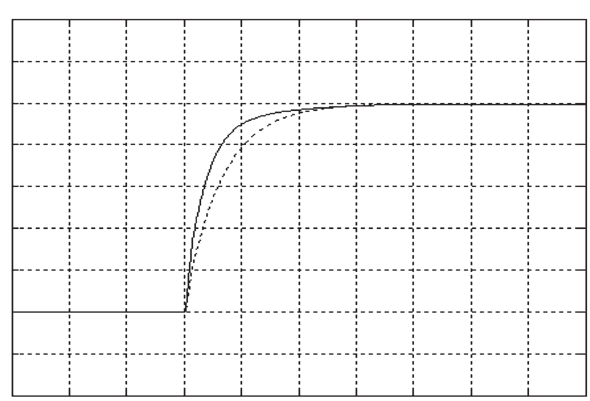

Fig. 14. Simulation results of output voltage response to reference voltage changes from 2.5 to 3 V (load current = 10 A). Solid line: FLC, dashed line: digital PI controller. x- axis: 0.5 ms/div, y-axis: 100 mV/div.

It is shown in Fig. 13 that, using the digital PI controller, the overshoot due to load current change is 210 mV. Using the proposed FLC, the overshoot is reduced to 180 mV, which is 86% of that using the PI controller.

Under the reference voltage step change, the transient time using the digital PI controller is 1.3 ms (shown in

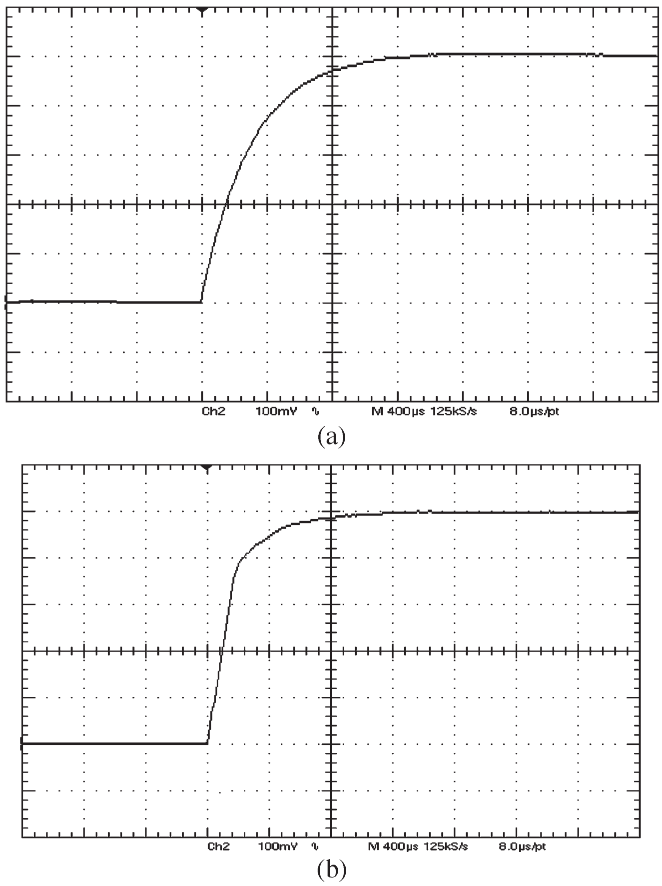

Fig. 15. Experimental results of output voltage response to large step reference change (load current = 10 A) (x-axis: 400 μs/div, y-axis: 100 mV/div). (a) Digital PI controller. (b) FLC.

Fig. 14). Using the proposed FLC, the transient time is reduced to 1.1 ms.

Fig. 15 shows the measured output voltage responses for a large step reference voltage change (from 2.5 to 3.0 V). It is observed that under the reference voltage step change, the proposed FLC has faster transient response [Fig. 15(b)] than the original digital PI controller [shown in Fig. 15(a)].

V. Conclusion

This paper presented a design procedure of FLCs for dc–dc converters. The proposed technique allows the small signal model of the converter and linear control techniques to be applied in the initial stages of fuzzy controller design. This makes assessing the performance and stability of the fuzzy controller easy. It also allows linear design techniques to be exploited. The FLC that was designed using linear techniques serves as a known starting point from which improved performance can be achieved by applying heuristic knowledge to obtain a nonlinear controller. The performance and stability of the improved nonlinear controller can still be assessed using linear control techniques for small signals if the control surface remains linear in the region in which these small signals fall. A design example was presented with simulation and experimental results to illustrate and verify this procedure.

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