A New Digital Control Algorithm to Achieve Optimal Dynamic Performance in DC-to-DC Converters

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***Abstract*—In this paper, a new control algorithm is proposed to achieve optimal dynamic performance for dc-to-dc converters under a load current change and for a given set of circuit parameters, such as the output inductor, output capacitor, switching frequency, input voltage, and output voltage. Using the concept of capacitor charge balance, the proposed algorithm predicts the optimal transient response for a dc-to-dc converter during a large signal load current change. During steady state operation, conventional current mode proportional–integral–derivative (PID) is used. During large signal transient conditions, the new control algorithm takes over. The equations needed to calculate the transient time and the required duty cycle series are presented. By using the proposed algorithm, the optimal transient performance, including the smallest output voltage overshoot/undershoot and the shortest recovery time, is achieved. In addition, since the large signal dynamic response of the power converter is successfully predicted, the large signal stability is guaranteed. Experimental results show that the proposed method produces superior dynamic performance over a conventional current mode PID controller.**

***Index Terms*—Capacitor charge balance, digital control, load transient response, proportional–integral–derivative (PID) controller, switching power supply.**

I. Introduction

As THE voltage regulation criteria for digital circuit's supply voltage becomes more stringent, there has been an increasing demand for high dynamic performance power converters. Among the many characteristics of dynamic performance, output voltage overshoot/undershoot and recovery time are often considered the most important. In general, the output voltage deviates under a load change, or an input voltage change. In order to improve the dynamic response of a dc–dc converter, the switching frequency and/or output filter can be altered. However, this method will result in either an increase in component cost or a decrease in efficiency. By improving the controller's dynamic response, the transient performance of a power converter can be improved without topology modification, thereby greatly reducing the component size and cost for high-performance converters.

Numerous control strategies [1]–[6] in analog implementation have been introduced to provide improved dynamic performance. Transient response is improved in [1] by utilizing load current feed-forward compensation. Unfortunately, this method requires a current transformer in series with the load. This may not be feasible under high output current conditions as it would present a significant voltage drop across the transformer.

Hysteretic current mode controllers, as presented in [2] and [3], provide fast dynamic response since the conventional feedback compensation network is removed; however, this method may not be suitable in many applications due to its variable switching frequency and non-zero steady-state error, as reported in [2].

In [4]–[6], various forms of hysteretic control, based on output voltage ripple, are presented. While these methods improve dynamic performance over conventional linear controllers, they all possess at least one of the following undesired attributes: 1) variable switching frequency, 2) non-zero steady-state error, and 3) operating frequencies largely dependant on the equivalent series resistance of the output capacitor (which can vary significantly with age).

In general, all forms of analog control suffer from at least one of the following conditions: 1) large component count for complex control methods, 2) vulnerability to noise, thermal conditions, component age and tolerance, and 3) tedious parameter modification procedures. Most importantly, it is impossible for any of the aforementioned analog controllers to achieve optimal dynamic response (minimal undershoot/overshoot with shortest possible settling time), as it requires complex derivation and calculation, that can only be practically derived digitally.

Compared to analog control, digital control offers many advantages such as re-programmability, reliability and simplicity of complex arithmetic. While extensive work has been conducted in designing digital controllers that mimic their analog counterparts [7]–[11], little research has been conducted to develop novel digital controller concepts that fully utilize the mathematical capabilities of such systems. In the past, typically only simple digital PI or PID controllers have been implemented. These control systems suffer from the limitations of slow compensator networks which degrade the dynamic performance of the converter.

It is demonstrated in [12], [13], that by implementing two separate control strategies for steady-state and transient conditions, the overall dynamic performance of the converter is improved. In [12], two separate sets of linear PID compensators are implemented digitally to provide larger bandwidth during transient conditions. While transient response is improved in [12], the controller is still subject to the limitations of slow compensator networks. In [13], a method combining linear voltage mode control and non-linear hysteretic control is introduced. While this method does improve dynamic response, the controller tends to "over-compensate" for load current variations, causing the output voltage to over-shoot after it recovers from a voltage drop, thereby resulting in large settling times.

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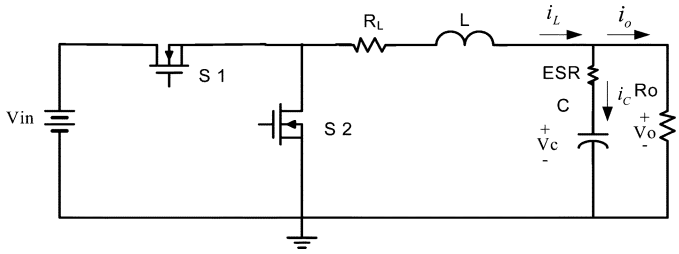

Fig. 1. Synchronous buck converter.

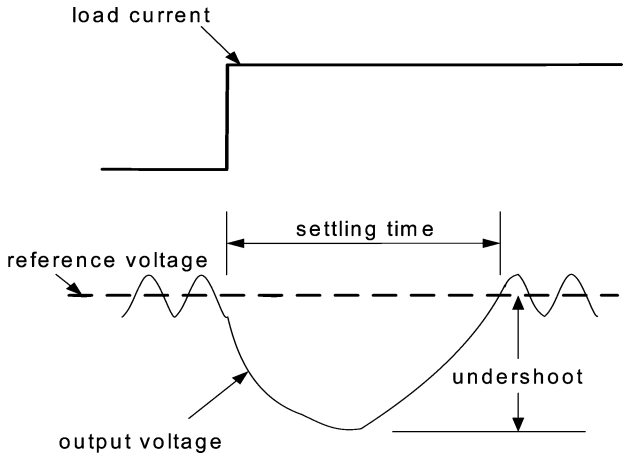

Fig. 2. Converter response to a positive load current step change.

For a Buck converter with a specified set of parameters (switching frequency, output inductor and output capacitor), there exists a best possible dynamic response/optimality condition to a load current step of any magnitude. Under this optimality condition, the shortest recovery time and the smallest overshoot/undershoot during the transient are achieved simultaneously. In [14] and [15], controllers are presented which attempt to achieve optimal dynamic response. In [14], the authors attempt to mimic optimal response by using a conventional control method. However, this approximation only produces near-optimal results and fails to minimize the voltage deviation and settling time. In addition, the implementation is very complicated. In [15], it is acknowledged that in order for a Buck converter to provide an optimal response to a rapid parameter change, the duty cycle must be set to 100% (for load current step up)/0% (for load current step down) for a specified period of time and then 0% (for load current step up)/100% (for load current step down) for an additional period. In [15], these time periods are calculated in Matlab offline and then programmed in an FPGA. The system only functions properly when the parameter variation (such as the load current change) is defined in advance. This is contrary to typical Buck converter applications.

In this paper, an algorithm is proposed which allows converters to achieve their best possible dynamic performance. It is demonstrated that by employing the principle of capacitor charge balance, a converter can achieve optimal dynamic response under a load current variation of an arbitrary magnitude.

In Section II, the concept of optimal dynamic response is introduced. In Section III, the transient response of a Buck converter under voltage mode control is analyzed in order to outline the deficiencies of conventional linear control techniques. In Section IV, the optimal transient response algorithm is proposed. This is followed by the derivation of the equations to implement the proposed method in Section V. Simulation and experimental results are presented in Section VI and the conclusions are presented in Section VII.

II. Optimal Dynamic Response

Fig. 1 illustrates the topology of a synchronous Buck converter. It is well known, that in the case of a rapid load current variation, the output voltage will deviate from its reference value for a finite period of time. Since the inductor current i_L cannot change instantaneously to correspond with the output current variation, the capacitor current i_C must compensate for the difference between i_L and i_o. Therefore, until the inductor current i_L reaches the new output current i_o, the capacitor must either charge or discharge, causing the output voltage to overshoot or undershoot the reference voltage.

Power train parameters, such as output filter components and switching frequency, are normally decided based on efficiency and steady-state requirements. The input and output voltages are determined by the system requirement. The control loop design of the converter is primarily based upon the desired dynamic response. For a given set of power train and control loop parameters, there exists a corresponding transient response to a load current step. The dynamic response of a converter can generally be characterized by the voltage undershoot/overshoot and the settling time, illustrated in Fig. 2.

It is known that different control methods will yield different dynamic responses (such as overshoot, undershoot, settling time, etc) for a given load current step. It is noted that for a specified set of power train parameters, there exists an optimal dynamic response (minimum possible undershoot/overshoot with minimum possible settling time) for a load current step change.

The primary goal is to develop a control method that allows converters to achieve this response for load current steps of any magnitude. This paper proposes a digital control method to achieve this optimal dynamic response.

III. Limitations of Conventional Control Methods During a Load Transient

Since the dynamic performance under a load current change is arguably the most important issue in power converter design, the transient response of a power converter under a large signal positive load current change will be fully discussed. In this section, the transient response of a Buck converter (Fig. 1) under voltage mode control is analyzed.

The dynamic response waveforms of a voltage mode controlled Buck converter, under a positive load current step change, are illustrated in Fig. 3. The load current steps from i_{o1} to i_{o2} at point 0. It is assumed that before point 1, the output voltage drop has not been sensed by the control circuit. Therefore, the duty cycle remains constant. As a result, the inductor current remains unchanged for the period t_0. Since the load current is greater than the inductor current, the capacitor begins to discharge as it provides the required load current.

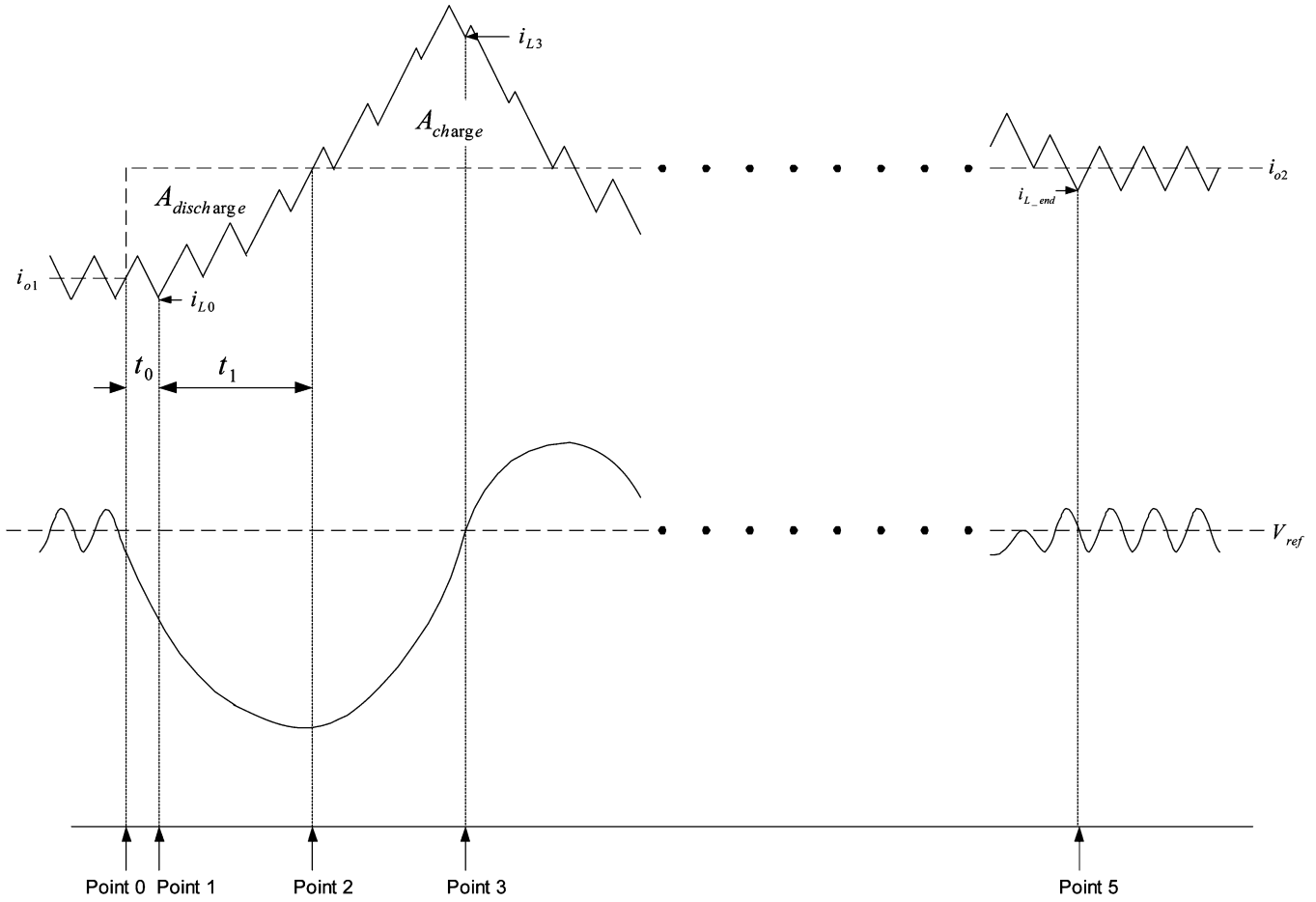

Fig. 3. Transient response of a voltage mode controlled buck converter under positive load current step change (top: inductor current, bottom: capacitor voltage).

As a result, the capacitor and output voltages decrease. At point 1, the converter begins to react to the output voltage drop. The duty cycle increases, which causes the inductor current to increase. However, before point 2, the inductor current is still lower than the load current. As a result, the capacitor voltage continues to decrease. At point 2, the inductor current is equal to the load current and the capacitor stops discharging. At this point, the capacitor voltage drop is at its maximum.

After point 2, the inductor current continues to increase and becomes greater than the load current. As a result, the capacitor begins re-charging and the output voltage rises up towards the nominal value $V_{\rm ref}$. When the value of capacitor charge, $A_{\rm charge}$, is equal to the capacitor discharge, $A_{\rm discharge}$, the capacitor voltage reaches its nominal value, $V_{\rm ref}$, at point 3. It can be observed in Fig. 3, that at point 3, the inductor current i_{L1} is larger than the load current i_{o2}, indicating that the capacitor current is non-zero. Therefore, the capacitor will continue to charge and the voltage will continue to rise. The controller will now compensate for this overshoot by decreasing its duty cycle. This cyclical pattern will continue for many cycles until the converter fully recovers at point 5, thus causing the recovery time to be sub-optimal. This analysis indicates that voltage mode control cannot achieve the best possible dynamic performance.

Generally speaking, the design objectives for voltage mode control, or other conventional linear control methods are to make the steady state error converge to zero and to achieve wide bandwidth with sufficient phase margin. The design is based on frequency domain analysis and does not focus on the time-domain response. Additionally, since the controller is based solely on the small signal response of the converter, it cannot possibly guarantee optimal large signal dynamic performance. Therefore, a new method should be proposed to achieve the best possible dynamic response.

IV. Proposed Optimal Transient Response Algorithm

As previously mentioned, for any given power converter and its related parameters, there exists an optimal dynamic response (minimum undershoot/overshoot and minimum recovery time) to a load current change. Fig. 4 shows the optimal response.

In order to achieve the optimal dynamic response, the following can be observed from Fig. 4:

1) Following a positive load current step change (at Point 0), the inductor current can not change instantaneously and therefore a portion of the load current is supplied by the output capacitor. The capacitor voltage drop is expressed in

$$C\frac{dv_C}{dt} = i_c = i_L - i_o$$
$$\Delta v_c = \frac{1}{C}\int_{\rm Point0}^{\rm Point2}(i_L - i_o)dt. \quad (1)$$

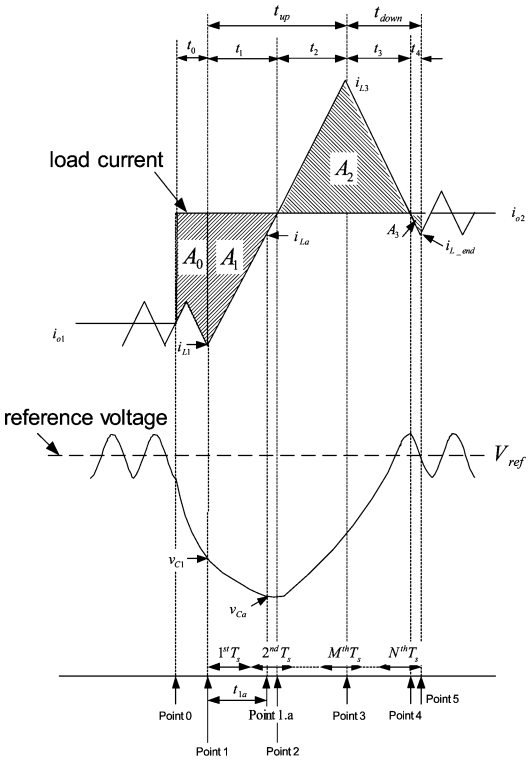

Fig. 4. Optimal inductor current path for load current positive change (top: inductor current, bottom: capacitor voltage).

In order to minimize Δv_c, and consequently, Δv_o, A_0 and A_1 (as shown in Fig. 4) must be minimized. The capacitor discharge portion A_0 occurs prior to the controller detecting the transient and is considered an unavoidable capacitor charge loss. A_0 may be reduced by decreasing the sampling time. Thus, in order to ensure that the voltage drop is minimized, the controller must minimize the capacitor discharge portion A_1.

2) In order to minimize A_1 (and thus Δv_o), the duty cycle must be set to its maximum duty cycle (100%) during t_1 in order to allow the inductor current to increase at its maximum slew rate. The maximum positive inductor slew rate is expressed in

$$\frac{di_L}{dt} = \frac{v_{\text{in}} - v_o'}{L}. \tag{2}$$

Allowing the inductor current to increase at its maximum slew rate minimizes t_1 and thus minimizes the integral period in (1). Conversely, if the duty cycle were not set to its maximum for t_1, the voltage drop would not be minimized as excess charge would be removed from the capacitor, as demonstrated in Fig. 5.

3) The capacitor re-charges during periods t_2 and t_3 (as shown in Fig. 4) since the inductor current is greater than the load current. The output voltage will rise and return to its nominal value at the instant that the charge previously removed from the capacitor equals the charge delivered to the capacitor. If the inductor current reaches its new steady state value at the instant when the output voltage equals the reference voltage, the converter is considered recovered.

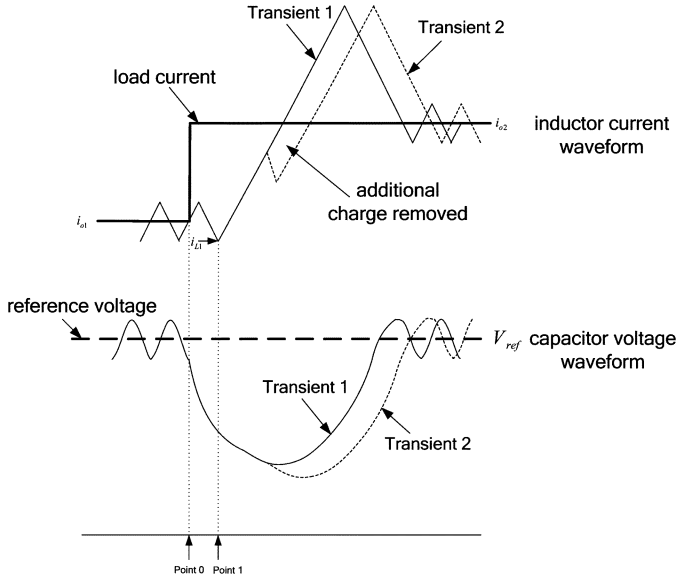

Fig. 5. Alternate inductor current path of a Buck converter under a load current change.

4) As previously mentioned, t_1 was minimized by initially setting the duty cycle to 100%. This, in turn, minimized A_1 ensuring that the necessary recharge portion A_2 is minimal. Since the required recharge portion A_2 is minimized, it is necessary to minimize the time required to deliver this charge. Referring to Fig. 4, in order to minimize the time required (t_2+t_3) to deliver A_2, the inductor current should be allowed to vary at its maximum slew rates [(2) for t_{up} and (3) for t_{down}]. Since A_2 is fixed, this will effectively maximize the height of A_2, thereby minimizing the base of A_2 $(t_2 + t_3)$. Thus, the duty cycle is set to 100% for t_{up} and 0% for t_{down}

$$\frac{di_L}{dt} = \frac{-v_o'}{L}. \tag{3}$$

The main concept of the optimal path is that t_{up} and t_{down} are chosen such that the charge removed from the capacitor is equal to the charge supplied to the capacitor at Point 5.

Fig. 4 illustrates the optimal response of a Buck converter to a positive load current step.

A similar analysis can be performed for a negative current step change.

The proposed algorithm precisely calculates the value of t_{up} and t_{down} in real time so that the optimal response is realized for a load current variation of any magnitude. Furthermore, the algorithm calculates the new steady-state duty cycle value so that the controller may undergo a smooth transition from transient to steady-state mode without any switchover. Therefore, the shortest possible transient time is realized.

V. Derivation of the Optimal Control Algorithm

From the analysis in the previous section, the best possible dynamic response can be achieved by setting the duty cycle to

its maximum value (usually 100%) for a period of $t_{\rm up}$ so that the inductor current can increase at its maximum slew rate to provide the increased load current and also to recharge the output capacitor. Immediately following $t_{\rm up}$, the duty cycle is set to its minimum value (usually 0%) for a period of $t_{\rm down}$ and the inductor current decreases at its maximum slew rate. The value of $t_{\rm up}$ and $t_{\rm down}$ should be selected such that at the end of $t_{\rm down}$, the output voltage recovers to its original voltage level and the inductor current reaches its new steady state value. Therefore, in order to achieve the best possible dynamic response, it is necessary to determine the rising time $(t_{\rm up})$ of the inductor current and the falling time $(t_{\rm down})$ of the inductor current. In addition, the new duty cycle, $D_{\rm new}$, should also be estimated.

The dynamic equations of a synchronous Buck converter are previously expressed in (1)–(3). Equation (2) is applicable when $S1$ is on and $S2$ is off. Equation (3) is applicable when $S1$ is off and $S2$ is on.

In (1)–(3), $v_{\rm in}$ represents the input voltage, v_c represents the capacitor voltage, i_c represents the capacitor current, i_L represents the inductor current, i_o represents the load current and v_o' represents the equivalent output voltage including the system losses. v_o' is specified in (4), which includes the output voltage, v_o, and system loss, $r_{\rm loss}$

$$v_o' = v_o + i_o r_{\rm loss}. \tag{4}$$

The output voltage is defined in (5), where ESR represents the equivalent series resistance of the output capacitor

$$v_o = v_C + i_C \mathrm{ESR} \tag{5}$$

$r_{\rm loss}$ is defined in (6), where R_L represents the winding resistance of the filter inductor, $R_{\rm on}$ represents the MOSFET on-resistance and $R_{\rm switching}$ represents the equivalent MOSFET switching loss

$$r_{\rm loss} = R_L + R_{\rm on} + R_{\rm switching}. \tag{6}$$

The key concept to achieve the optimal transient response is to precisely predict the rising and falling periods of the transient, $t_{\rm up}$ and $t_{\rm down}$. Calculating $t_{\rm up}$ and $t_{\rm down}$ requires values for $i_L, v_{\rm in} v_o$ and i_o. In real time implementation $i_L, v_{\rm in}$ and v_o can be directly measured, however i_o must be estimated.

In the proposed algorithm, the transient time is calculated in six steps.

1) Estimate the new load current i_{o2}
2) Calculate the inductor current rising and falling slew rates.
3) Calculate the capacitor discharge portion A_0.
4) Calculate t_1 and the capacitor discharge portion A_1.
5) Calculate t_4 and the capacitor discharge portion A_3.
6) Calculate the capacitor charge portion A_2 and the time periods t_2 and t_3.

In order to simplify the calculations, four assumptions are made.

1) During the transient period, the output voltage variation is small, so it can be assumed that the output voltage is approximately equal to $V_{\rm ref}$.
2) After point 1, the load current remains constant at i_{o2} and load oscillations have subsided.
3) The input voltage remains constant during the transient.
4) Current feed-forward and load-line regulation methods are not utilized in the proposed optimal control algorithm.

Using these assumptions, the equations to calculate the transient time are given as follows.

Step 1) **Estimate the new load current i_{o2}**

To estimate the new load current value, the output voltage, v_{o1}, the inductor current i_{L1} at point 1, the output voltage, $v_{\rm oa}$, and the inductor current, i_{La} at point 1.a are sensed. The time period between these two sample points, t_{1a}, is known. During the time interval, t_{1a}, the change of output capacitor charge can be written as (7), and rewritten as (8) as follows:

$$C\Delta v_C = C(\Delta v_0 - \Delta i_C \mathrm{ESR}) \tag{7}$$

$$C \cdot \Delta_{v_c} = C \cdot [(v_{0a} - v_{01}) - (i_{ca} - i_{c1}) \cdot \mathrm{ESR}] = \int_{\mathrm{po\,int}\,1}^{\mathrm{po\,int}\,1,a} (i_L - i_{o2}) \cdot dt. \tag{8}$$

In (8), i_{Ca} and i_{C1} are the capacitor currents at point 1.a and point 1 respectively. Since $i_{C1} = i_{L1} - i_{o2}, i_{Ca} = i_{La} - i_{o2}$, and $i_{C2} - i_{C1} = i_{La} - i_{L1}$, (8) can be approximated in discrete-time form in (9) as follows:

$$C\cdot(v_{0a}-v_{01}) = \frac{1}{2}(i_{L1}+i_{La})\cdot t_{1a} - i_{o2}\cdot t_{1a} + (i_{La}-i_{L1})\cdot C\cdot \mathrm{ESR}. \tag{9}$$

From (9), the new load current i_{o2} can be estimated using (10) as follows:

$$i_{o2} = \frac{1}{2}(i_{L1}+i_{La}) - \frac{C\cdot(v_{0a}-v_{01}) - C\cdot(i_{La}-i_{L1})\cdot \mathrm{ESR}}{t_{1a}}. \tag{10}$$

Step 2) **Calculate the inductor current rising and falling slew rates**

Considering the losses of the power stage, the inductor current rising and falling slew rates can be obtained from (2) and (3), respectively. Here, for simplicity, an approximation is made for v_o', as defined in

$$v_o' \approx V_{\rm ref} + i_{o2} \cdot r_{\rm loss}. \tag{11}$$

Step 3) **Calculate the capacitor discharge portion A_0**

The capacitor discharge portion A_0 can be estimated by using the change of the capacitor voltage during the time period t_0. Assuming that the capacitor voltage ripple is very small, the capacitor discharge portion A_0 can be obtained using

$$A_0 = C \cdot (v_{C0} - v_{C1}) \approx C \cdot (V_{\rm ref} - v_{C1}) = C \cdot (V_{\rm ref} - v_{o1} + i_{C1} \cdot \mathrm{ESR}) = C \cdot (V_{\rm ref} - v_{o1} + (i_{L1} - i_{o2}) \cdot \mathrm{ESR}). \tag{12}$$

Step 4) **Calculate t_1 and the capacitor discharge portion A_1**

Based on the estimated load current i_{o2} and the inductor current rising slew rate given by (2), the interval t_1 and the capacitor discharge A_1 can be obtained utilizing simple geometry, as defined in

$$t_1 = \frac{i_{o2} - i_{L1}}{(v_{\text{in}} - v'_o)/L} \tag{13}$$

$$A_1 = \frac{1}{2} t_1 (i_{02} - i_{L1}). \tag{14}$$

Step 5) **Calculate t_4 and the capacitor discharge portion A_3**

When the transient ends, the new steady state duty cycle is obtained using

$$D_{\text{new}} = \frac{v'_a}{v_m}. \tag{15}$$

The value of the new steady state inductor current ripple can be expressed as

$$I_{\text{ripple}} = (1 - D_{\text{new}}) \cdot T_s \cdot \frac{v'_o}{L}. \tag{16}$$

Therefore, the new steady state inductor current valley value i_{L_end} is given by

$$i_{L\_\text{end}} = i_{a2} - \frac{1}{2} l_{\text{ripple}} = i_{o2} - \frac{1}{2} \left(1 - \frac{v'_o}{v_{\text{in}}}\right) \cdot T_s \cdot \frac{v'_o}{L}. \tag{17}$$

Based on the estimated load current, i_{o2}, the inductor current falling slew rate, given by (3), and the new steady state inductor current valley value, given by (17), the interval t_4 and the capacitor discharge portion, A_3 can be obtained geometrically using

$$t_4 = \frac{i_{o2} - i_{L\_\text{end}}}{v'_o 1L} \tag{18}$$

$$A_3 = \frac{1}{2} t_4 \cdot (i_{02} - i_{L\_\text{end}}). \tag{19}$$

Step 6) **Calculate the capacitor charge portion A_2 and the time periods t_2 and t_3**

It is noted in Fig. 4 that by the end of t_4 (or at point 5), the charge removed from the capacitor is equal to the charge delivered to the capacitor, thus (20) must be satisfied

$$A_0 + A_1 + A_3 = A_2. \tag{20}$$

During the time period t_2, the inductor current slew rate is given by (2). During the time period t_3, the inductor current slew rate is given by (3). The capacitor charge area A_2 can be derived geometrically in (21), where i_{L3} is given by

$$A_2 = \frac{1}{2}(t_2 + t_3) \cdot (i_{L3} - i_{02}) \tag{21}$$

$$i_{L3} = i_{o2} + \frac{v'_0}{L} \cdot t_3 = i_{o2} + \frac{v_{\text{in}} - v'_0}{L} \cdot t_2. \tag{22}$$

Using (22), the ratio t_2/t_3 can be derived as

$$t_2/t_3 = \frac{v'_o}{v_{\text{in}} - v'_o}. \tag{23}$$

Therefore, using (12), (14), (19), and (21)–(23), the optimal transient time t_2 and t_3 can be derived as

$$t_2 = \sqrt{\frac{A_0 + A_1 + A_3}{\frac{1}{2}\frac{v_{\text{in}}}{v_o}, \frac{v_{\text{in}} - v'_o}{L}}} \tag{24}$$

$$t_3 = \frac{v_{\text{in}} - v'_o}{v'_o} t_2. \tag{25}$$

By using (13), (18), (24), and (25), the optimal transient time is expressed as

$$T_{\text{opt}} = t_1 + t_2 + t_3 + t_4. \tag{26}$$

From the above equations, it can be observed that the proposed optimal transient response method primarily uses division and square root operations to calculate t_1 through t_4. If these two calculation operations were saved and implemented by look-up tables, the control algorithm can be easily implemented using ASIC (Application Specific Integrated Circuit).

Using the values of t_1, t_2, t_3, and t_4, the minimum number of switching cycles and their corresponding duty cycles can be predicted. However, it is unrealistic to assume that t_{up} and t_{down} will be an integer multiple of the switching period. Since, the duty cycle can only vary once per switching period, two possible cases for t_{opt} must be considered and compensated for:

1) t_{opt} is an integer multiple of T_s, where T_s is the switching period, which is also the sampling period;
2) t_{opt} is not an integer multiple of T_s.

In the first case, it is assumed that $t_{\text{opt}} = \text{N}T_s$, and t_{up} is greater than $(M-1)T_s$ and less than MT_s, where M are N are integers. To achieve the best possible transient response, for the 1st to $(M-1)$th switching cycles, the duty cycle is 100%. For the Mth switching cycle, the duty cycle must be changed according to (27) and for $(M+1)$th to Nth switching cycles, the duty cycle is 0%

$$d = \frac{t_{\text{up}} - (M-1)T_s}{T_s}. \tag{27}$$

In the second case, t_{opt} is not an integer multiple of T_s. Instead, t_{opt} can be expressed as $t_{\text{opt}} = NT_s + t_{\text{residual}}$, where $t_{\text{residual}} < T_s$ and t_{up} is greater than $(M-1)T_s$ and less than MT_s, as shown in Fig. 6. In this situation, the duty cycle values for the first to Nth switching cycle are the same as that of the previous case. However, for the last $(N+1)$th switching cycle, an approximate method is used. As shown in Fig. 6, the duty cycle is set to d_{N+1} given by (28), where i_{LN} is the inductor current at the end of switching cycle N. Therefore, the inductor current can still reach its new steady state valley value, i_{L_end}, at the end of the transient response (shown as the solid line shown in Fig. 6). The voltage error caused by this approximation method is very small compared to the output voltage drop during the load current step change, and thus, its influence can be neglected

$$d_{N+1} = \frac{v_o T_s + (i_{L\_\text{end}} - i_{LN})L}{v_{\text{in}} T_s}. \tag{28}$$

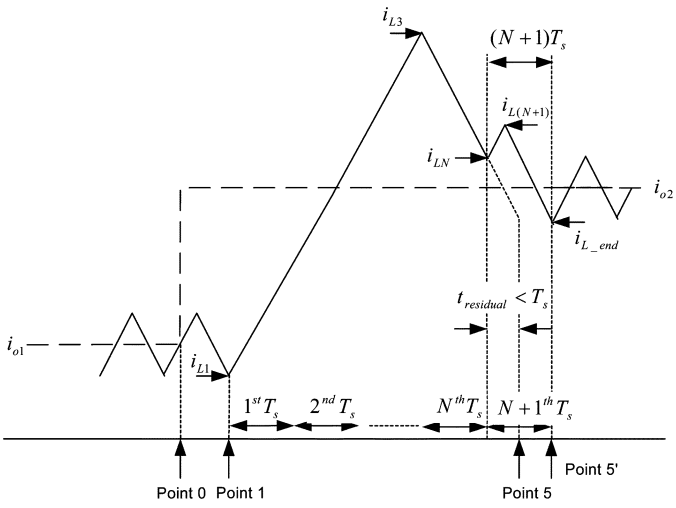

Fig. 6. Optimal inductor current transient for positive load current change when $T_{\rm opt} = NT_s + T_{\rm residual}$.

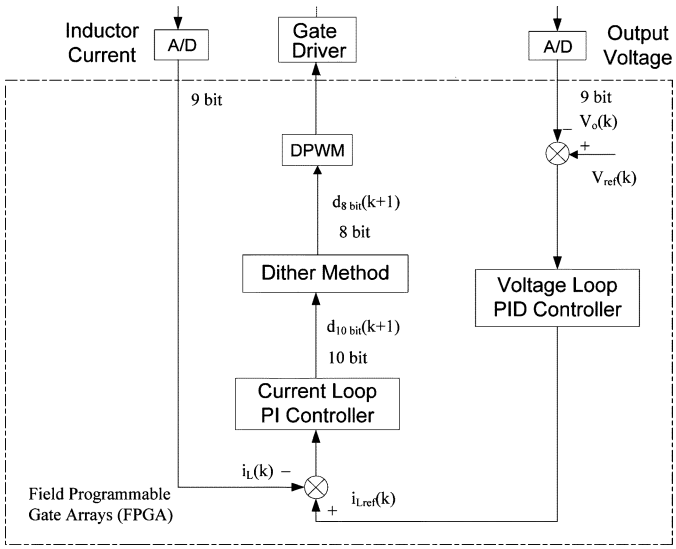

Fig. 7. Block diagram of current-mode PID controller.

In the proposed control system implemented with a buck converter, a PID controller is used to regulate the power converter during steady state periods and any small signal transient response periods. During a large transient, after the proposed algorithm completes at point 5, the control is switched back to the PID controller. Before the control algorithm is switched back to the PID controller, the algorithm calculates the new steady state values $I_{\rm Lnew}$ (if current mode control is used) and $D_{\rm new}$ for the PID controller, and resets the outputs of the PID controller to these values.

The value of $D_{\rm new}$ is obtained using (15). Since, in steady state, the inductor current is sensed 0.3 T_s before the switch is turned on and the slew rate during MOSFET turn-off period is—v_o'/L, the steady state reference inductor current value $I_{\rm Lnew}$ for a current mode PID controller can be obtained using

$$I_{\rm Lnew} = i_{L\_{\rm end}+0.3\cdot v_o'\cdot\frac{T_s}{L}}. \tag{29}$$

Compared to current-mode control, only one additional real-time measurement is required: the input voltage. This addition can be accomplished without significant cost. While some converter parameters must be estimated by the designer, small errors will not significantly affect the performance of the proposed algorithm.

In order for the proposed controller to be transferred from one converter to another, the power train parameters and switching speed must be reprogrammed. This proves advantageous over traditional analog designs which require the compensator's components to be replaced.

In this section, the equations of the proposed optimal control algorithm were derived for a positive load current change. In order to apply the algorithm to a negative load current change, the operation principles and equations are virtually identical to those detailed above. It is noted that if the load current changes again before the output voltage recovers due to previous transient, the system might oscillate. Fortunately, this is not common as the output voltage can recover very quickly.

VI. Computer Simulation and Experimental Results

Simulation and experimental results are used to demonstrate the superior performance of the proposed optimal control method for a Buck converter. Matlab was utilized to simulate a synchronous Buck converter with the following parameters: $V_{\rm in} = 5$ V, $V_o = 2.5$ V, rated load power = 25 W, $L = 1$ μH, $C = 235$ μF, ESR= 1 mΩ, RL = 2 mΩ and $fs = 400$ kHz.

The proposed algorithm was tested against a digitally-implemented current-mode PID controller. Although numerous controllers for dc–dc converters exist, a comparison was made with a current-mode controller because it is most frequently used in VRM applications and produces superior results over voltage-mode control. However, since the proposed controller allows the converter to achieve optimal dynamic performance (smallest overshoot/undershoot and shortest recovery time), other controllers cannot attain superior results.

A block diagram of the current mode PID controller is illustrated in Fig. 7. The z-domain transfer functions of the outer PID loop and the inner PI loop are expressed in (30) and (31), respectively. The PID controller was designed in the frequency-domain with a bandwidth of 70 kHz and a phase margin of 50°. In order to ensure stability of the current-mode PID controller, the sampling delay must be compensated for. The sampling delay does not affect the stability of the proposed large-signal algorithm

$$G(z) = \frac{42.26 - 49.56z^{-1} + 8.82z^{-2}}{1 - z^{-1}} \tag{30}$$

$$G(z) = \frac{0.0856 - 0.078z^{-1}}{1 - z^{-1}}. \tag{31}$$

The 9-b A/D converters allowed for a 7.8-mV voltage resolution. The voltage deviation threshold, required to activate the proposed algorithm, was set to 15.6 mV (double the least significant digit of the A/D converters). The finite resolution of the A/D converter caused minor inaccuracies in the algorithm's operation. Small "switch-over" effects can be observed from both

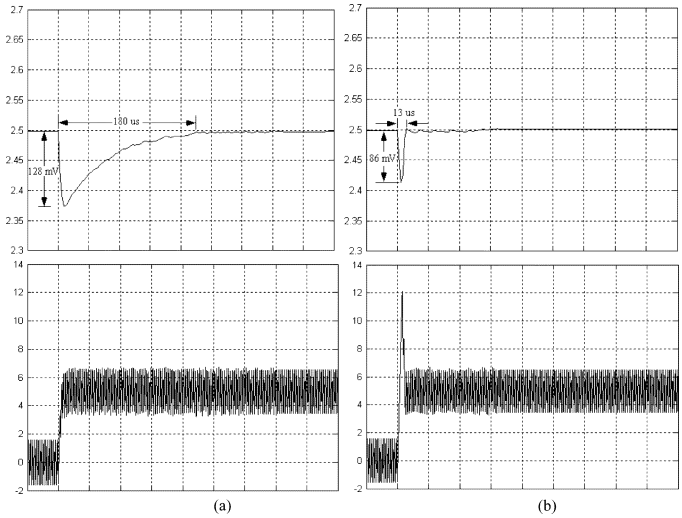

Fig. 8. Simulation result of output voltage (top) and inductor current (bottom) response to a load current step change from 0A to 5A; [X axis: 40 μs/div; Y axis: 50 mv/div (top), 2 A/div (bottom)]. (a) Current mode PID controller, output voltage (top) and inductor current (bottom) (b) The proposed optimal control algorithm (average case), output voltage (top) and inductor current (bottom).

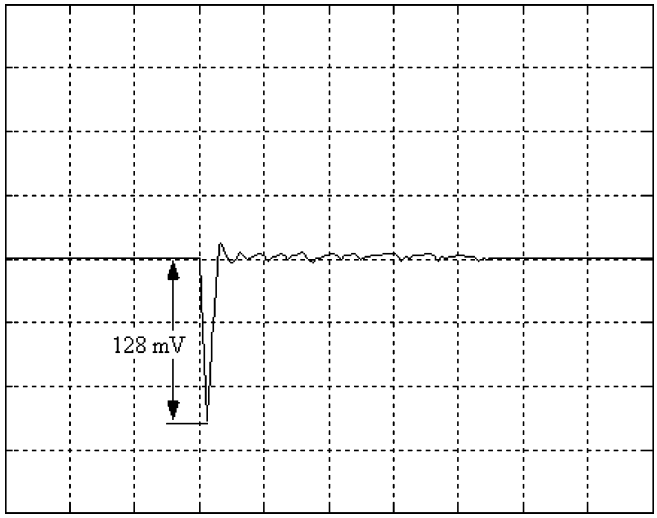

Fig. 9. Simulation result of output voltage response to a load current step change from 0 to 5 A (Output capacitance: 160 μF); X axis: 40μs/div; Y axis: 50 mv/div.

TABLE I
SIMULATION RESULTS OF THE DYNAMIC RESPONSE TO A LOAD A CURRENT CHANGE FROM 0 A TO 5 A

Control method		Δv_o (mV)	$T_{recovery}$ (us)
Optimal control algorithm	Best case	-65	14
	Average case	-86	13
	Worst case	-105	16
Current mode PID controller		-128	170

simulation and experimental results at the completion of the algorithm due to this inaccuracy.

Through simulation, three separate cases were tested: 1) Best case (the voltage deviation threshold is exceeded immediately before the voltage is sensed), worst case (the voltage deviation threshold is exceeded immediately after the voltage is sensed), and average case (the voltage deviation threshold is exceeded midway between two sensing time points). In Fig. 8, the average case response of the proposed optimal algorithm is compared with the digitally-implemented current-mode PID controller.

It can be observed from Fig. 8 that with the proposed method, during load current transient, the inductor current responds very quickly and rises above the new steady state output current to quickly charge the output capacitor. With PID controller, during load current transient, the inductor current is slightly above the new steady state value (about 0.2 A) and the recovery of the output voltage is much slower. The result is that under the same current step change, the voltage dip is reduced from 128 mv (with conventional current mode PID method) to 86 mv (with proposed method) and the recovery time is reduced from 180 μs to 13 μs. Significant improvement of dynamic performance is achieved.

Table I summarizes the simulation results of all three cases of the optimal control algorithm compared with the conventional PID controller.

It is observed from Table I that in the best case, the voltage undershoot is approximately half of the conventional current mode PID controller. For the worst case, the voltage undershoot is still 20% less than that of the PID controller. In all the cases, the recovery time is significantly reduced (90% less) from that of the current mode PID controller.

In the above simulation, the voltage undershoot under current-mode PID was 128 mV. Fig. 9 shows the simulated response of the proposed controller when the output capacitor is reduced to 160 μF (reduced from 235 μF). It is observed that the proposed controller can use a much smaller output capacitor (32% reduction) to achieve same performance as the conventional PID controller.

A prototype was constructed in order to experimentally test the proposed control method. The Buck controller parameters are identical to that of the simulation. A field programmable gate array (FPGA) was used to implement the proposed algorithm in a synchronous buck converter. Fig. 10 depicts a block diagram of the system under test.

In the experiment, an FPGA is used. The digitally-implemented PID current-mode controller requires approximately 10 K gates. For the proposed method, the gate number is approximately 160 K gates. It is noted that 12-b arithmetic is used in the FPGA design in order to prove the concept. As we only consider large signal deviation from the steady state, 8-b arithmetic will be accurate enough in practical implementation. Therefore, the number of gates can be reduced to approximately 70 K gates, 160 K $\times (8/12)^2$. In addition, the computationally-intensive arithmetic (such as division and square-root operations) can be effectively implemented using lookup tables to save more gates. After the above two methods are implemented, it is estimated that less than 50 K gates will be needed to implement the control algorithm by an FPGA. It is noted that with an application specific integrated circuit (ASIC) design, further gate number reduction can be achieved. Although the gate number for ASIC depends on experience

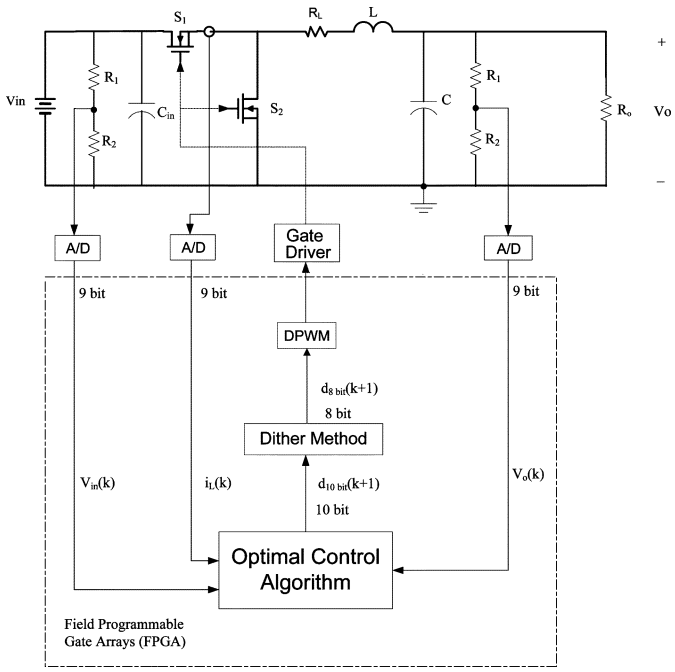

Fig. 10. Diagram of experimental Buck converter test bench using the proposed optimal control algorithms.

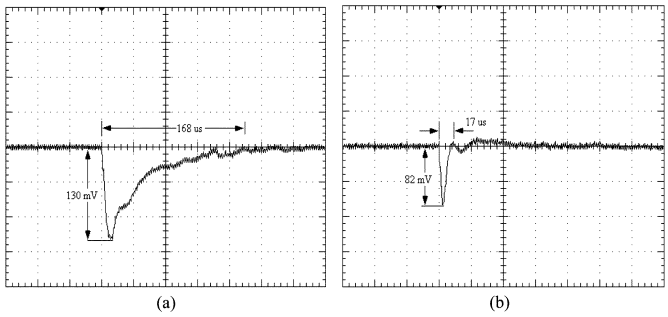

Fig. 11. Experimental result of output voltage response to load current change from 0 to 5 A (X axis: 40 μs/div; Y axis: 50 mv/div). (a) Current mode PID controller. (b) The proposed optimal control algorithm.

and process, it is estimated that the control algorithm can be implemented with 20–30 K gates in an ASIC.

It is shown in Fig. 11 that by using the proposed control algorithm, the voltage undershoot, due to a positive load current step change (0 to 5 A), is decreased from 130 mV using current mode PID to 82 mV using the proposed optimal control. The recovery time is reduced from 168 μs using the current mode PID controller to 17 us using the proposed optimal control method. The experimental results are consistent with the simulation results. It can also be observed from Fig. 11(b) that the transition from the proposed control method to the small signal control algorithm is fairly smooth, with less than a 10 mV deviation.

It is demonstrated in Fig. 12 that by using the proposed control algorithm, the voltage overshoot, due to a negative load current step change (5 A to 0 A), is decreased from 128 mV using the current mode PID controller to 58 mV using the proposed optimal control. The recovery time is reduced from 144 μs using current mode PID controller to 12 μs using the proposed optimal control method.

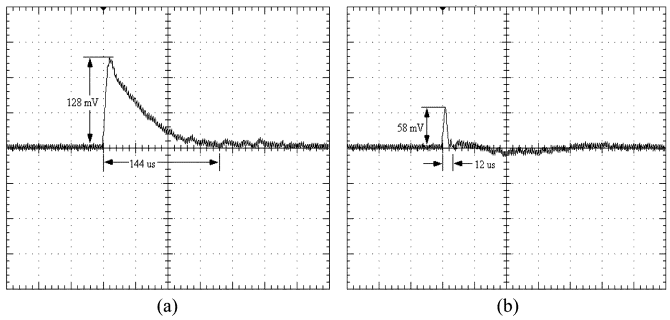

Fig. 12. Experimental result of output voltage response to load current change from 5 A to 0 A (X axis: 40 μs/div; Y axis: 50 mv/div). (a) Current mode PID controller. (b) The proposed optimal control algorithm.

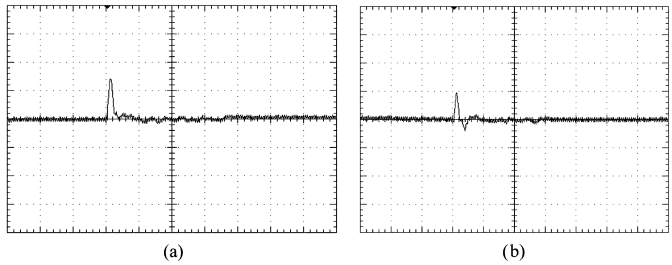

Fig. 13. Experimental result of output voltage response to load current change from 5 A to 0 A with poorly-defined output filter components (X axis: 40 μs/div; Y axis: 50 mv/div) (a) L: nominal, C: -20% and (b) L: -20%, C: nominal.

Significant dynamic performance improvement is observed from the above experimental results.

The proposed control algorithm requires the value of the output inductor and capacitor. It is common for output filter components to have large tolerances (approximately $\pm 20\%$). In order to verify the robustness of the algorithm, the filter components were varied by 20%. Fig. 13 illustrates two examples of transient responses when the output filter components are not accurately defined.

It is clear in Fig. 13, that the optimal path is no longer followed precisely. In Fig. 13(a), the algorithm allows the PID controller to regain control prematurely. In Fig. 13(b), the algorithm causes a slight voltage undershoot after the recovered overshoot. However, the dynamic response of the converter is still significantly improved and the system still demonstrates large-signal stability. Therefore, it can be concluded that poorly-defined parameters will degrade performance slightly but still allow the algorithm to function.

VII. Conclusion

In this paper, a new optimal control algorithm to improve the dynamic performance of dc-to-dc converters was proposed. Using the principle of capacitor charge balance, the minimum number of switching cycles and their respective duty cycles are predicted in order to minimize the output voltage overshoot/undershoot and to drive the output voltage back to its nominal value in the shortest possible time during load transient conditions. By utilizing the proposed algorithm, the output capacitor size can be significantly reduced while still meeting the voltage tolerance requirements. Therefore, the cost

of the converter can be reduced without sacrificing dynamic performance. Conversely, the system dynamic performance can be significantly improved without any change in components or switching frequency.

Experimental results show that the proposed optimal control algorithm produces superior dynamic performance under load current step changes. These results indicate that the proposed algorithm can be an attractive alternative to classic controllers in power converter applications where high dynamic performance is required. Furthermore, the proposed algorithm can be easily applied to other topologies such as boost and buck-boost converters.

REFERENCES

[1] S. Kanemaru, T. Hamada, T. Nabeshima, T. Sato, and T. Nakano, "Analysis and optimum design of a buck-type DC-to-DC converter employing load current feedforward," in *Proc. IEEE 35th Annu. Power Electron. Spec. Conf. (PESC'98)*, 1998, vol. 1, pp. 309–314.

[2] C. Song and J. L. Nilles, "Accuracy analysis of hysteretic current-mode voltage regulator," in *Proc. IEEE 20th Annu. Appl. Power Electron. Conf. Expo (APEC'05)*, 2005, vol. 1, pp. 276–280.

[3] B. Arbetter and D. Maksimovic, "DC-DC converter with fast transient response and high efficiency for low-voltage microprocessor loads," in *Proc. IEEE 13th Annu. Appl. Power Electron. Conf. Expo (APEC'98)*, 1998, vol. 1, pp. 156–162.

[4] R. Miftakhutdinov, "Optimal design of interleaved synchronous buck converter at high slew-rate load current transients," in *Proc. IEEE 32nd Annu. Power Electron. Spec. Conf. (PESC'01)*, 2001, vol. 3, pp. 1714–1718.

[5] J. Zhao, T. Sato, T. Nabeshima, and T. Nakano, "Steady-state and dynamic analysis of a buck converter using a hysteretic PWM control," in *Proc. IEEE 35th Power Electron. Spec. Conf. (PESC'04)*, 2004, vol. 5, pp. 3654–3658.

[6] J. Zhao, T. Sato, T. Nabeshima, and T. Nakano, "A new PWM control scheme using a triangle waveform modulated by output voltage," in *Proc. IEEE 19th Appl. Power Electron. Conf. Expo (APEC'04)*, 2004, vol. 1, pp. 399–403.

[7] B. J. Patella, A. Prodic, A. Zirger, and D. Maksimovic, "High-frequency digital PWM controller IC for DC-DC converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 438–446, Jan. 2003.

[8] Y. Duan and H. Jin, "Digital controller design for switchmode power converters," in *Proc. IEEE 14th Annu. Appl. Power Electron. Conf. Expo (APEC'99)*, 1999, vol. 2, pp. 967–973.

[9] L. Guo, J. Y. Hung, and R. M. Nelms, "PID controller modifications to improve steady-state performance of digital controllers for buck and boost converters," in *Proc. IEEE 17th Annu. Appl. Power Electron. Conf. Expo (APEC'02)*, 2002, vol. 1, pp. 381–388.

[10] B. J. Patella, A. Prodic, A. Zirger, and D. Maksimovic, "High-frequency digital PWM controller IC for DC-DC converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pt. 2, pp. 438–446, Jan. 2003.

[11] A. V. Peterchev, J. Xiao, and S. R. Sanders, "Architecture and IC implementation of a digital VRM controller," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pt. 2, pp. 356–364, Jan. 2003.

[12] M. Milanovic, M. Truntic, and P. Slibar, "FPGA implementation of digital controller for DC-DC buck converter," in *Proc. 5th Int. Workshop Syst.-on-Chip Real-Time Appl.*, Jul. 2005, pp. 439–443.

[13] A. Barrado, J. Quintero, A. Lazaro, C. Fernandez, P. Zumel, and E. Olias, "Linear-non-linear control applied in multiphase VRM," in *Proc. IEEE 36th Annu. Power Electron. Spec. (PESC'05)*, 2005, pp. 904–909.

[14] A. Soto, P. Alou, J. A. Oliver, J. A. Cobos, and J. Uceda, "Optimal control design of PWM-buck topologies to minimize output impedance," in *Proc. IEEE 17th Annu. Appl. Power Electron. Conf. Expo (APEC'02)*, 2002, pp. 426–432.

[15] A. Soto, A. de Castro, P. Alou, J. A. Cobos, J. Uceda, and A. Lofti, "Analysis of the buck converter for scaling the supply voltage of digital circuits," in *Proc. IEEE 18th Annu. Appl. Power Electron. Conf. Expo (APEC'03)*, 2003, pp. 711–717.

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