A New Resonant Gate Drive Circuit for Synchronous Buck Converter

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***Abstract*—This paper proposes a new resonant gate drive circuit for driving both the control metal oxide semiconductor field effect transistor (MOSFET) and synchronous MOSFET in a synchronous buck converter. The circuit can recover more than 70% of the conventional gate drive loss. More importantly, the driving circuit can also reduce the switching loss. It charges and discharges the gate of MOSFET at a constant current during switching interval. Other advantages of the proposed circuit include better noise immunity for dv/dt turn on, less sensitive to parasitic track inductance. The experimental prototype shows that the loss reduction is 10% of the output power for 12 V input, 1.5 V/15 A output with switching frequency of 1 MHz.**

***Index Terms*—Buck converter, current source gate driver, metal oxide semiconductor field effect transistor (MOSFET), resonant gate driver, voltage regulator (VR).**

I. Introduction

POWERING the latest microprocessor is always a challenge to the power industry. Buck converter is used almost exclusively for this application. In order to reduce size and to meet the stringent transient response requirement, the switching frequency of a Buck converter that converts 12 V bus voltage to 1.5 V and lower to power the CPU core has to be increased to beyond 1 MHz range. Another benefit of high switching frequency is lower cost as ceramic capacitor would be enough to provide enough hold up energy during load transient.

With high switching frequency operation, the switching loss and gate drive loss are both increased [1]. Fig. 1 shows the widely used conventional gate drive scheme, where Q represents the driven power MOSFET and $R_{\rm DRV}$ represents the gate resistor in the driving path. Using this conventional gate drive scheme with voltage source driven approach, when switching frequency is increased to higher than 1 MHz, significant compromise has to be made between conduction loss and frequency related loss, such as switching loss and gate drive loss. MOSFET with higher on resistor has to be used in order to reduce the switching loss and gate drive loss. In addition, the impact of the parasitic inductor caused by PCB track becomes worse. The parasitic inductance introduced by PCB track will increase the turn on and turn off time of the MOSFET, which increases the switching loss. Another possible problem with Buck converter at high switching frequency operation is dv/dt turn on for the synchronous FET.

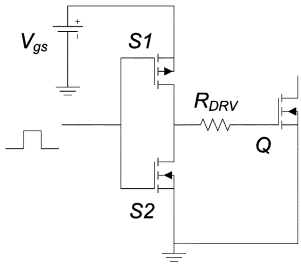

Fig. 1. Conventional gate drive scheme.

Therefore, effective gate drive scheme is needed to meet this challenge. Resonant gate drive schemes have been proposed to reduce the gate drive loss [2]–[16]. However, most of them are designed for one MOSFET. The complexity and cost is increased for driving two MOSFETs in a Buck converter [2]–[11], [13]. Some of them require transformer which further increases the complexity and cost [12], [13]. Few resonant gate driver circuits are proposed for two MOSFETs driving required by Buck converter or other topologies [14]–[16]. However, those circuits are complicated and/or have intrinsic drawbacks. For example, with the circuit proposed in [14], the MOSFET gate remains open during on and off state, which is prone to noise and causes malfunction. Other problems of the existing resonant gate drive schemes include 1) it can only recover the gate drive energy, which limits the potential for total power saving; 2) minimum Ton time is needed; and 3) it is difficult to achieve high side driver [17].

This paper presents a new resonant gate drive circuit for synchronous Buck converter that can reduce both the gate drive loss and switching loss. It uses a constant current to charge and discharge MOSFET input capacitor. Other benefits include simple circuit configuration, better dv/dt turn on immunity, less impact by parasitic inductance. Section II of the paper introduces the principle of the proposed resonant gate drive circuit. Section III of the paper summarizes the advantages of the proposed drive circuit. Section IV of the paper presents the detailed loss analysis and design procedure of the proposed circuit. Section V of the paper provides the simulation results and experimental results. Section VI is conclusions.

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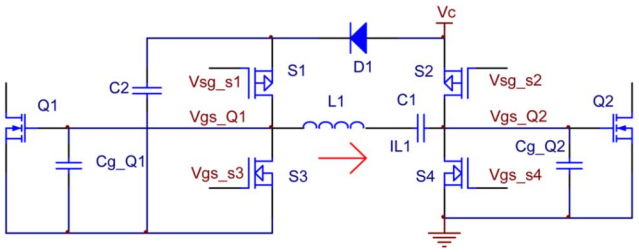

Fig. 2. Dual channel high side and low side resonant gate drive circuit.

II. Operating Principle of the Proposed Resonant Gate Drive Circuit

The proposed new resonant gate drive circuit is shown in Fig. 2. The circuit consists of four switches $S1$–$S4$, which is inherited from dual channel conventional gate drive circuit, connecting as a bridge configuration, an inductor, $L1$ and a capacitor $C1$ connecting across the bridge. Diode $D1$ and capacitor $C2$ consist of a bootstrap circuit for high side drive. Capacitors, C_{g_Q1} and C_{g_Q2}, represent the input capacitors of the power MOSFETs $Q1$ and $Q2$ respectively. $Q1$ is the high side switch and Q2 is the lower side switch. V_c is the gate drive voltage source. In order to simplify the implementation, P-channel MOSFET is used for $S1$ and $S2$ and N-channel MOSFET is used for $S3$ and $S4$. It is noted that other implementation methods can also be used to achieve the same objective.

The proposed resonant gate drive circuit shown in Fig. 2 can operate in both complementary and symmetrical mode. When it works in complementary mode, it provides two drive signals with duty cycle D and 1-D, respectively. This mode is suitable for driving two MOSFETs in a synchronous buck converter or primary MOSFETs in an asymmetrical half bridge converter. When operating in symmetrical mode, the proposed circuit provides two drive signals with same duty cycle D and with 180° out of phase. This mode is suitable for driving MOSFETs in half bridge and full bridge topologies.

The following provides the detailed operation of the proposed dual high side and low side resonant gate driver circuit operating at complementary mode. The duty cycle for $Q1$ is D and duty cycle for $Q2$ is $1 - D$. In high side and low side configuration, the current of the resonant inductor will flow through the power train of the converter in addition to the switches $S1$–$S4$. A synchronous buck converter is used for the operation principle depiction. The key waveforms are shown in Fig. 3 and a synchronous buck converter with the proposed resonant gate drive circuit is shown in Fig. 4.

In Fig. 3, $V_{sg\_S1}, V_{sg\_S2}, V_{gs\_S3}$, and V_{gs_S4} are gate drive signals for $S1$–$S4$. V_{gs_Q1} and V_{gs_Q2} are the voltage across C_{g_Q1} and C_{g_Q2}. The rising edge and falling edge of V_{gs_Q1} and V_{gs_Q2} are shown to illustrate the details of charging and discharging interval. I_{L1} is the current waveform of inductor $L1$. In the analysis, it is assumed that capacitor $C1$ is large and the voltage across $C1$ is a dc value. If the capacitor value $C1$ is small, the operation of the circuit does not change.

The operation of this circuit can be briefly described as following by six operation modes as shown in Fig. 5.

1) Before t0: $S1$ and $S4$ are off while $S2$ and $S3$ are on. $Q1$ is off and $Q2$ is on. The inductor current, I_{L1}, increases to

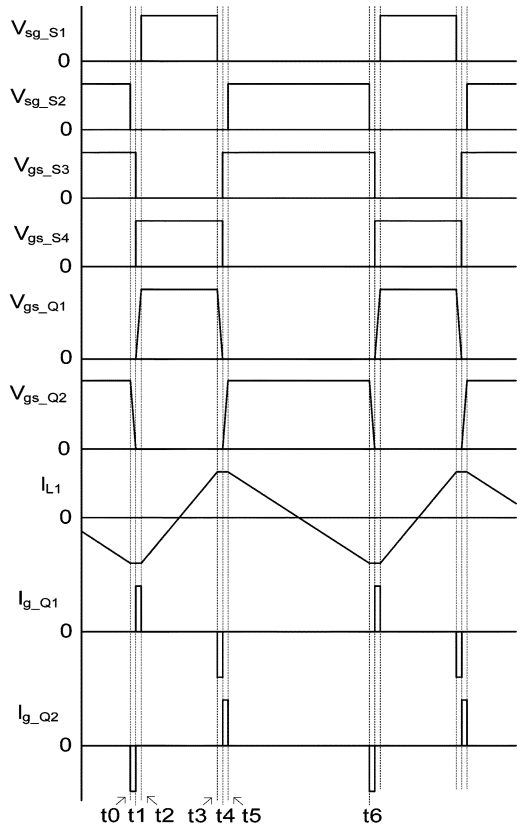

Fig. 3. Typical waveforms of dual channel high side and low side resonant gate drive circuit with complementary drive signal, $D_{Q1} = D$ and $D_{Q2} = 1 - D$.

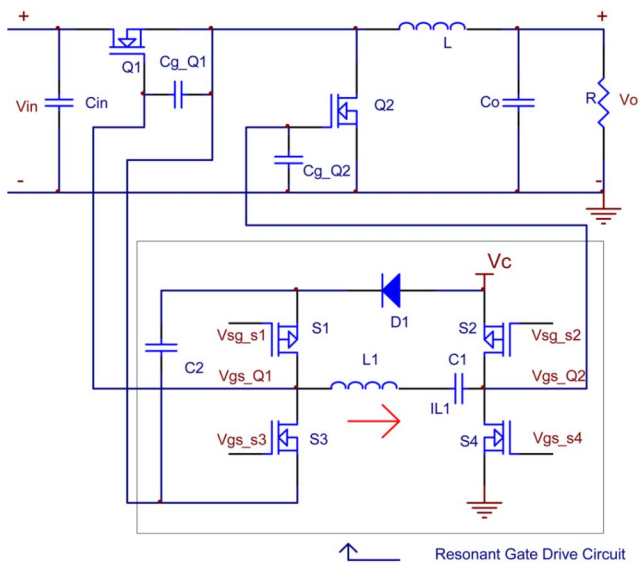

Fig. 4. Synchronous buck converter with dual high side and low side resonant gate drive circuit.

negative maximum value (Assume that current flowing from left to right side in the figure is positive). The inductor current I_{L1} flows in the loop consisted of *S2, C1, L1, S3, Q2,* and V_c. The voltage across C2 is charged to the level of V_c via $D1$ and $Q2$ as shown in Fig. 5(a).

2) From t0 to t1: $S2$ is turned off at t0. Inductor $L1$ resonates with the input capacitor of MOSFET $Q2, C_{g\_Q2}$. C_{g_Q2}

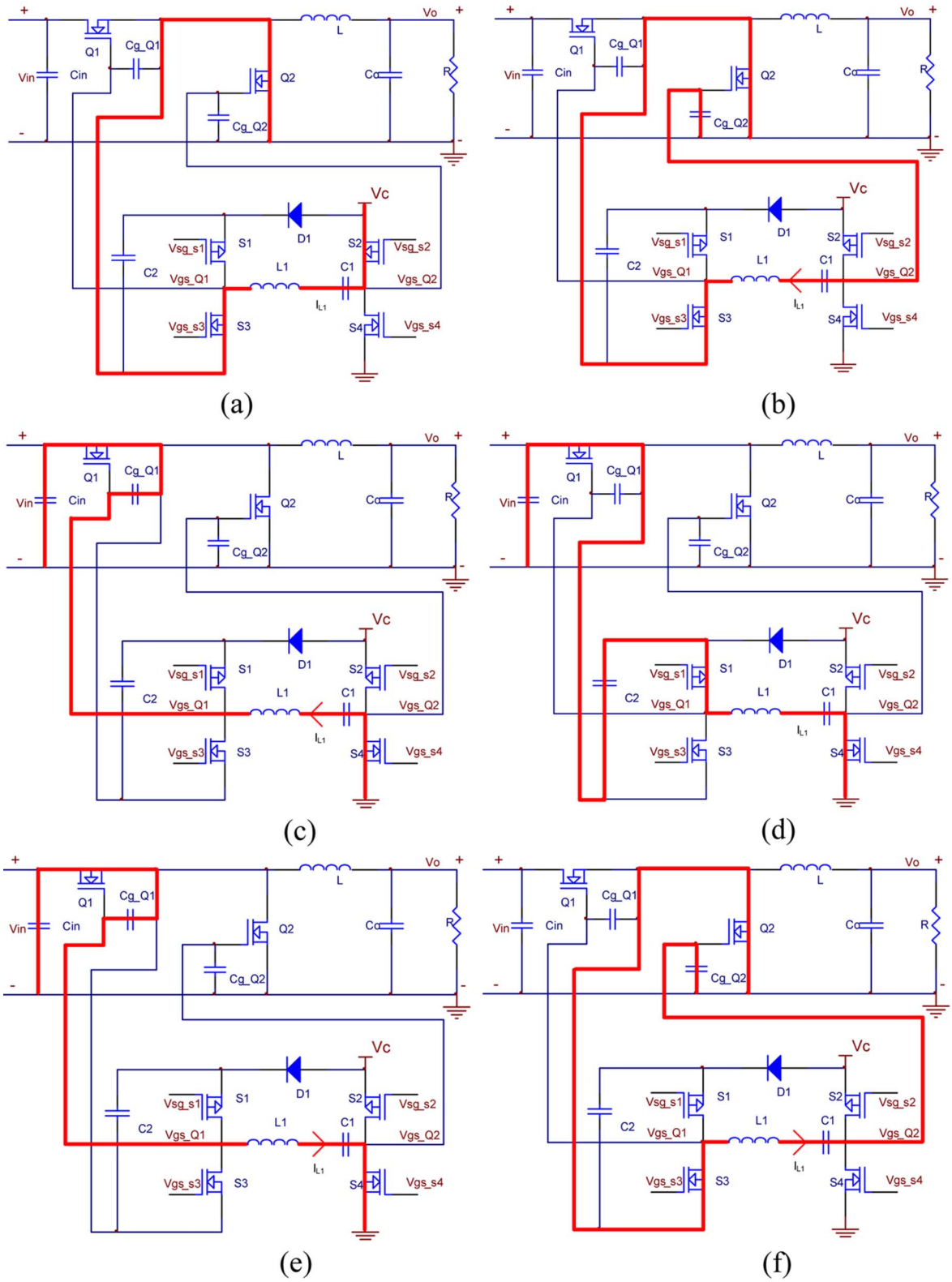

Fig. 5. Equivalent circuits of six operation modes of the proposed resonant gate drive circuit working in complementary mode. (a) Mode 1 ($t0 < t$ and $t5 < t < t6$). (b) Mode 2 ($t0 < t < t1$). (c) Mode 3 ($t1 < t < t2$). (d) Mode 4 ($t2 < t < t3$). (e) Mode 5 ($t3 < t < t4$). (f) Mode 6 ($t4 < t < t5$).

will be discharged at this period. The voltage across C_{g_Q2} decreasesand it will be clamped to zero by the body diode of $S4$ before t1. $Q2$ is turned off in this time interval. The current IL1 flows in the loop consisted of $C_{g\_Q2}, C1, L1, S3$ and $Q2$. Then at t1, $S3$ is turned off and $S4$ is turned on with zero voltage simultaneously. By controlling the turn off instant of $S2(\mathrm{t0})$, the turn off instant of $Q2$ can be controlled as shown in Fig. 5(b).

3) From t1 to t2: $S3$ is turned off and $S4$ is turned on with zero voltage at t1 simultaneously. Inductor $L1$ resonates with the input capacitor of MOSFET $Q1, C_{g\_Q1}$. C_{g_Q1} will be

charged at this period. The voltage across C_{g_Q1} increases and it will be clamped to the level of V_c by the body diode of $S1$ before t2. $Q1$ is turned on in this time interval. The current I_{L1} flows in the loop consisted of $S4, C1, L1, C_{g\_Q1}, Q1$ and V_{in} after $Q1$ is turned on. Then at t2, $S1$ is turned on with zero voltage. By controlling the turn off instant of $S3$(t1), the turn on instant of $Q1$ can be controlled as shown in Fig. 5(c).

4) From t2 to t3: $S1$ and $S4$ are on while $S2$ and $S3$ are off. $Q1$ is on and $Q2$ is off. The negative inductor current I_{L1} rises to zero and further increases. The value of the current I_{L1} will increase to positive maximum at t3. The current I_{L1} flows in the loop consisted of $C2, S1, L1, C1, S4, V_{\text{in}}$, and $Q1$. Then at t3, $S1$ is turned off with zero voltage as shown in Fig. 5(d).

5) From t3 to t4: $S1$ is turned off at t3. Inductor $L1$ resonates with capacitor C_{g_Q1}. C_{g_Q1} will be discharged at this period. The voltage across C_{g_Q1} decreases and it will be clamped to zero by the body diode of $S3$ before t4. $Q1$ is turned off in this time interval. The current I_{L1} flows in the loop consisted of $C_{g\_Q1}, L1, C1, S4, V_{\text{in}}$ and $Q1$. At t4, $S3$ is turned on and $S4$ is turned off with zero voltage simultaneously. By controlling the turn off instant of $S1$ (t3), the turn off instant of $Q1$ can be controlled as shown in Fig. 5(e).

6) From t4 to t5: $S3$ is turned on and $S4$ is turned off with zero voltage at t4 simultaneously. Inductor $L1$ resonates with capacitor C_{g_Q2}. C_{g_Q2} will be charged at this period. The voltage across C_{g_Q2} increases and it will be clamped to the source voltage V_c by the body diode of $S2$ before t5. $Q2$ is turned on in this time interval. The current I_{L1} flows in the loop consisted of *S3, L1, C1,* C_{g_Q2}, and $Q2$. At t5, $S2$ is turned on with zero voltage. By controlling the turn on instant of $S3$ (t4), the turn on instant of $Q2$ can be controlled as shown in Fig. 5(f).

7) From t5 to t6: $S1$ and $S4$ are off while $S2$ and $S3$ are on, while $Q1$ is off and $Q2$ is on. The inductor current I_{L1} decreases to zero then it will increase in opposite direction. The value of the current I_{L1} will increase to negative maximum at t6. The current I_{L1} flows in the loop consisted of $S2, C1, L1, S3, Q2$ and V_c. The next cycle will start at t6 as shown in Fig. 5(a).

In a synchronous buck converter shown in Fig. 4, the dc voltage across capacitor $C1$ is given by

$$V_{C1} = D^{*}V_{\text{in}} + (2D-1)^{*}V_C. \tag{1}$$

The peak resonant inductor current is given by

$$I_{\text{Lpeak}} = \frac{(V_{\text{in}} + 2V_C) * D * (1-D) * T_s}{2L} \tag{2}$$

where V_{in} is the input voltage of the converter. V_c is the gate drive voltage, which could be the input voltage of the converter. T_s is switching period. L is the resonant inductor value. D is the duty cycle of the control MOSFET.

The proposed dual channel high side and low side resonant gate drive circuit shown in Fig. 2 can also operate in symmetrical duty cycle mode. In this case, it provides two drive signals with the same duty cycle and 180° out of phase. A half bridge converter and a full bridge converter require this operation mode. The operation is similar to the complementary duty cycle mode and detailed description won't be provided here. The key waveforms of this operation mode are shown in Fig. 6. Fig. 7 shows a half bridge converter with dual channel high side and low side resonant gate drive circuit. In this converter, the resonant gate drive circuit works in symmetrical mode. The duty cycle of MOSFETs $Q1$ and $Q2$ are both D.

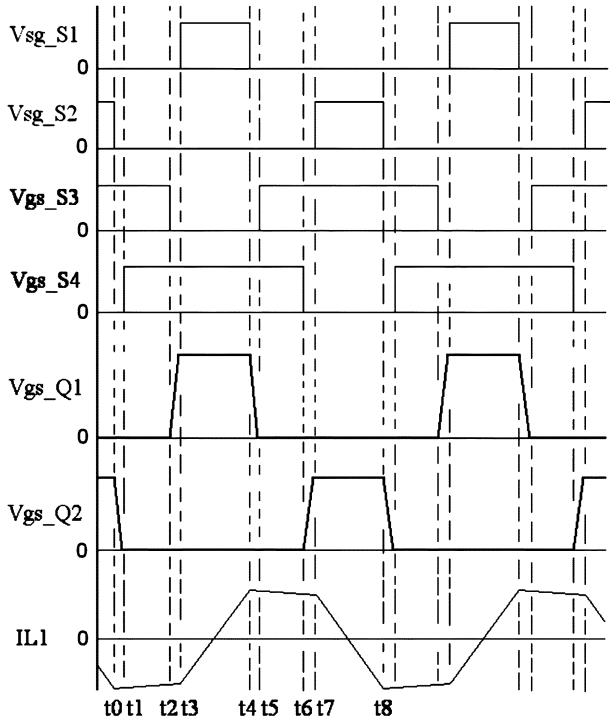

Fig. 6. Typical waveforms of dual channel high side and low side resonant gate drive with symmetrical drive signal, $D_{Q1} = D_{Q2} = D$.

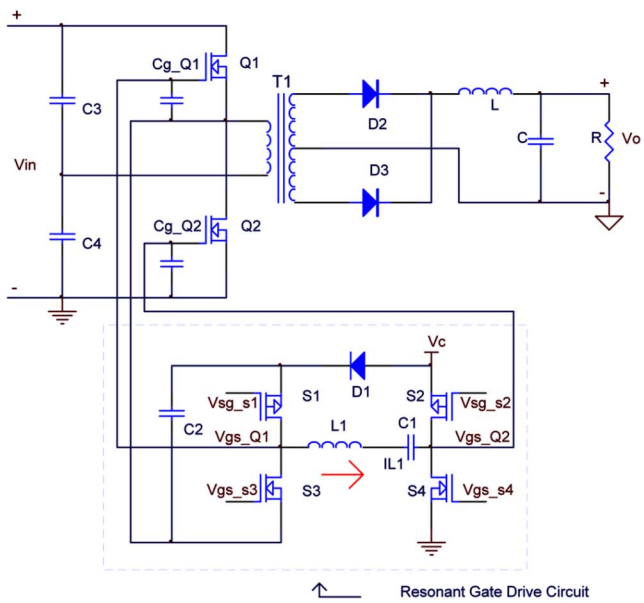

Fig. 7. Half bridge converter with dual high side and low side drive circuit.

III. Advantages

One key point for the proposed resonant gate drive circuit is that during MOSFET turn on transition, its input capacitor is

charged by the peak inductor current, $I_{\rm Lpeak}$ and the input capacitor is discharged by the peak inductor current as well during MOSFET turn off transition. During charging and discharging period, the inductor current is constant. This fact brings significant advantages to the operation of synchronous Buck converter as summarized below.

1) Smaller Gate Drive Loss: The gate charge loss can be significantly reduced. The analysis in Section IV shows that more than 70% of the gate drive loss can be recovered at 1 MHz switching frequency.

2) Reduced Switching Loss and Body Diode Conduction Loss: The charge current and discharge current is constant and is the peak value of the inductor current. This ensures quick discharge of the miller capacitor, which is critical to reduce the switching loss, especially the turn off loss when the turn off current is higher. An additional benefit from this fact is that the dead time required to avoid cross conduction between the control FET and synchronous FET can also be reduced. Thus, the diode conduction loss can be reduced.

3) High Noise Immunity and Alleviation of dv/dt Effect: With the proposed resonant gate drive circuit, as shown in Fig. 4, the gates of main MOSFETs, $Q1$ and $Q2$, are connected to either the voltage source or ground via low impedance path (S1 to S4). The $R_{\rm DS(on)}$ of $S3$ and $S4$ could be fairly small such that $|I_{\rm Lpeak}| * R_{\rm DS(on)} \ll V_{\rm th}$, the threshold voltage of the driven power MOSFETs. With the conventional gate drive scheme, the gate is connected to ground or to Vcc through external gate resistor (around 1 ohm) and driver's on-resistance (a few ohms). Therefore, the noise immunity is significantly improved and it is much less likely the synchronous FET will be turned on by dv/dt effect.

4) Less Impact of Parasitic Inductance: As the gate is charged/discharged by a constant current source, the impact caused by the parasitic inductance in the gate drive loop (such as PCB track, lead inside MOSFET) is much less. It is noted that in the conventional gate drive scheme, the parasitic inductance will reduce the charge and discharge current and therefore increase switching loss.

IV. Loss Analysis

As discussed above, the proposed resonant gate drive circuit can reduce gate drive loss. It can also reduce the switching loss (turn on and turn-off). This section compares the gate drive loss and switching loss of a Buck converter based on the proposed resonant gate drive circuit and the conventional gate drive circuit.

1) Gate Drive Loss Comparison: The current used to charge and discharge the input capacitors of the power MOSFETs is the peak inductor current $I_{\rm Lpeak}$, which is almost constant as the resonant transition is much shorter than the resonant period and the switching period T_s.

The inductor current waveform shown in Fig. 3 for one switching cycle can be divided into two pieces: $t0$–$t3$ and $t3$–$t6$. Duty cycle D equals to interval $t0$–$t3$ divided by the switching period. During interval $t0$–$t3$, the inductor current increases from negative peak current-$I_{\rm Lpeak}$ to positive peak current $I_{\rm Lpeak}$, whereas during interval $t3$–$t6$, the inductor current declines from positive peak current $I_{\rm Lpeak}$ to negative peak current-$I_{\rm Lpeak}$. Therefore, the RMS value of the inductor current $I_{\rm LRMS}$ equals to $I_{\rm Lpeak}/\sqrt{3}$.

The RMS currents flowing through the switches $S1$–$S4$ can also be derived. The inductor current flows through switches S1 and $S4$ during interval $t0$–$t3$, thus the RMS currents flowing through switches $S1$ and $S4$ are the same and given by

$$I_{\rm S1RMS} = I_{\rm S4RMS} = I_{\rm Lpeak} * \sqrt{\frac{D}{3}}. \tag{3}$$

The inductor current flows through switches $S2$ and $S3$ during interval $t3$–$t6$, thus the RMS currents flowing through switches $S2$ and $S3$ are the same and given by

$$I_{\rm S2RMS} = I_{\rm S3RMS} = I_{\rm Lpeak} * \sqrt{\frac{1-D}{3}}. \tag{4}$$

The total power loss of the proposed resonant gate drive circuit is the sum of the resistive losses and gate drive losses of switches $S1$–$S4$, the core loss and copper loss of the resonant inductor $L1$, and the resistive loss caused by the internal gate mesh resistance of the power MOSFETs (R_{G1} and R_{G2}). There is no switching loss or cross conduction loss as switches $S1$–$S4$ operate in ZVS condition.

DC resistance of the inductor winding cannot be used here to directly calculate its copper loss because of the high operation frequency. Skin-effect has to be considered. The copper loss of the inductor winding is given by

$$P_{\rm copper} = R_{\rm ac} * I_{\rm LRMS}^2 \tag{5}$$

where $R_{\rm ac}$ is the ac resistance of the inductor winding. $I_{\rm LRMS}$ is the RMS value of the inductor current. Core loss of the resonant inductor is another loss in this resonant gate drive circuit. The core loss $P_{\rm core}$ depends upon the inductor design. Core materials with high permeability such as 3F5 or PC50 should be used to reduce core loss. Air core inductor may be used when the switching frequency goes above 2 MHz. In that case, core loss is eliminated. The total inductor loss is given in

$$P_{\rm ind} = P_{\rm copper} + P_{\rm core}. \tag{6}$$

Both the charge and discharge currents flow through the internal gate mesh resistance of the power MOSFET and cause resistive loss. The charge and discharge current is the peak value of the inductor current. Thus the total losses caused by the internal resistance of two power MOSFETs during turn-on and turn-off can be given in

$$P_{\rm RG} = R_{G1} * I_{\rm Lpeak}^2 * t_{\rm sw1} * f_s + R_{G2} * I_{\rm Lpeak}^2 * t_{\rm sw2} * f_s \tag{7}$$

where $t_{\rm sw1}$ equals to the turn-on time $t1$–$t2$ plus turn-off time $t3$–$t4$ of MOSFET $Q1$, and $t_{\rm sw2}$ equals to the turn-on time $t4$–$t5$ plus turn-off time $t0$–$t1$ of MOSFET $Q2$ as shown in Fig. 3. R_{G1} and R_{G2} are the internal gate resistors of $Q1$ and $Q2$, respectively. f_s is the switching frequency. $P_{\rm RG}$ includes both the charging loss and discharging loss caused by the internal resistance of two power MOSFETs.

The RMS current flowing through switches $S1$ and $S4$ is given by (3). Assume the on-state resistors of switches $S1$–$S4$

are the same and equals to $R_{\mathrm{DS(on)}}$. Therefore the resistive loss caused by the on-state resistors of $S1$ and $S4$ can be given by

$$P_{S1} = P_{S4} = R_{\mathrm{DS(on)}} * I^2_{\mathrm{S1RMS}} = R_{\mathrm{DS(on)}} * I^2_{\mathrm{Lpeak}} * \frac{D}{3}. \quad (8)$$

The RMS current flowing through bottom switches $S2$ and $S3$ is given by (4). So the resistive loss caused by the on-state resistors of $S2$ and $S3$ can be given by

$$P_{S2} = P_{S3} = R_{\mathrm{DS(on)}} * I^2_{\mathrm{S2RMS}} = R_{\mathrm{DS(on)}} * I^2_{\mathrm{Lpeak}} * \frac{1-D}{3}. \quad (9)$$

As mentioned previously, switches $S3$ and $S4$ are N-channel MOSFET, whereas switches $S1$ and $S2$ can be either N-channel MOSFET or P-channel MOSFET. When all switches $S1$–$S4$ are same type MOSFET and their on-state resistors are the same as $R_{\mathrm{DS(on)}}$, the total conduction loss caused by the switches $S1$–$S4$ is given by (10)

$$P_{\mathrm{cond}} = P_{S1} + P_{S2} + P_{S3} + P_{S4} = 2 * R_{\mathrm{DS(on)}} * I^2_{\mathrm{Lpeak}} * \frac{1}{3}. \quad (10)$$

It is noted from above equation that the conduction loss for $S1$–$S4$ is independent of duty cycle. Although the total gate charges of switches $S1$–$S4$ are very small, they will still cause some losses at high switching frequency. The operating frequency of these four switches is the same as the switching frequency f_s of the power MOSFETs. The total gate drive loss of all four switches is given by

$$P_{\mathrm{Gate}} = 4 * Q_{g\_s} * V_{gs\_s} * f_s \quad (11)$$

where Q_{g_s} is the total gate charge of the switch, V_{gs_s} is the drive voltage of the switch, which is usually 5 V.

Therefore, the total loss of the resonant gate drive circuit can be derived by adding all above mentioned losses together and is given by

$$P_{\mathrm{DRV}} = P_{\mathrm{cond}} + P_{\mathrm{RG}} + P_{\mathrm{Gate}} + P_{\mathrm{ind}}. \quad (12)$$

On the other side, the total gate charge loss for conventional gate drive scheme can be calculated by the following equation:

$$P_{g\_\mathrm{chg}} = (Q_{g1} + Q_{g2}) * V_{gs} * f_s \quad (13)$$

where Q_{g1} and Q_{g2} are the total gate charge for $Q1$ and $Q2$, respectively. It is noted that the above equation gives only the loss related to the gate charge of MOSFET. The driver chip loss should also be considered, which will be discussed later on.

Two examples are taken to calculate the total gate drive loss for the proposed resonant gate drive circuit and for conventional gate drive circuit. One example is gate voltage of 5 V for main FET and the other example is gate voltage of 12 V for main FET. MOSFET IRF7821 from International Rectifier is selected as control MOSFET $Q1$ and FDS7088N7 from Fairchild is selected as synchronous MOSFET $Q2$. FDN335N is selected for switches $S1$–$S4$, with typical $R_{\mathrm{DS(on)}} = 0.045\ \Omega$ at 5 V gate voltage. Its gate charge at ZVS condition is $Q_{g\_s} = 3.5$ nC. The inductor peak current is designed as 1.2 A. The switching frequency is 1 MHz. DS3316P-1.0 μH is used as the inductor at 5 V and DS3316P-2.2 μH is used as the inductor at 12 V. Table I summarizes the detailed loss break down for resonant gate drive circuit and the conventional gate drive circuit.

TABLE I
LOSS COMPARISON BETWEEN RESONANT GATE DRIVER AND CONVENTIONAL GATE DRIVER

	Resonant Gate Driver (W)						Conventional Gate Driver (W)		
	Pcond	P_{RG}	Pgate	Pind	P_logic	**Ptot_rgd**	Pg_chg	P_driver	**Ptot_conv**
Vgs = 5V	0.043	0.149	0.080	0.015	0.04	**0.327**	0.31	0.15	**0.46**
Vgs = 12V	0.043	0.321	0.080	0.021	0.04	**0.506**	1.607	0.3	**1.907**

In Table I, *Pcond*, P_{RG}, *Pgate*, and *Pind* (for resonant gate drive circuit) can be calculated from (6), (7), (10), and (11). P_logic indicates the loss for logic circuit required for converting the input PWM signal to the drive signal for $S1$–$S4$. Its value is similar to the power loss of a conventional gate drive chip operating at no load. The loss is around 0.04 W. Pg_chg in Table I represents the gate charge loss, as expressed by (13). P_driver represents the driver chip loss, which is estimated at around 0.3 W for switching frequency of 1 MHz and Vgs of 12 V [1]. For 5 V operation, P_driver is estimated at around 0.15 W.

It can be observed from Table I that at $Vgs = 5$ V, the resonant gate drive circuit can reduce the total gate drive loss from 0.46 W to 0.327 W, a reduction of 0.133 W, or 29%. At $Vgs =$ 12 V, the resonant gate drive circuit can reduce the total gate loss from 1.907 W to 0.506 W, a reduction of 1.401 W, or 73%.

It should be noted that for conventional gate drive circuit, the gate drive loss at Vgs of 12 V is very high and the driver chip will have a high temperature rise. Therefore, Vgs of 12 V is not used for 1 MHz switching frequency operation. Vgs of 5 V is normally used. The consequence of 5 V Vgs is higher conduction loss for the MOSFET. Design compromise has to be made between higher gate drive loss and lower conduction loss.

With the proposed resonant gate drive circuit, the total gate drive loss at Vgs of 12 V is 0.506 W, marginally increased from 0.327 W at $Vgs = 5$ V and almost the same as the gate loss for conventional gate driver at 5 V gate voltage. Therefore, the design compromise between higher gate loss and lower switching loss and conduction loss is not needed. In the simulation and experimental prototype, Vgs of 12 V is used for resonant gate drive circuit. For conventional gate drive circuit, Vgs of 6 V and 12 V are both used.

2) Switching Loss Analysis: Turnoff behavior of the driven MOSFETs under the proposed resonant gate drive circuit is much different from that of conventional voltage gate drive scheme. Switching loss can be reduced by reducing switching time. Therefore, significant switching loss reduction can be achieved.

Normally, $V_{\mathrm{gs(th)}}$ of a power MOSFET is around 2 V, and the plateau voltage V_p is around 3 V. Under conventional gate drive scheme, assume gate drive voltage V_{gs} is 5 V and the total gate resistance (including the gate resistor inside the MOSFET, which is around 1–2 Ω, the on resistor of the driver, which is around 1 to 2 Ω, as well as external gate resistor to damp the

TABLE II
PARAMETERS FOR SIMULATING DUAL HIGH SIDE AND LOW SIDE RESONANT GATE DRIVE CIRCUIT

Part Number	Part Type	Part Number	Part Type
Q1	IRF6623	L1	2.2uH
Q2	IRF6618	C1	1uF
S1-S4	FDN335N	C2	2.2uF

gate capacitor, which is usually around 1 Ω) is around 3–5 Ω. Then the average charge current in turn-on transition (charging the miller plateau) is $(5\ \text{V} - 3\ \text{V})/3\ \Omega = 0.7$ A, whereas the average discharge current in turn-off transition is determined by the threshold voltage and plateau voltage and is only 3 V/3 Ω = 1 A [1]. It is also noted that because of the parasitic inductance introduced by PCB track and wire inside the MOSFET, the actual charge current and discharge current is much smaller and the switching loss is much larger [18], [19].

With the resonant gate drive circuit, the charge current at turn on and discharge current at turn off are constant and equal to the peak inductor current. Therefore, the switching time is reduced significantly and the switching loss is also reduced significantly, as shown in the simulation and experimental results.

An additional benefit for synchronous Buck converter with the proposed resonant gate drive circuit is that the dead time between the control FET and SR FET can be reduced and therefore, the body diode conduction loss can be reduced.

V. COMPUTER SIMULATION AND EXPERIMENTAL RESULTS

Both the conventional gate drive scheme and the proposed resonant gate drive scheme are simulated by using Pspice. A totem pole drive topology is used to represent the conventional voltage drive scheme. A resistor is used to limit the drive current so that the peak current in turn on transition is 2 A. An experimental prototype is also built to verify the feasibility and advantages of the proposed resonant gate drive circuit. As a comparison, a Buck converter with conventional gate drive circuit is also built.

In order to determine the parameters in the resonant gate drive circuit, the peak inductor current needs to be decided first. A 2 A peak drive current is chosen for the conventional gate drive scheme, for the same switching time, only half of the peak inductor current is needed by using the proposed resonant drive scheme. Once the drive current and duty cycle of the drive signal is determined, the resonant inductor value can be calculated by using (2). The parameters in both the simulation and experiment are chosen in this way.

1) Simulation Results: The simulation circuit is shown in Fig. 4. The key parameters used for the simulation are listed in Table II. The switching frequency is 1 MHz and duty cycle of $Q1$ is 0.12. Both the input voltage V_{in} and the drive voltage V_c is 12 V. The drive signals of $S1$–$S4$ come from four pulse voltage sources in the simulation software. The output current is 20 A and the peak to peak output current ripple is 20 A as well.

The simulation waveforms are shown from Figs. 8 –13. Fig. 8 shows the gate source voltage and charge/discharge currents of MOSFET $Q1$. The drive voltage is 12 V, which equals to the input voltage. The charge current and discharge current are both

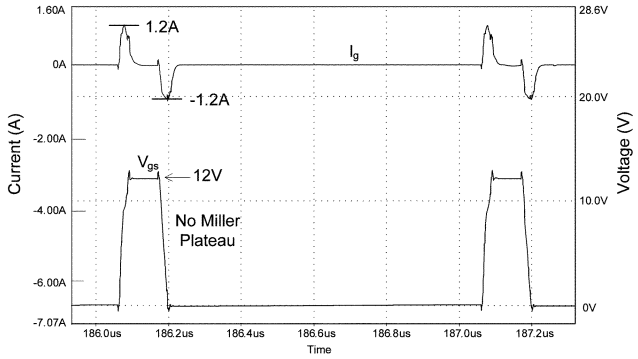

Fig. 8. Gate-source voltage and charge/discharge currents of MOSFET $Q1$ in a synchronous buck converter with resonant gate drive circuit.

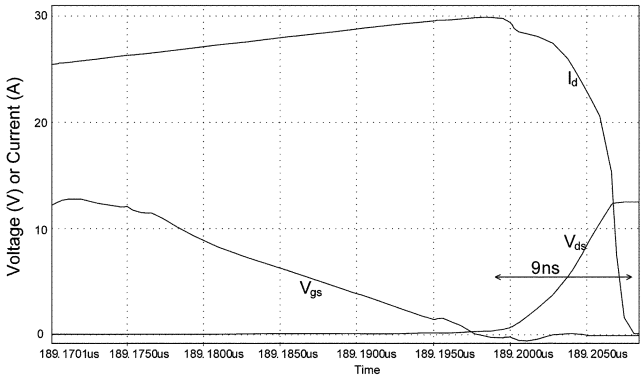

Fig. 9. Drain-source voltage and drain current of MOSFET $Q1$ in turn-off transition with resonant gate drive circuit.

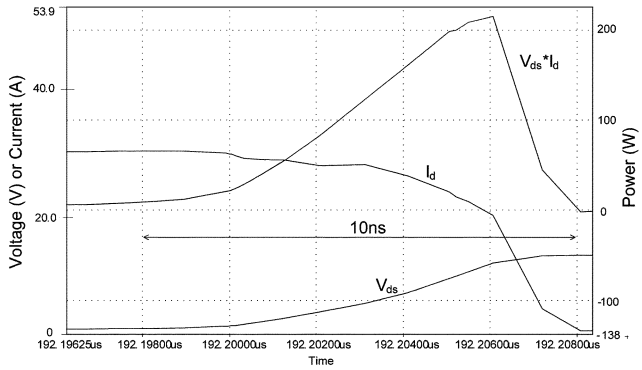

Fig. 10. Turn-off switching loss of MOSFET $Q1$ in a synchronous buck converter with resonant gate drive circuit.

1.2 A, which is also the peak inductor current. It is also noted that there is no miller plateau in V_{gs} waveform.

Fig. 9 shows the drain-source voltage and drain current of control MOSFET $Q1$ in turn-off transition with resonant gate drive circuit, the gate-source voltage is included as well. It is observed that the turn-off switching time (rising of V_{ds} and falling of I_d) is only 9 ns.

Fig. 10 shows the instant turn-off switching loss of MOSFET $Q1$. Referring to curve of $V_{ds} * I_d$, the average turn-off switching loss can be estimated as $0.5 * 10\ \text{ns} * 215\ \text{W} * 1\ \text{MHz} = 1.075$ W.

A synchronous buck converter with conventional gate driver is also simulated. The source-sink current capacity of the driver

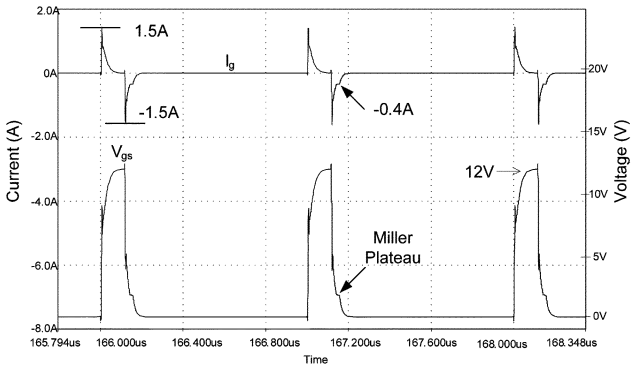

Fig. 11. Gate-source voltage and charge/discharge currents of MOSFET $Q1$ in a synchronous buck converter with conventional gate drive scheme.

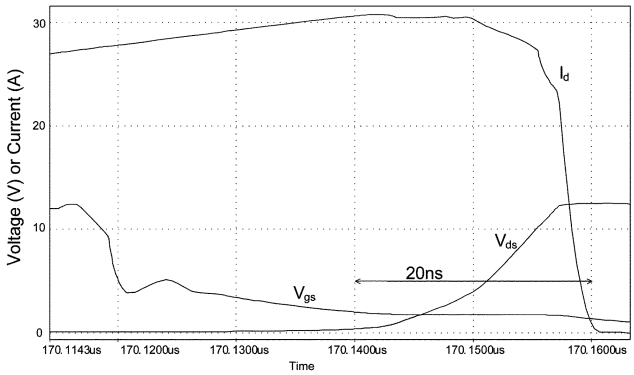

Fig. 12. Drain-source voltage and drain current of MOSFET $Q1$ in turn-off transition with conventional gate drive scheme.

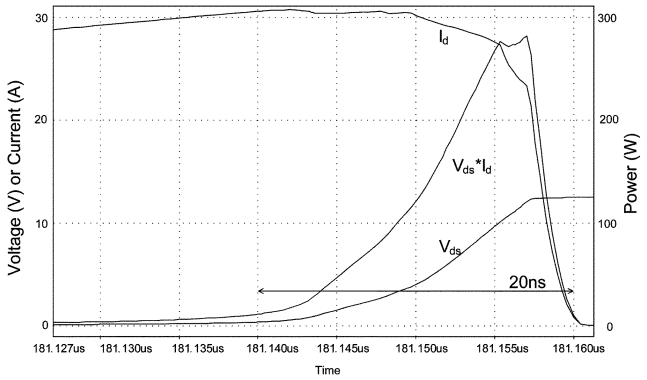

Fig. 13. Turn-off switching loss of MOSFET $Q1$ in synchronous buck converter with conventional gate drive scheme.

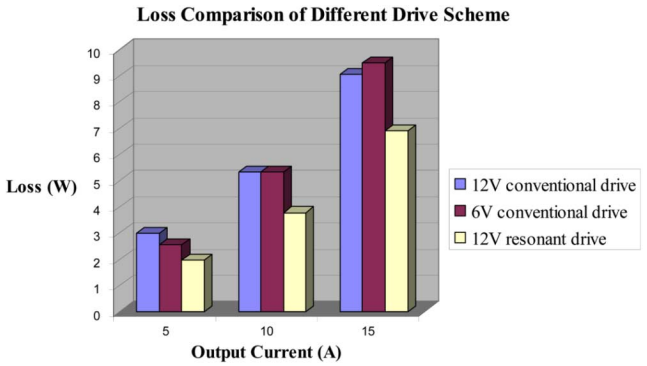

Fig. 14. Loss comparison of conventional drive scheme and resonant drive scheme.

is 2 A. The parameters for Buck converter and the switching frequency are the same in two drive schemes.

Fig. 11 shows the gate-source voltage and charge/discharge currents under conventional gate drive scheme. The peak charge/discharge currents are 1.5 A. The internal mesh resistor of the MOSFETs limits the source-sink current of the driver less than 2 A. It is also observed that discharge current at Miller plateau is only about 0.4 A and Miller plateau in V_{gs} is clearly observed.

Fig. 12 shows the drain-source voltage and drain current. The gate-source voltage is included as well. It is observed that the turn off switching time (rising of V_{ds} and falling of I_d) is 20 ns, which is two times of the turn off time for the case of resonant gate drive circuit.

Fig. 13 shows the instant turn-off switching loss of MOSFET $Q1$. Referring to curve of $V_{ds}*I_d$, the average turn-off switching loss can be calculated as $0.5 * 20$ ns $* 280$ W $* 1$ MHz $=$ 2.80 W. It is noted that the peak switching loss of 280 W is higher than that in the case of resonant gate drive circuit.

Comparing with the turn-off switching loss under resonant gate drive circuit, the loss saving is: $2.80 - 1.075 = 1.725$ W. In other words, the percentage of the turn loss saving is $1.725/2.8 = 61.6\%$.

2) Experimental Results: Two Buck converters are built. One with resonant gate drive circuit and the other with the conventional gate drive circuit. The Buck converter parameters are the same. The input voltage of the prototype is 12 V. The output is 1.5 V/15 A. The switching frequency is 1 MHz. For Buck converter, the control FET is IRF7821 and the synchronous FET is FDS7088N7. The Buck inductor value is selected as 0.5 μH with ripple current of 2.6 A peak to peak.

For resonant gate drive circuit, FDN335N is selected for switches $S1$–$S4$. The inductor is DS3316P-2.2 uH from Coilcraft. The peak inductor current is 1.2 A.

For conventional gate drive scheme, the driver chip is TPS2832 from Texas Instrument [19]–[21], which uses adaptive dead-time control circuit to eliminate shoot-through currents through the control FET and SR FET during switching transition. The external gate resistor is 1 Ω. It is noted that when the external gate resistor is set to zero. The measurement result does not change.

For resonant gate drive circuit, the gate-source voltage is 12 V. For conventional gate drive circuit, gate voltage of 12 V and 6 V are both used. It is noted that with Vgs of 12 V, the driver chip is very hot and it can not operate continuously for more than 10 min.

The total power loss for two converters under different load current is measured and summarized in Fig. 14.

It is observed from the measurement that significant power loss reduction is achieved. It is also observed from the above figure that at 1.5 V/15 A output, the power loss reduction is 2.15 W at 15 A output current. It is almost 10% of the output power (22.5 W).

A more detailed look at the measurement data shows that when the load current increases, the total power loss reduction

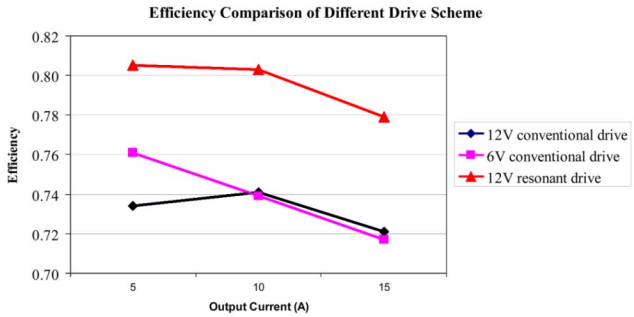

Fig. 15. Efficiency comparison of conventional drive scheme and resonant drive scheme.

achieved by the resonant gate drive circuit is also increased. At 5 A load current, the total loss reduction is 1.03 W and at 15 A, the total loss reduction is increased to 2.15 W. As the gate drive loss is independent of load current and the conduction loss is same for both gate drive schemes, the result shows that the switching loss is reduced by the resonant gate drive scheme. The power loss reduction due to switching loss reduction is very significant.

The proposed resonant gate drive circuit also beats the conventional gate drive scheme with 6 V drive voltage. It is observed that less energy is saved under light load condition by using resonant gate drive circuit as the driving loss under 6 V conventional drive scheme is reduced dramatically. Whereas under heavy load condition, more energy is saved by using resonant gate drive circuit, since the drive loss reduction benefit is overwhelmed by the conduction loss increasing.

Fig. 15 shows the efficiency comparison of the prototype under different drive scheme. It is observed that the efficiency improvement is higher than 5% under almost all condition. It is up to 7.8% under 15 A.

Fig. 16 shows the measured waveforms with resonant gate drive circuit. As shown in Fig. 16(a), the gate drive signal for $Vgs1$ (control FET) is very clean and smooth. No miller plateau is observed as the miller charge is removed very quickly. The total rise time and fall time (between 0 V and 12 V) of $Vgs1$ is less than 20 ns. This indicates that the switching time is much less than that, and therefore, very fast switching is achieved. The ringing in $Vgs2$ is caused by noise picked up by the probe. Fig. 16(b) shows the drain to source voltage of synchronous rectifier. Fig. 16(c) shows the resonant inductor current waveform. The peak inductor current, which is also the charge and discharge current, is about 1.2 A.

The simulation results and experimental results presented in this section demonstrate that the proposed resonant gate drive circuit can significantly reduce the power loss, especially the switching loss, and, therefore, improve the efficiency. With resonant gate drive circuit, the loss saving of 2.15 W is achieved for 22.5 W (1.5 V/15 A) output, or almost 10%.

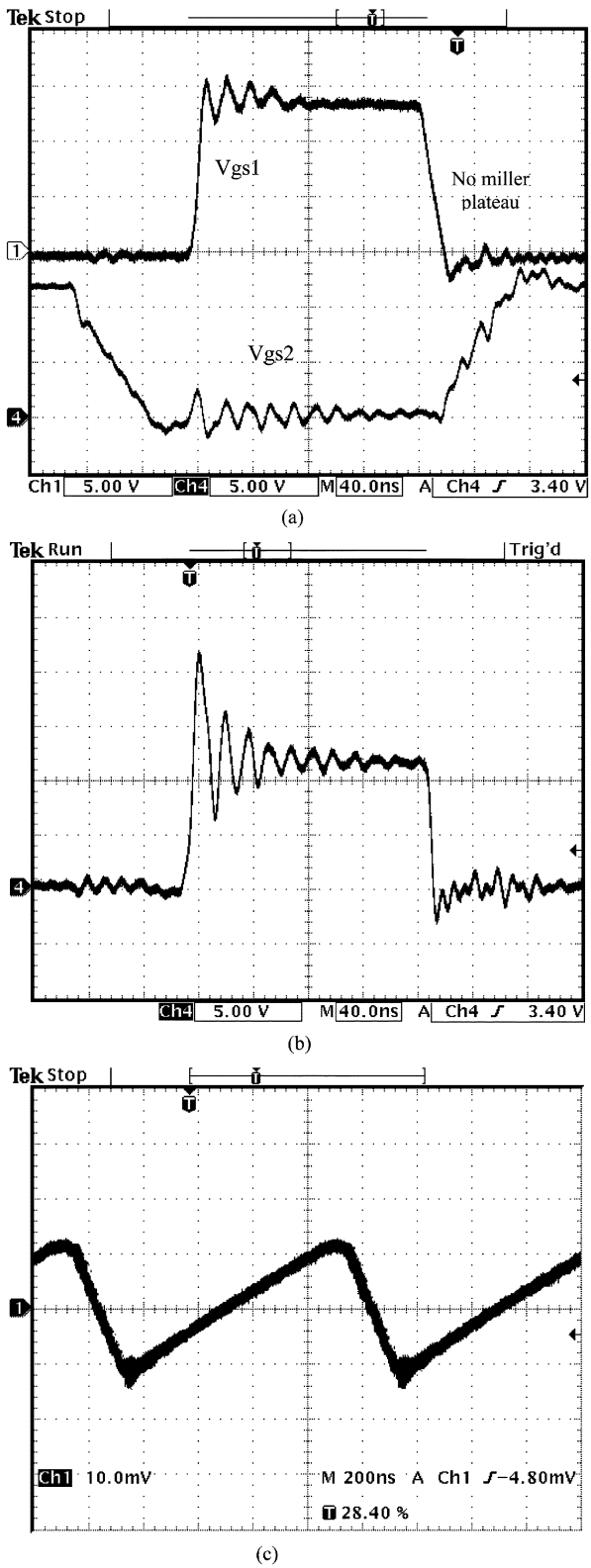

Fig. 16. Measured key waveforms of the proposed resonant gate drive circuit. (a) Top trace: $Vgs1$ (control FET). Bottom trace: $Vgs2$ (SR FET), scale: 5 V/div, 40 ns/div. (b) Drain to source voltage for SR FET scale: 5 V/div, 40 ns/div. (c) Resonant inductor current 1 A/div (10 mV/div), 200 ns/div.

VI. Conclusion

A new resonant gate drive circuit suitable for synchronous Buck converter is proposed in this paper. The gate drive loss can be reduced. More importantly, the switching loss can also be reduced significantly. Therefore, the overall power loss can be reduced significantly. The gate drive loss and switching loss is analyzed in detail and compared with the conventional gate

drive scheme. Computer simulation is performed and experimental prototype is built to verify the operation of the new resonant gate drive circuit. The measurement result shows that the power loss can be reduced by almost 10% of the output power for 12 V input and 1.5 V/15 A output Buck converter operating at switching frequency of 1 MHz.

The proposed resonant gate drive circuit provides a new and a very promising way to improve the performance for VRM application. Although an additional inductor is needed to implement the resonant gate drive circuit, this cost penalty can be offset by the following factors: At high switching frequency operation, ceramic capacitors will be able to provide adequate dynamic response and more expensive Oscon capacitor is no longer needed, which will reduce board area and cost. In addition, Buck inductor value can also be reduced, which also reduce board area and cost.

If the switching frequency remains same as present application, such as around 300 KHz, the reduction of switching loss will improve the efficiency and thermal performance. Therefore, each phase can deliver more load current or the number of phases can be reduced to deliver same amount of load current.

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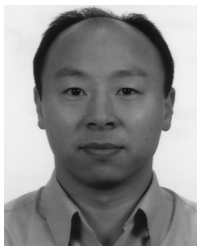

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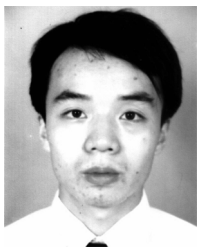

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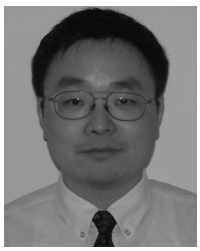

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