A Practical Minimum Time Control Method for Buck Converters Based on Capacitor Charge Balance

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Abstract – A control method is presented in this paper which utilizes the concept of capacitor charge balance to achieve optimal dynamic response for Buck converters undergoing a rapid load change. The proposed charge balance method is implemented with analog components and is cheaper and more effective than its digital counterparts since complex arithmetic and sampling delay is eliminated. The proposed controller will consistently cause the Buck converter to recover from an arbitrary load transient with the smallest possible voltage deviation in the shortest possible settling time. Since the controller is non-linear during transient conditions, it is not limited by bandwidth/switching frequency. Unlike conventional linear controllers, the dynamic response (voltage deviation, settling time) of the proposed controller can be accurately predicted using a set of equations. This greatly simplifies the design process of the output filter. Simulation and experimental results show the functionality of the controller and demonstrate the superior dynamic response over that of a conventional linear controller.

I. INTRODUCTION

Traditionally, linear analog controllers (such as voltage-mode and current-mode schemes) have been utilized to control Buck converters. These controllers offer benefits such as zero steady-state error and predictable switching frequency. However, the dynamic response of linear controllers is limited by their bandwidth. Therefore, numerous alternative controllers have been proposed to overcome bandwidth limitations.

An ideal Buck controller would behave linearly during steady-state conditions for tight voltage regulation and behave non-linearly during transient conditions for fast response. It is demonstrated in [1]-[5] that by employing two separate controllers for steady-state operation and for transient operation, the dynamic response can be significantly improved while not sacrificing steady-state accuracy. In [1], two linear controllers are utilized: a compensator with high DC gain and lower bandwidth for steady-state conditions and a high bandwidth compensator for transient conditions. While this method improves dynamic performance, the controller still suffers from traditional bandwidth limitations. In [2]-[4], control methods are presented which utilize a linear control scheme during steady-state conditions and saturate the duty cycle to either 0% or 100% when a load transient occurs. While these methods effectively reduce voltage deviation caused by load transients, imprecise timing of the saturation period leads to sub-optimal settling times in most cases. In [5], a combined linear/non-linear control method is provided which saturates the duty cycle for a precise period to minimize the settling time of output voltage transients due to varying reference voltages. While this method is effective, little investigation was conducted regarding the controller's response to load transients.

It has been presented in [6]-[7], that to an arbitrary external disturbance, there exists an "optimal response" for a Buck converter. The optimal response is such that the settling time and voltage deviation would be reduced to its minimum possible value. While the response and theory is studied in these papers, no practical implementation of a controller is described.

In [8], a method is presented to design a linear controller that attempts to mimic the optimal response. While this controller can produce near-optimal results, it is impossible for a linear controller to accurately achieve the desired optimal response since the response is, in fact, non-linear. In [9], a digital controller is presented which attempts to achieve optimal response through fuzzy-logic approximation. Although the non-linear fuzzy-logic approach is better suited than the linear approximation, the response is still sub-optimal. In [10], a near-optimal response is achieved by using a digital output capacitor estimator and a simple linear switching surface. However, in order to achieve a true optimal response, a non-linear switching surface is required.

In [11], an analog second-order switching surface controller is designed to achieve the optimal response to an external disturbance. However, an analog multiplier is utilized in the control scheme which is expensive and significantly limits the speed of the controller. In order to utilize the controller, the switching speed of the converter was set to 20kHz.

In [12], equations to determine the optimal response to a disturbance are presented. The optimal response, to a large range of disturbances, is calculated using MATLAB offline and programmed into a digital controller. The controller successfully achieves a minimal, predictable settling time to an external disturbance. Unfortunately, the controller is only functional in open-loop configuration. The time instant when the disturbance occurs and the magnitude of the load variation must be defined in advance, which is an impossible situation for most Buck converter applications.

In [13], a digital controller is presented which can calculate the optimal response to an arbitrary load variation "on-the-fly". The digital controller significantly improves the dynamic response of a converter undergoing a fast load transition. However, the controller performs multiplication, division and square-root operations resulting in costly implementation. Furthermore, it is determined that the response of [13] could further be improved if the sampling delay were eliminated.

In this paper, a combined linear/non-linear controller is presented which is able to achieve the optimal response of a Buck converter for a large-signal load variation. The controller is practical as it requires only simple analog functions (comparison and integration). As some recent VRM drivers operate in discontinuous current mode (DCM) in order to boost light-load efficiency, the controller is capable of operation in continuous current mode (CCM) and DCM. The controller ensures that the converter will respond to an arbitrary load current variation with the minimum possible voltage deviation and shortest possible settling time. In addition, since the response to a load current change is predictable under the proposed controller, the design procedure of the converter is greatly simplified.

II. CONTROLLER CONCEPT

The "optimal response" to a load current variation occurs when the output voltage deviation and the settling time is minimized to their smallest possible values.

A. Minimize Voltage Deviation

Referring to Fig. 1, immediately following a positive load current step, the inductor current cannot change instantaneously to supply the load. Therefore, a portion of the load current must be supplied by the output capacitor. This, in turn, causes the output capacitor to lose charge and causes the output voltage to decrease. The output capacitor will finish discharging when the inductor current reaches the new load current (at t_1). In order to minimize the output voltage undershoot, the inductor current must be allowed to vary at its maximum slew rate ($d = 100\%$) for T_0.

Referring to Fig. 2, following a negative load current step, the capacitor must absorb the excess inductor current until it equals the new load current (at t_1). This causes the capacitor to charge and causes the output voltage to increase. In order to minimize the output voltage overshoot, the inductor current must be allowed to vary at its maximum slew rate ($d = 0\%$) for T_0.

B. Minimize Settling Time

Referring to Fig. 1, the output capacitor will start to recharge and the output voltage increase when the inductor current begins to exceed the new load current. In order to minimize the time required to recharge the capacitor, the duty cycle will remain at 100% for T_1. At t_2, the duty cycle will be set to 0% causing the inductor current to decrease at its maximum slew rate. t_2 should be such that at the instant that the inductor current returns to the new load current (at t_3), $A_{discharge}$ equals A_{charge}. At t_3, the output voltage and the inductor current are at their steady-state values and the converter will have fully recovered from the positive load step.

Referring to Fig. 2, for a negative load step, the duty cycle will remain at 0% for T_1 in order to minimize the time required to remove the necessary charge from the capacitor. At t_2, the duty cycle will be set to 100% causing the inductor current to increase at its maximum slew rate. As above, t_2

should be such that at the instant that the inductor current returns to the new load current (at t_3), $A_{discharge}$ equals A_{charge}.

In summary, the two key points of the proposed control method are:
1. Immediately detect the load current step change and react by setting the duty cycle to its maximum value (for a positive step change) or to its minimum value (for a negative step change).
2. Set the duty cycle to its minimum value (for a positive load step) or its maximum value (for a negative load step) at t_2. t_2 should be such that A_{charge} will equal $A_{discharge}$ at time t_3. This will cause the output voltage to equal the reference voltage at the exact moment that the inductor current equals the load current.
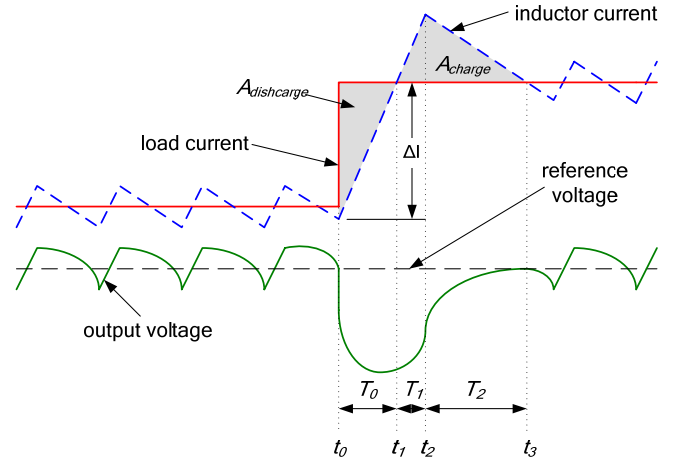

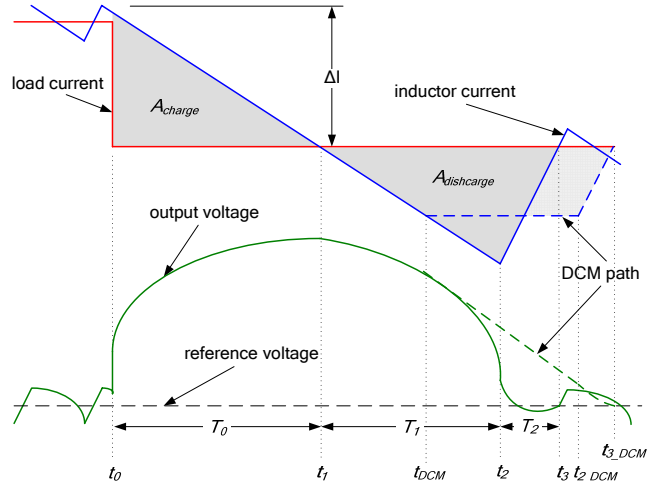Fig. 1   Proposed controller response to a positive load current step

Fig. 2   Proposed controller response to a negative load current step

III. MATHEMATICAL ANALYSIS OF THE PROPOSED CONTROLLER RESPONSE

Fig. 3 illustrates the charge and discharge areas for a positive load current step change.

Time period T_0:

It is apparent in Fig. 3, that the total discharge area A_1 is equal to A_{1a}, thus (1) is true.

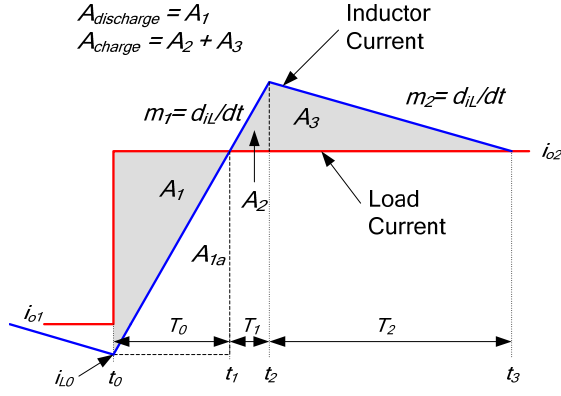Fig. 3   Proposed inductor current response to a positive load step

$$A_1 = \int_{t0}^{t1} [i_{o2} - i_L(t)]dt = A_{1a} = \int_{t0}^{t1} [i_L(t) - i_{L0}]dt \qquad (1)$$

where m_1 represents the rate at which $i_L(t) - i_{L0}$ is increasing, such that (2) and (3) are true.

$$m_1 = \frac{d[i_L(t) - i_{L0}]}{dt} \qquad (2)$$

$$i_L(t) - i_{L0} = \int_{t0}^{t} m_1 dt \qquad (3)$$

Therefore, by combining (1) and (3), the total discharge area $A_{discharge}$ can be expressed in (4).

$$A_{discharge} = A_1 = A_{1a} = \iint_{T0} m_1 (dt)^2 \qquad (4)$$

Time period T_1:

Through similar steps as (1) through (4), A_2 can be calculated as shown in (5).

$$A_2 = \iint_{T1} m_1 (dt)^2 \qquad (5)$$

Using basic geometry, a relationship for A_2 and A_3 is found in (6), in terms of the rising (m_1) and falling (m_2) slew rates of the inductor current.

$$\frac{A_3}{A_2} = \frac{m_1}{-m_2} \qquad (6)$$

Thus, by combining (5) and (6), an expression for the total charge area A_{charge} is presented in (7).

$$A_{charge} = A_2 + A_3 = \iint_{T1} m_1 (dt)^2 + \iint_{T1} \frac{m_1^2}{-m_2} (dt)^2$$
$$= \iint_{T1} \frac{m_1 m_2 - m_1^2}{m_2} (dt)^2 \qquad (7)$$

By using (7), it is possible to predict the total charge area at time t_2. In order to satisfy the principle of capacitor charge balance at t_3, (8) must be true.

$$A_{discharge} - A_{charge} = 0$$

$$\iint_{T0} m_1 (dt)^2 - \iint_{T1} \frac{m_1 m_2 - m_1^2}{m_2} (dt)^2 = 0 \qquad (8)$$

$$\iint_{T0} (dt)^2 - \frac{m_2 - m_1}{m_2} \iint_{T1} (dt)^2 = 0$$

The inductor current slew rates of a Buck converter are known ($m_1 = (V_{in}-V_o)/L$; $m_2 = -V_o/L$) and are substituted into (8) to yield (9).

$$\iint_{T0} (dt)^2 - \frac{\frac{-V_o}{L} - \frac{(V_{in}-V_o)}{L}}{\frac{-V_o}{L}} \iint_{T1} (dt)^2 = 0 \qquad (9)$$

$$V_o \iint_{T0} (dt)^2 - V_{in} \iint_{T1} (dt)^2 = 0$$

Using equation (9), it is possible to use an analog double integrator, to calculate the time t_2 that will allow $A_{charge} - A_{discharge}$ to equal zero when the inductor current reaches the new load current (at t_3). The aforementioned concept is illustrated in Fig. 5a).

In the case of a positive load current step, the duty cycle would be set to 0% when V_2 equals zero (at time t_2). This will allow the inductor current to fall and reach the output current at the exact moment that the charge previously removed from the capacitor equals the charge delivered to the capacitor.

A similar analysis is performed for a negative current step change for a continuous current mode (CCM) converter. The result of the analysis is expressed in (10).

$$A_{charge} - A_{discharge} = 0$$

$$(V_{in} - V_o) \iint_{T0} (dt)^2 - V_{in} \iint_{T1} (dt)^2 = 0 \qquad (10)$$

Using the double integrator illustrated in Fig. 5b), t_2 can be determined for a negative load current step (with CCM).

Fig. 4 illustrates the charge and discharge areas for a negative load current step change of a converter that operates in discontinuous current mode (DCM). It is assumed that the converter operates with a synchronous MOSFET and uses a "diode emulation" driver to determine when the sync FET is to be deactivated; therefore, no diode drop is accounted for.

Through similar analysis as (1)-(4), A_{charge} can be calculated, as shown in (11).

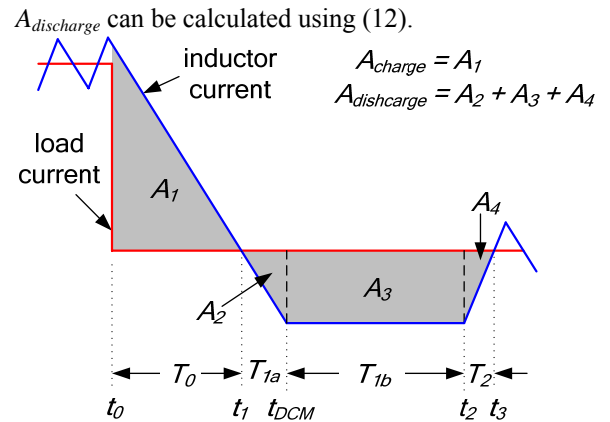$$A_{charge} = A_1 = \iint_{T0} m_2 (dt)^2 \qquad (11)$$

$A_{discharge}$ can be calculated using (12).

Fig. 4   Proposed inductor current response to a negative current step for a DCM converter

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$$A_{discharge} = A_2 + A_3 + A_4$$

$$= \iint_{T1a} m_2 (dt)^2 + \int_{T1b} m_2 \int_{T1a} dt dt + \iint_{T1a} \frac{m_2}{-m_1} (dt)^2 \qquad (12)$$

$$= \iint_{T1} \frac{m_1 m_2 - m_2^2}{m_1} (dt)^2 + \int_{T1b} m_2 \int_{T1a} dt dt$$

In order to balance the charges, (11) and (12) can be used to produce (13).

$$A_{charge} - A_{discharge} = 0$$

$$\iint_{T0} m_2 (dt)^2 - \iint_{T1} \frac{m_1 m_2 - m_2^2}{m_1} (dt)^2 - \int_{T1b} m_2 \int_{T1a} dt dt = 0 \qquad (13)$$

By substituting the known values ($m_1 = (V_{in}\text{-}V_o)/L$; $m_2 = -V_o/L$) and simplifying, (14) is calculated.

$$\iint_{T0} (V_{in} - V_o)(dt)^2 - \iint_{T1aD} V_{in} (dt)^2 - \int_{T1bD} \left(\int_{T1aD} (V_{in} - V_o) dt \right) dt = 0 \qquad (14)$$

Therefore, using the double integrator illustrated in Fig. 5c), t_2 can be determined.

IV.   OPERATION OF PROPOSED CONTROL METHOD

Fig. 6 illustrates the block diagram of the proposed control method.

The operation of the controller and its logic is described below.

The converter switches from its conventional controller to the proposed controller immediately following a load step change. The controller operation can be described in 4 steps.

Step 1: Detect Load Current Step Change (t_0)

The controller indirectly senses the capacitor current using a non-invasive trans-impedance amplifier, connected to the output voltage (as shown in Fig. 6).

When the capacitor current exceeds a predetermined threshold, the controller will immediately change the duty cycle to 100% (for a positive load step), or 0% (for a negative load step).

The controller logic will release the "reset" switch of integrator 1a and integrator 2. The output of integrator 1a will begin to increase linearly with a slope of V_o (for a positive step change), or V_{in}-V_o, (for a negative step change). The output of integrator 2 will begin to increase exponentially.

Step 2: Detect Capacitor Current Cross-over (t_1)

A comparator, fed by the capacitor current sensor, is used to determine the point at which the capacitor current changes direction. This point indicates that the inductor current has

a) Positive load step   b) Negative load step (CCM)   c) Negative load step (DCM)
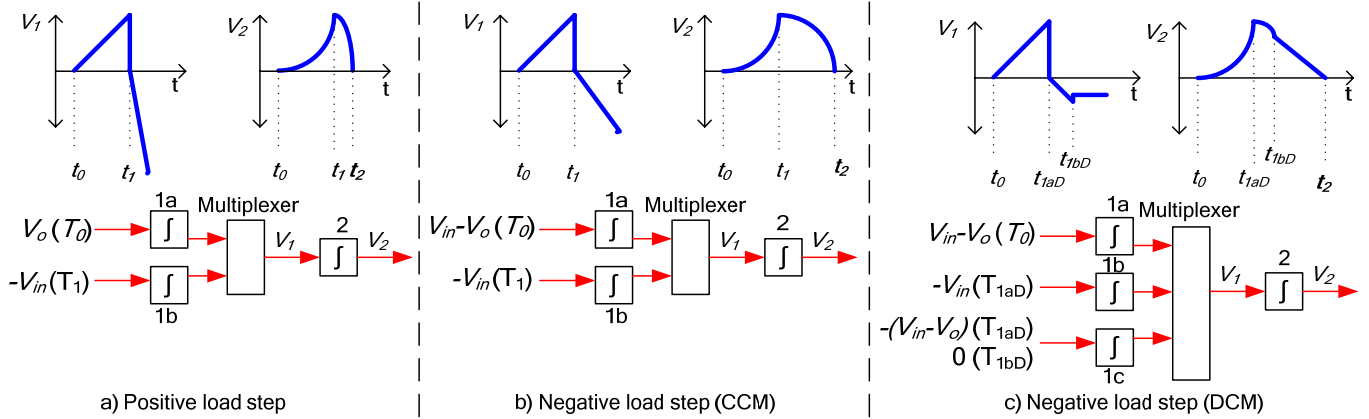
Fig. 5   Proposed double integrator for to calculate t_2 for a) positive load step, b) negative load step (CCM) and c) negative load step (DCM)
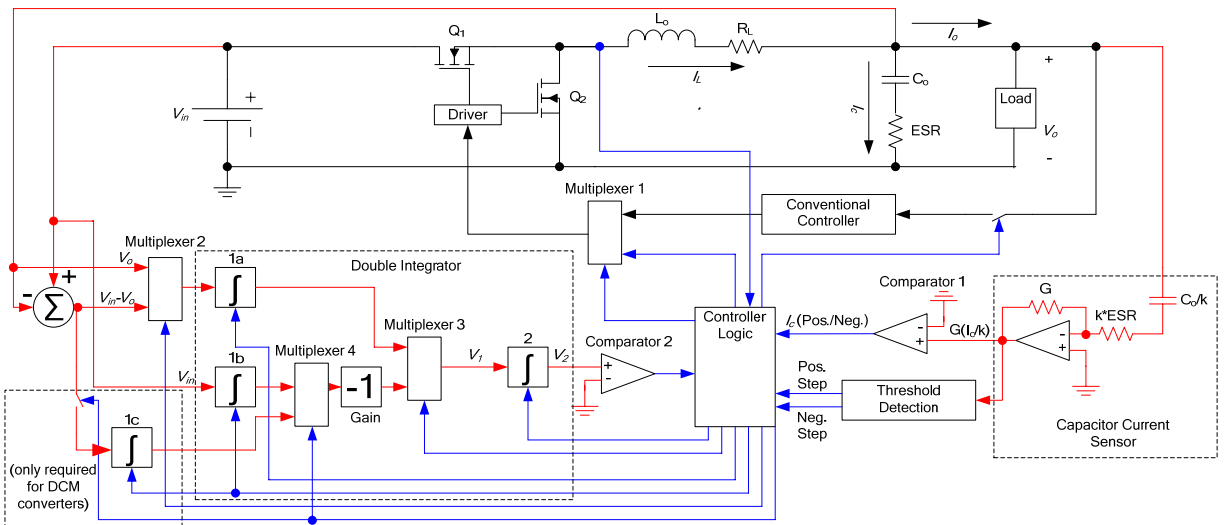

Fig. 6   Block diagram of proposed controller

reached the new load current. At this point, integrator 1a will be "reset" and integrator 1b will be activated. The output of integrator 1b will begin to decrease linearly with a slope of $-V_{in}$. The output of integrator 2 will begin to decrease exponentially.

Step 2a): Detect DCM (for DCM converters undergoing a negative current step change only) (t_{DCM})

By observing the drain voltage of the synchronous FET while the main FET is off, the moment that the converter enters DCM can be detected. At this point, the "hold" switch of integrator 1c is opened and multiplexer 3 is switched to the output of integrator 1c. The output of integrator 2 will begin to decrease linearly.

Step 3: Alter Duty Cycle (t_2)

At the moment that the output of integrator 2 returns to zero (at t_2), the duty cycle will be set to 0% (for a positive load change) or 100% (for a negative load change). At this point, the inductor current will be at its maximum (in the case of a positive load change) or its minimum (in the case of a negative load change). The inductor current will begin to decrease toward the new load current in the case of a positive load step change. In the case of a negative load change, the inductor current will begin to increase toward the new load current.

Step 4: De-activate Controller (t_3)

At t_3, the inductor current reaches the new load current (determined by a second capacitor current switchover) and the output voltage returns to its reference value. At this point, the controller deactivates and the conventional controller resumes control of the converter.

V. CALCULATED SETTLING TIME AND VOLTAGE DEVIATION

In addition to improving the dynamic performance of a Buck converter, the proposed controller also simplifies the design of the output filter since its response to a large-signal load transient is predictable. It is possible to calculate the dynamic response (settling time, voltage deviation) to a converter experiencing an arbitrary load variation. The results of this analysis are presented in this paper. Full derivation of the following equations is presented in [14].

The settling time for an arbitrary positive load step is computed in (15).

$$T_{set\_pos} = \frac{L\Delta I}{(V_{in} - V_o)}\left(1 + \frac{V_{in}}{V_o}\sqrt{\frac{V_o}{V_{in}}}\right) \quad (15)$$

For a negative load step (for a CCM converter), the settling time is calculated in (16).

$$T_{set\_neg} = \frac{L\Delta I}{V_o}\left[1 + \left(\frac{V_{in}}{V_{in} - V_o}\right)\sqrt{\frac{(V_{in} - V_o)}{V_{in}}}\right] \quad (16)$$

It should be noted that the settling time is only dependant on the inductor value, not the capacitor value. Using (15) and (16), for a CCM-only Buck converter (with the following parameters: V_{in} = 12V, V_o = 1.5V, L = 1uH) the settling times for a positive and negative 10A load current step change are calculated to be 3.6us and 13.8us respectively.

Under the proposed controller, it is also possible to calculate the voltage deviation due to an arbitrary load current step change.

The expected output voltage deviation for a positive and negative current step change is expressed in (17) and (18) respectively.

$$\Delta v_{o\_pos} = -\frac{ESR^2 \cdot C^2\left(V_{in}^2 - 2V_{in}V_o + V_o^2\right) + \Delta I^2 L^2}{2(V_{in} - V_o)L \cdot C} \quad (17)$$

$$\Delta v_{o\_neg} = \frac{ESR^2 \cdot C^2 \cdot V_o^2 + \Delta I^2 L^2}{2V_o \cdot L \cdot C} \quad (18)$$

Using (17) and (18) the voltage deviation for a Buck converter (V_{in} = 12V, V_o = 1.5V, L = 1uH, C = 180uF, ESR = 0.5mΩ) for a positive and negative 10A load current step are calculated to be -26.7mV and 185mV respectively.

VI. SIMULATION RESULTS

The parameters of the simulated Buck converter were as follows: V_{in}=12V, V_{out}=1.5V, f_s=400kHz, L=1uH, C=180uF, ESR=0.5mΩ, ESL = 100pH.

Fig. 7 shows the minimum time control method response to a 0A→10A load step change. Fig. 8 shows the response to a 10A→0A (CCM) load step change.
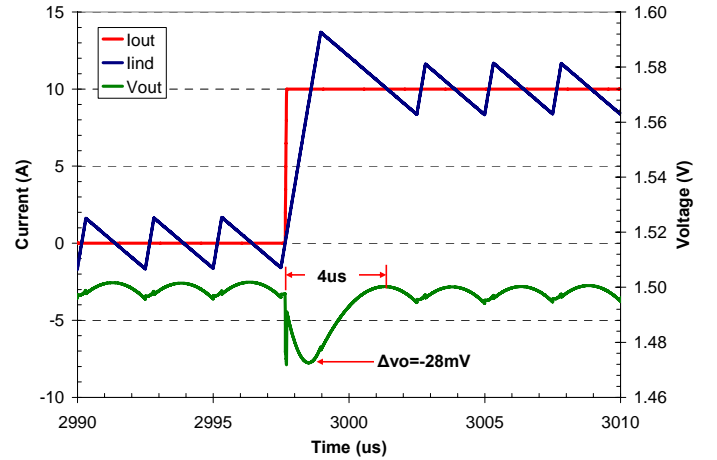

Fig. 7   Simulated proposed controller response to a 0A→ 10A load current step change
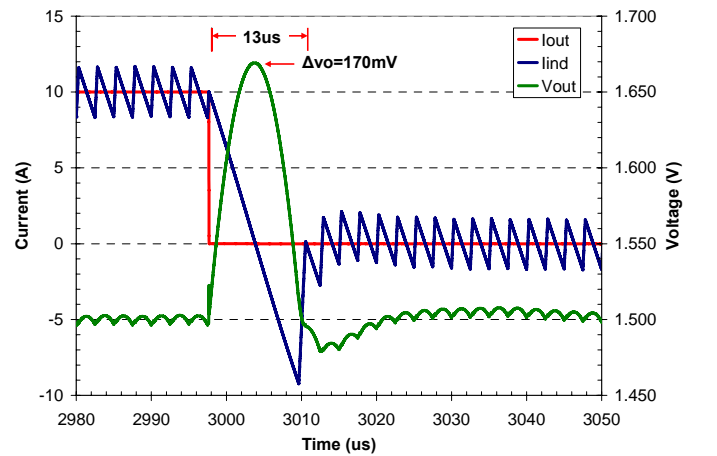

Fig. 8   Simulated proposed controller response to a 10A→ 0A load current step change (for CCM converter)

Fig. 9 illustrates the minimum time control response to a 12.5A→2.5A load step for a DCM converter using diode emulation.
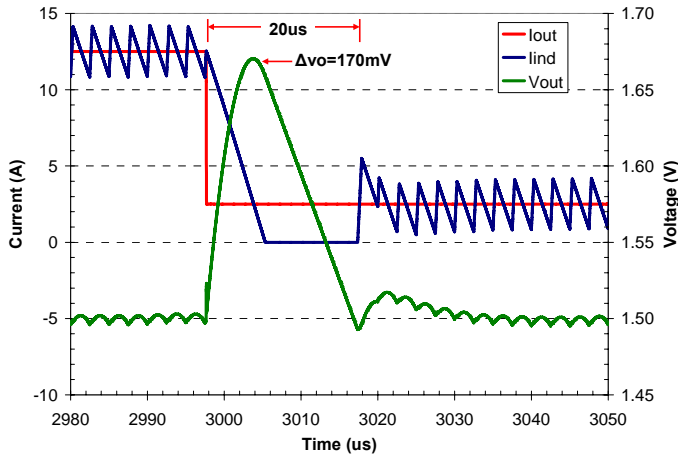

Fig. 9   Simulated proposed controller response to a 12.5→2.5A load current step change (for a DCM converter utilizing diode emulation)

It is determined that the simulation results of the proposed controller are similar to the predicted results calculated in Section V.

VII.   EXPERIMENTAL RESULTS

A prototype of the minimum time control method was designed and implemented with the aforementioned converter. The prototype was tested with load steps with a slew rate >75A/us. Fig. 10 and Fig. 11 show a voltage-mode controlled Buck converter (with a bandwidth of approximately 50kHz and a phase margin of approximately 45 degrees) and a Buck controlled by the proposed method undergoing a 0A→10A load step change respectively.

Fig. 12 and Fig. 13 show a voltage-mode controlled CCM Buck converter and a Buck controlled by the proposed method undergoing a 10A→0A load step change respectively.
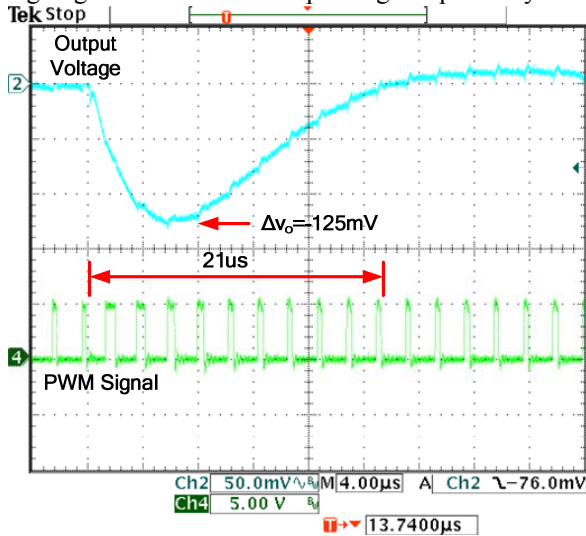

Fig. 10   Voltage-mode controlled converter undergoing a 0A→10A load step
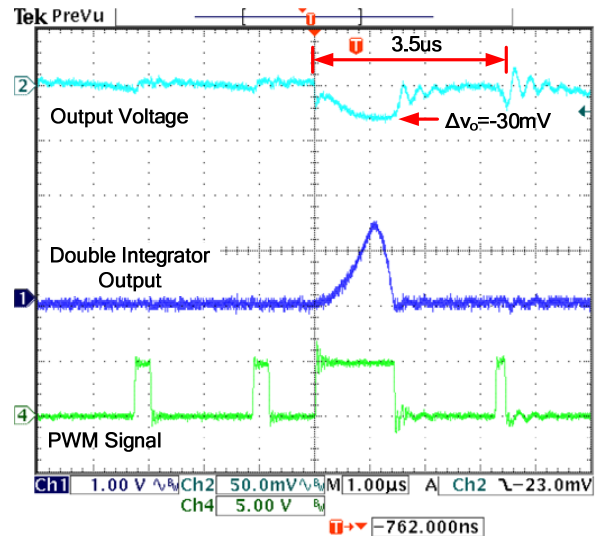

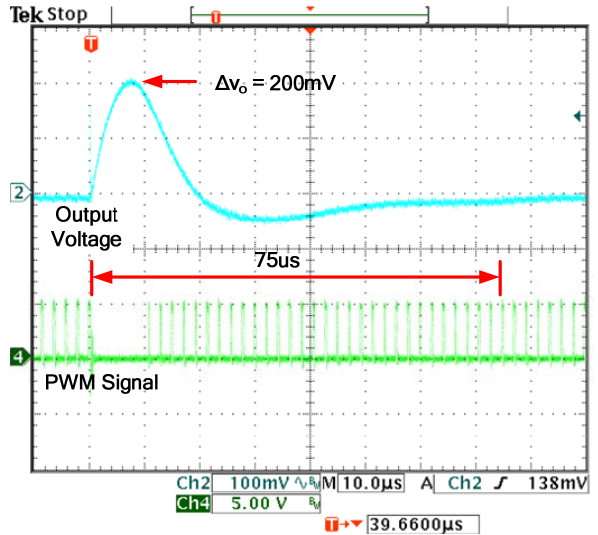Fig. 11   Proposed controller undergoing a 0A→10A load step

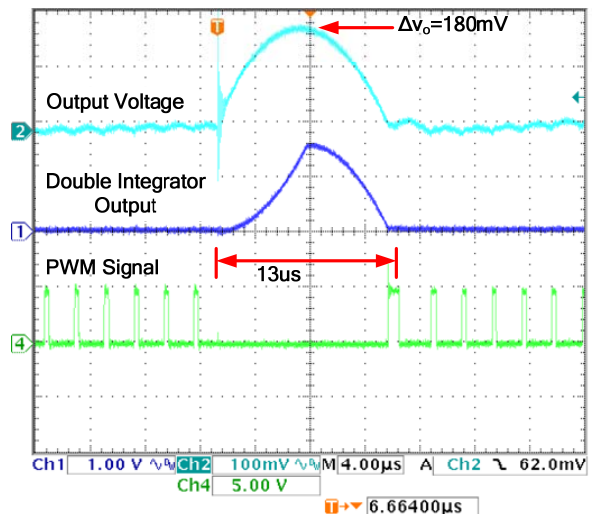Fig. 12   Voltage-mode controller response to a 10A→ 0A load step

Fig. 13   Proposed controller response to a 10A→ 0A load step

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A DCM converter was constructed with a diode emulation synchronous driver (ISL6208). Fig. 14 and Fig. 15 show a voltage-mode controlled DCM Buck converter and a Buck controlled by the proposed method undergoing a 12.5A→2.5A load step change respectively.
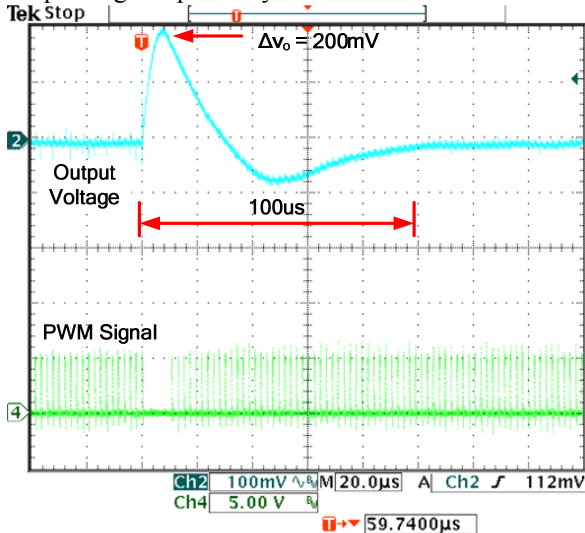

Fig. 14   Voltage-mode controlled converter undergoing a 12.5A→2.5A load step (for a DCM converter utilizing diode emulation)
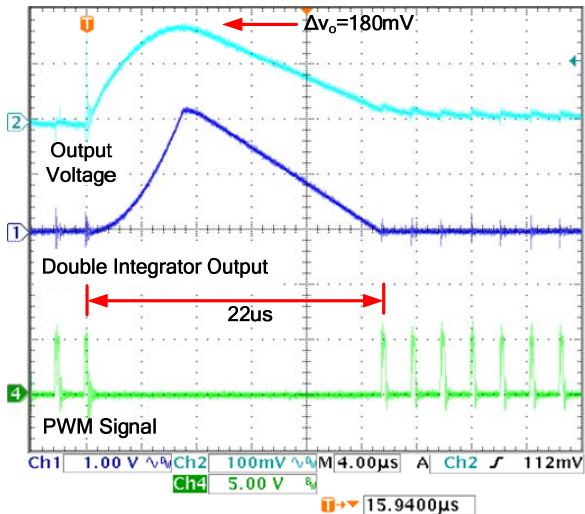

Fig. 15   Proposed controller undergoing a 12.5A→2.5A load step (for a DCM converter utilizing diode emulation)

For a positive 10A current step, the proposed controller improves the voltage undershoot by 76% and improves the settling time by 81% over that of the voltage-mode controlled Buck. For a negative 10A current step (CCM), the proposed controller improves the voltage overshoot by 10% and improves the settling time by 84% over that of the voltage-mode controlled Buck. For a negative 10A current step (DCM), the proposed controller improves the voltage overshoot by 10% and improves the settling time by 78% over that of the voltage-mode controlled Buck.

It is demonstrated that the experimental results are in close correspondence to the predicted and simulated results.

VIII. CONCLUSIONS

A practical optimal controller has been presented in this paper. The proposed control method only requires simple analog functions (such as comparison and integration) and is therefore not limited by the slow response of analog multipliers. The controller ensures a predictable response to a load variation, with the minimum possible voltage deviation and settling time. The predictable response greatly simplifies the design procedure of the output filter of a Buck converter. Using a set of simple equations, a designer can be guaranteed that the converter will be stable and operate within output voltage regulation criteria. Simulation and experimental results confirm the operation of the controller and demonstrate the significant improvement in dynamic response over tradition linear controllers.

IX.   REFERENCES

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