A Novel Non-Isolated Two-Phase Full Bridge Topology for VRM Applications

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***Abstract* - In this paper a new full bridge topology called the Two-Phase Non-isolated Full Bridge (NFB) is introduced. The proposed two-phase NFB can handle the same power as two parallel one-phase NFBs, but with less MOSFETs, better efficiency and lower cost.To demonstrate the advantages of the new topology, two prototypes are built on a 12 layer 2oz PCB board, one with four inductors, the other with three inductors. Two prototypes achieve 82.3% & 82% efficiency at 1MHz full load (1V/80A) respectively. This is compared to 81.8% efficiency of the two paralleled one-phase NFBs. At light load (1V/10A), a 4% efficiency improvement is achieved. Experimental results demonstrate that compared with two paralleled one-phase NFBs the two-phase NFB is able to achieve better efficiency with a simplified power train circuit and reduced cost.**

I. INTRODUCTION

With the continued improvements in integrated circuit technology, next generation CPUs will operate at much higher clock frequencies and consume more power. To reduce power consumption, CPUs will operate at supply voltages below 1V with tight voltage tolerance, large current demand (above 100A), and fast dynamic response (above 100A/s) [1].

The multi-phase interleaved Buck converter is the most popular topology for VRM design because of its low cost. However this topology also has some drawbacks:

1) If an output current of 100A is required, assuming 20A/phase, a five-phase buck converter is required. If the output current keeps increasing, more phases would be needed. Eventually the multi-phase Buck will become overly complex and will no longer be cost effective.

2) The Buck converter has an extremely narrow duty cycle for output voltages at and below 1V. Narrow duty cycles yield high switching loss which limits the Buck's switching frequency and makes it difficult to design a Buck based VRM that can achieve high efficiency at a high switching frequency. A narrow duty cycle also reduces the effectiveness of current ripple cancellation by using phase shift control.

3）Using too many phases in parallel makes current sharing complex.

To solve the aforementioned problems several new topologies have been proposed. The topologies proposed in [5]-[10] are Buck based topologies that use coupled-inductors or transformers to extend the duty cycle. The major drawback of these topologies is that the voltage stress of the control MOSFET is higher than the input voltage, so an auxiliary circuit is often required to limit the voltage stress on the switches. Furthermore, these topologies operate in hard switching mode, so switching losses prevent them from being suitable candidates at very high switching frequencies.

To solve the problems of the conventional Buck, a new single phase non-isolated full bridge is proposed in [2]. It demonstrates significant advantages over the conventional multi-phase Buck, however, if 80A or more output current is required, two parallel NFBs would be required; this solution is complex and not cost effective.

In this paper a new two-phase Non-Isolated Full Bridge (NFB) topology is proposed with significant advantages over two parallel NFBs, and it can reduce the cost and double the output current with better efficiency. The detailed operation of the proposed topology is presented and analyzed in the following sections.

II. DERIVATION AND OPERATION OF THE TWO-PHASE NON ISOLATED FULL BRIDGE

Fig 1 illustrates the evolution of the two-phase non-isolated full bridge from two paralleled one-phase NFBs. Fig 1a) illustrates two one-phase NFBs in parallel. Since the conduction loss of the SR is the most significant loss in low voltage high current applications, we simply parallel the two rectifier stages, and this forms the rectifier stage of the two-phase NFB shown in Fig 1b).

When the rectifier stage is in parallel, the primary side should also operate in parallel, this is illustrated in Fig 1b). Since the primary side operates in parallel, point B and D shown in Fig 1b) can be connected together. When the two primary side windings are connected at B as show in Fig 1c), it is observed that QA, Q3 and Q4, QB actually operates in parallel. Considering the conduction loss at the primary side is usually insignificant, four MOSFETs (Q3, Q4, QA and QB) can be combined to two MOSFETs (Q3 and Q4) to simplify the circuit. After making the aforementioned modifications, a new topology is created, as shown in Fig 2.

The primary side windings of T1 and T2 in Fig 2 are connected at B, which means for the secondary side windings there are two points that have the same voltage and can be connected together. It is observed that the DS voltages of SR1 and SR4 are exactly the same, so they can be connected together and SR4 and L4 can be removed. The further simplified two-phase NFB is show in Fig 3. This change will result in higher conduction loss for the rectifier stage, but the total gate loss and cost is reduced.

Using the proposed topology many benefits can be achieved; 1) Components cost is reduced；2) Better efficiency is achieved. A more detailed analysis is shown in section V；3) Current sharing is simplified due to the sharing leg (Q3, Q4) which makes two power stages coupled with each other；4)

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Compared with the single phase topology [12], a smaller output capacitor and inductor can be used to improve dynamic performance；5）Since SR1 and SR4 operate in parallel, the number of SRs and inductors can be reduced from four to three if necessary. The further simplified two-phase NFB is shown in Fig 3. A more detailed analysis of those benefits will be shown in the following sections.

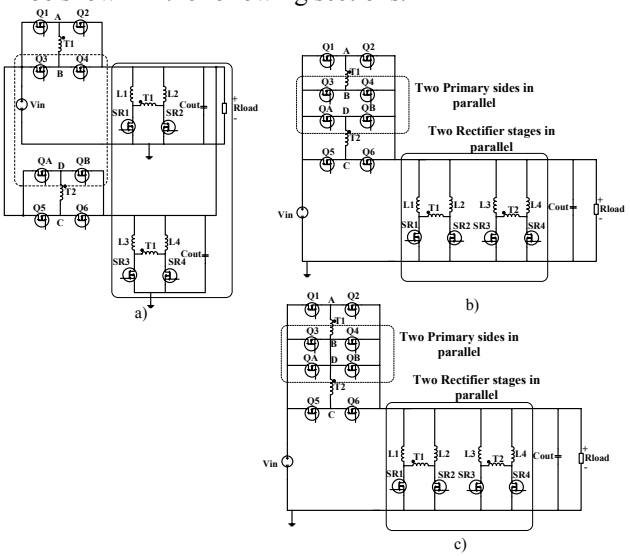

Fig 1 Evolution of the two-phase non-isolated full bridge from two paralleled one-phase NFBs

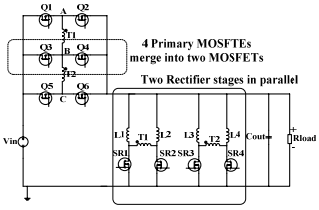

Fig 2 Proposed new two-phase non-isolated full bridge

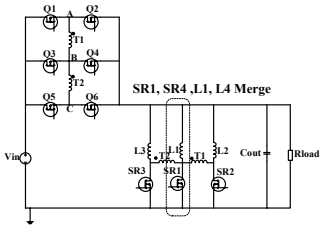

Fig 3 Two-phase non-isolated full bridge with simplified rectifier stage

Fig 4 depicts the key waveforms of the two-phase NFB. There are thirteen operation modes and they will be analyzed in detail in section III. The synchronous MOSFET driving signal $V_{GSSR1,4}$, V_{GSSR2}, and V_{GSSR3} are generated by the voltages from point A, B, C respectively, as shown in Fig 2. SR1 and SR4 are driven by the same driver because they operate in parallel. It is also noted that the source of MOSFETs Q2, Q4 and Q6 are directly connected to the output, thus they are turned off by -Vo, which allows them to be turned off faster to reduce switching loss.

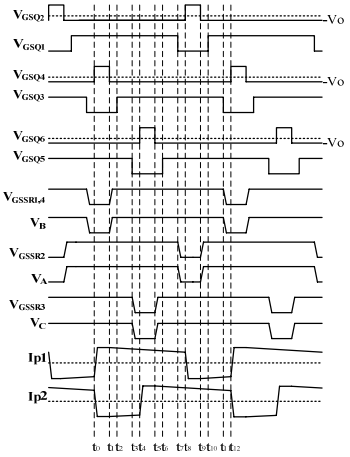

Fig 4 Key waveforms of the two-phase NFB operating in phase shift mode.

III. Operation Modes

In this section the operation modes of the new topology will be analyzed. There are a total of thirteen operation modes. The thirteen operation modes are in correspondence with the key waveforms shown in Fig 4.

The first state is from t0-t1 illustrated in Fig 5. In this operation mode Q1, Q4, Q5, SR2, SR3 are on. Q2, Q3, Q6 SR1 and SR4 are off. Energy is transferred by transformer T1 and T2 from the primary side to the secondary side. Two transformers operate in parallel and the input current travels to the load side directly. The current stress of the output inductors and the SRs is reduced as a result. During this time interval the current in Q1 and Q5 conducts through Q4 causing the current stress of Q4 to be doubled compared to that of Q1 and Q5.

The second state is from t1-t2 illustrated in Fig 6. In this operation mode Q4 is turned off at t1 to prepare for the zero voltage turn-on of Q3. The load current reflected from the secondary side begins charging C4 while discharging C3. V_B increases linearly from Vo to Vin. The gate voltage of SR1 and SR4 also begins to increase, and SR1 and SR4 will be turned on after their gate voltage increases above the threshold. However, due to the leakage inductance, SR1 and SR4 will not share the load current after they are turned on.

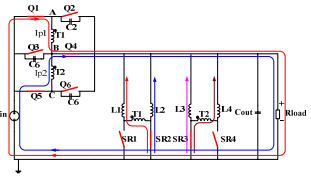

Fig 5 t0-t1

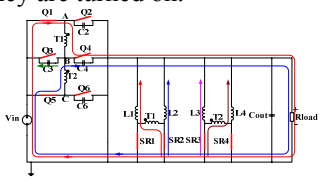

Fig 6 t1-t2

The third mode is from t2-t3 illustrated in Fig 7. When the voltage across Q3 equals zero, Q3 is turned on with ZVS at t2.

The fourth state is from t3-t4 illustrated in Fig 8. Q5 is turned off at t3 to prepare for the ZVS turn-on of Q6. The

energy stored in the leakage inductance of T2 charges C5 and discharges C6. V_C decreases from Vin to Vo. The gate voltage of SR3 also begins to decrease, and its body diode begins conducting after its gate voltage reduces below the threshold.

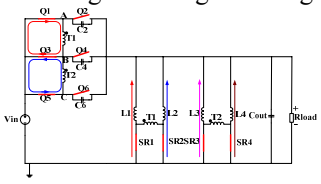

Fig 7 t2-t3

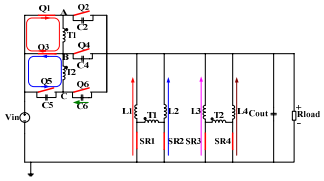

Fig 8 t3-t4

The fifth state is from t4-t5 illustrated in Fig 9. Q6 is turned on at t4 after the voltage across it becomes zero. The primary side current of T2 can not change direction instantly after Q6 is turned on. Thus Vin-Vo is added across the leakage inductance of T2 before -Ip2 changes to +Ip2. The body diode of SR3 is conducting and will be turned off after -Ip2 changes to +Ip2.

The sixth state is from t5-t6 illustrated in Fig 10. Q6 is turned off at t5 to prepare for the ZVS turn-on of Q5. The load current reflected from secondary side charges C6 and discharges C5. Vc increases from Vo to Vin. The gate voltage of SR3 also increases. SR3 is turned on after its gate voltage increases above the threshold; however SR3 will not share the load current after it is turned on due to the leakage inductance.

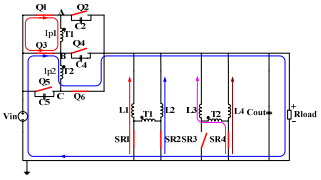

Fig 9 t4-t5

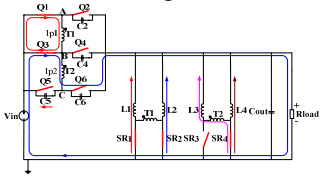

Fig 10 t5-t6

The seventh state is from t6-t7 illustrated in Fig 11. Q5 is turned on at t6 after the voltage across it becomes zero. At this time, the primary side and the secondary side of T2 are both shortened and SR3 begins to share the load current.

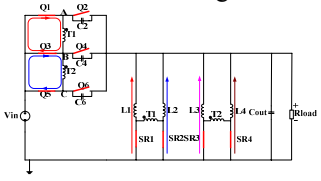

Fig 11 t6-t7

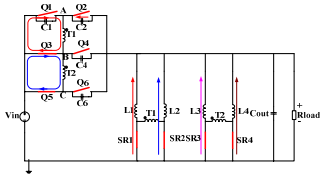

Fig 12 t7-t8

The eighth state is from t7-t8 illustrated in Fig 12. Q1 is turned off at t7 to prepare for the ZVS turn-on of Q2. The energy stored in the leakage inductance of T1 charges C1 and discharges C2. V_A decreases from Vin to Vo. The gate voltage of SR2 also decreases and its body diode begins to conduct after its gate voltage reduces below the threshold.

The ninth state is from t8-t9 illustrated in Fig 13. Q2 is turned on at t8 after V_A decreases to Vo. Due to the leakage inductance the primary current Ip1 can not change direction instantly; Vin-Vo will be added across the leakage inductance of T1 before Ip1 completely changes to –Ip1. After Ip1 changes to –Ip1, SR2 is turned off completely and T1 begins to transfer energy to the secondary side.

The tenth state is from t9-t10 illustrated in Fig 14. Q2 is turned off at t9 to prepare for the ZVS turn-on of Q1, the load current reflected from the secondary side charges C2 and discharges C1. V_A increases from Vo to Vin. The gate voltage of SR2 also begins to increase and SR2 is turned on after its gate voltage increases above the threshold; However, SR2 will not share the load current after it is turned on due to the leakage inductance.

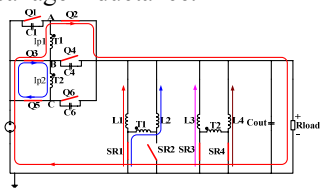

Fig 13 t8-t9

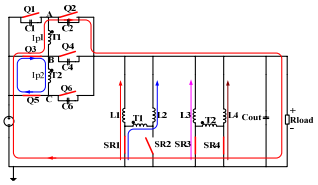

Fig 14 t9-t10

The eleventh state is from t10-t11 illustrated in Fig 15. Q1 is turned on at t10 after the voltage across it becomes zero. The primary windings of T1 are shortened, the primary side and secondary side are decoupled, and SR2 begins to share the load current.

The twelfth operation state is from t11-t12 illustrated in Fig 16. Q3 is turned off at t11 to prepare for the ZVS turn-on of Q4. The energy stored in the leakage inductance of T1 and T2 charges C3 and discharges C4. V_B decreases from Vin to Vo. The gate voltage of SR1 and SR4 also begins to decrease, and their body diodes begin to conduct after their gate voltages reduce below the threshold.

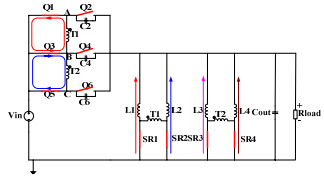

Fig 15 t10-t11

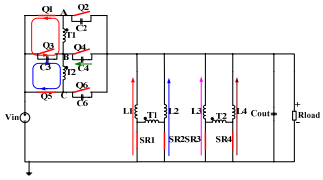

Fig 16 t11-t12

The thirteenth state is from t12-t13 illustrated in Fig 17. After the voltage across Q4 becomes zero, Q4 is turned on with ZVS at t12. Due to the leakage inductance primary current can not change its direction instantly; Vin-Vo is added across the leakage inductance of T1 and T2 and the primary current of T1 and T2 decreases from Ip to –Ip. SR1 and SR4 are turned off completely after the primary current change to -Ip and both transformers T1 and T2 begin to transfer energy to the secondary side. At this point one cycle is completed.

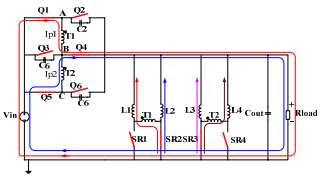

Fig 17 t12-t13

IV. Zero Voltage Transition

From the analysis in the previous sections, it is shown that Q1, Q3 and Q5 are leading leg MOSFETs. Q2, Q4 and Q6 are lagging leg MOSFETs. The output capacitors of the lagging leg MOSFETs are discharged by the energy stored in the leakage inductance, so it is more difficult for them to achieve zero voltage turn-on.

The SR's gate capacitor is in parallel with the output capacitor of Q2, Q4 and Q6 [12]. This equivalently enlarges the output capacitors of the primary side MOSFETs, and as a result increases the dead time and energy needed to achieve ZVS turn-on. The detailed analysis will be discussed in this section.

A. Leading legs, transition during [t9-t10] (Q1,Q3, Q5)

The transition paths of the leading leg are shown in Fig 14. Q2 is turned off to prepare for the zero voltage turn-on of Q1. The current reflected from the secondary side charges C2 and discharges C1. During this transition, the time required to charge C2 from Vo to Vin and discharge C1 from Vin to Vo is dependent on the load current. Since this time interval is very short, it is assumed that the charge current is constant during the transition. Equations (1) and (2) can be used to calculate the voltage across C1 and C2. If we assume C1=C2. (3) can be used to calculate the dead time needed to achieve zero voltage turn-on. Equation (3) is derived based on the assumption that during the duration of [t9~t10], the current is constant to charge C2 and discharge C1.I_{Lavg}, in (1)-(3), represents the average current in L2 and can be calculated using (4).

By using (1)-(4) the minimum dead time needed to achieve ZVS can be calculated The operating parameters are as follows:Vin=12V,Vo=1V,Fs=1MHz,Np:Ns=3:1,Np:Ns=2:1, C1=C2=2.5nF (since the SR gate capacitor is in parallel with C2, it equivalently increases the value of C1 and C2). From equation (3) it is observed that a heavy load and a low turn's ratio can help the NFB achieve ZVS. At 50A load, Td=14.4ns for N=3, and Td=9.6ns for N=2.

$$V_{C1}(t) = (V_{in} - V_o) - \frac{I_{Lavg} t}{2C2N} \tag{1}$$

$$V_{C2}(t) = \frac{I_{Lavg} t}{2C1N} \tag{2}$$

$$t_{dead\_Q12} > \frac{2C1(V_{in} - V_0)N}{I_{Lavg}} \tag{3}$$

$$I_{Lavg} = \frac{(I_o - I_{in})}{4} \tag{4}$$

B. Lagging Legs, transition during [t7-t8] (Q2 Q4 Q6)

The transition paths of the lagging leg are shown in Fig 12. Initially, Q1 is turned off to prepare for the zero voltage turn-on of Q2. If the energy stored in the leakage inductance of the transformer is sufficient to charge C1 to V_{in} and discharge C2+C_{GSR2} from V_{in} to Vo, Q2 can achieve zero voltage turn-on.

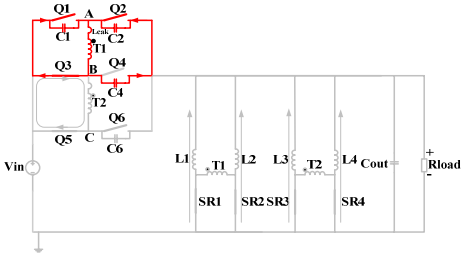

Fig 18 Lagging leg transition equivalent circuit

In this transition the leakage inductance resonates with C1 and C2+C_{GSR2}. The equivalent circuit is shown in Fig 18. If the voltage at point A can be discharged from Vin to Vo, the body diode of Q2 will be turned on. Q2 must be turned on before the current through the leakage inductance decreases to zero. The voltages across C1 and C2 can be calculated using (5)-(8). The leakage current $I_{Leakage}$, in (5) represents the current at the instant Q1 is turned off and can be estimated using (10), where Ip is the primary side current. From (5) it is observed that in order to achieve ZVS turn-on, (9) must be satisfied.

$$V_{C2}(t) = Z_o I_{Leakage} \sin \omega t - (V_{in} - V_o) \tag{5}$$

$$I_p(t) = I_{Leakage} \cos \omega t \tag{6}$$

$$V_{C1}(t) = Z_o I_{Leakage} \sin \omega t \tag{7}$$

$$Z_o = \sqrt{L_{Leakage} / 2C_1}$$

$$\omega = 1/\sqrt{2L_{Leakage} C_1} \quad t_X = \frac{1}{\omega} \sin^{-1}\left(\frac{V_{in} - V_o}{Z_o}\right) \tag{8}$$

$$\begin{cases} Z_o I_{Leakage\min} > (V_{in} - V_o) \\ \frac{1}{\omega} \sin^{-1}\left(\frac{V_{in} - V_o}{Z_o I_{Leakage}}\right) < t_{dead\_Q34} < \frac{(I_{Leakage} L_{Leakage}) \cos \omega t_X}{(V_{in} - V_o)} + t_X \end{cases} \tag{9}$$

$$I_{Leakage} = (I_o - I_{in}) / 4N \tag{10}$$

By using (5)-(10) the minimum dead time needed to achieve ZVS can be calculated. The operating parameters are as follow: V_{in}=12V, V_o=1V, C1=C2=2.5nF (since the SR gate capacitor is paralleled with C2, it equivalently increases the value of C1 and C2), $L_{Leakage}$=30nH. To chieve ZVS turn-on at 60A load for the lagging leg, Td=16.8ns for N=3 and

Td=8.7ns for N=2. And according to the calculation at 50A load current, N=3, ZVS can not be achieved.

V. Loss Comparison Between Two Paralleled One-phase NFB and The New Two-phase NFB

In this section the losses of two paralleled NFBs and the new proposed two-phase NFB will be compared. It will demonstrate that the new proposed two-phase FB has better efficiency. The comparison conditions are: Vin=12V, Vo=1V, Iout=80A, Fs=1MHz, Np:Ns=3:1 primary side MOSFETs IFR7821[13], SR IRF6619[14]. The output inductor is 100nH.

A. Switching loss

The switching loss can be calculated using (11) and (12). In a real circuit, the switching loss may be larger due to parasitic components [3]-[4], but using (11) and (12) still can be used to estimate the switching loss.

$$P_{on} = \frac{1}{2} f_s V_{ds} I_{PKon} t_r \qquad (11)$$

$$P_{off} = \frac{1}{2} f_s V_{ds} I_{PKoff} t_f \qquad (12)$$

Two-Phase NFB	Q1,Q2,Q5,Q6	Q3	Q4	Q7,Q8
Ipkoff	7.2A	7.2A	14.5A	X
Ipkon	4.8A	4.8A	9.6A	X
Vds	11V	11V	11V	X
Fs	1MHz	1MHz	1MHz	X
Two One-Phase NFBs	Q1,Q2,Q5,Q6	Q3	Q4	Q7,Q8
Ipkoff	7.2A	7.2A	7.2A	7.2A
Ipkon	4.8A	4.8A	4.8A	4.8A
Vds	11V	11V	11V	11V
Fs	1MHz	1MHz	1MHz	1MHz

Table 1 Current stress comparison between two one-phase NFB and two-phase NFB

Table 1 lists the current stress comparison between two paralleled one-phase NFBs and the two-phase NFB (the circulating current is neglected in the calculation). Form the table it is noticed that the current stress of Q4 is doubled compared with other MOSFETs. For Q3, since Iq3=Iq2+Iq6, and Iq2 and Iq6 are 120 degrees out of phase , Q3 has the same peak current as Q1, Q2, Q5 and Q6.

Solely considering switching loss, the two-phase NFB saves one primary side MOSFET compared with two one-phase NFBs. The total switching loss of the two-phase NFB is 7 times the switching loss of Q1; for the two parallel one-phase NFBs, the switching loss is 8 times the switching loss of Q1(assuming hard switching).

If only four MOSFETs at the primary side and four SRs for the rectifier stage are used, compared with two paralleled one-phase NFBs, no switching loss could be saved since the current stress of the MOSFETs at primary side would be doubled.

If we assume: 1) Ton=10nS and Toff=15nS. 2) Lagging leg does no achieve ZVS.3)Leading legs can achieve ZVS and recovery 75% of the switching loss. The calculated results: Two-phase FB switching loss=5.92W, two paralleled NFBs switching loss=6.64W.Therefore, 0.72W loss is saved.

B. Conduction loss

$$P_{con} = I_{RMS} R_{dson} \qquad (13)$$

The conduction loss can be calculated using (13). Table 1 shows the RMS current comparison between two one-phase NFBs and the two-phase NFB. Q4's RMS current is doubled compared with Q1. Q3's RMS current is between Q1 and Q4; this benefit is achieved by phase shifting the current in Q2 and Q6 120 degrees from each other.

Two-Phase NFB	Q1,Q2, Q5,Q6	Q3	Q4	Q7,Q8	SR
I_{RMS}	3.6A	5.1A	7.2A	X	22.4A
Two One-Phase NFBs	Q1,Q2, Q5,Q6	Q3	Q4	Q7,Q8	SR
I_{RMS}	3.6A	3.6A	3.6A	3.6A	22.4A

Table 2 RMS current comparison between two one-phase NFBs and two-phase NFB

At the primary side, the two-phase NFB will result in more conduction loss since it has a higher RMS current. At the secondary side they will have the same conduction loss. The calculated total MOSFETs conduction loss: Two-phase NFB conduction loss=4.47W, two paralleled NFBs conduction loss=4.24W. Therefore, there is an increase of 0.23W conduction loss for the two-phase NFB from the primary side.

C. Loss summary

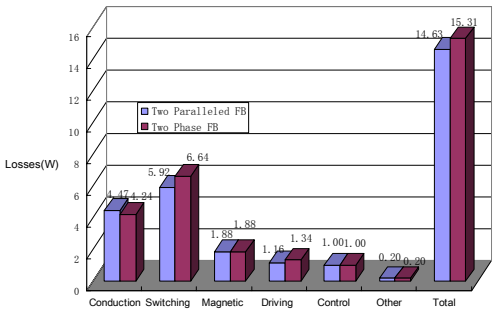

Fig 19 Losses breakdown comparison between the two-phase NFB and two paralleled NFBs at 1MHz switching frequency and 1V/80A load

The loss breakdown comparison between the two-phase NFB and two paralleled NFBs at 1MHz switching frequency is shown in Fig 19. It is observed that the total loss is reduced form 15.31W(for two paralleled NFB) to 14.63W (for two-phase NFB), 0.68W loss is saved because of the fewer

MOSFETs results in less gate loss and phase-shift control reduce the switching loss.

VI. Experimental Results

To verify the analysis in the previous sections, two prototypes were built on a 12 layer 2oz copper PCB, one with four output inductors , the other with three output inductors. The primary MOSFET is the IRF7821 and four IRF6619s are used as synchronous MOSFETs. The design parameters are: Vin=12V, Vo=1V, Fs=1MHz, Iout=80A, N=3, Lout=100nH.

Fig 20 illustrates the leading leg transition of Q5 at 10A, 1MHZ. It is observed that Vgs rises 16nS after Vds reduces to zero, and ZVS turn-on is achieved.

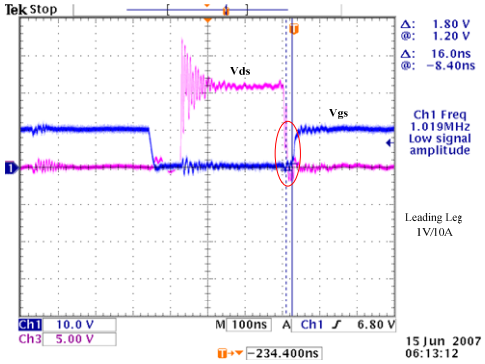

Fig 20 Zero voltage turn-on of Leading Leg MOSFET Q5 at 10A

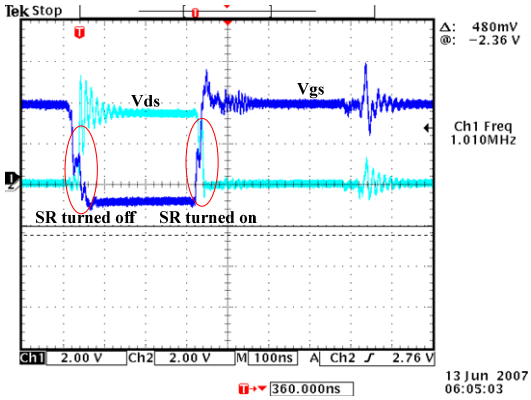

Fig 21 Synchronous MOSFETs turn-on and turn-off transition at 80A load

Fig 21 illustrates the synchronous MOSFETs turn-on and turn-off transition at 80A load. From the waveform it is observed that during the turn-on transition the SR will be turned on before it begins to conduct current, and the SR's body diode does not turn on during the turn-on transition.

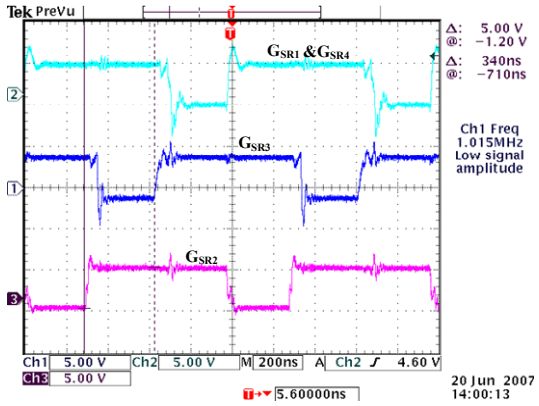

Fig 22 Gate driving signal of synchronous MOSFETs, each phase shift 120 degree

Fig 22 illustrates the gate signal of the synchronous MOSFETs. Each phase is 120 degrees shifted from each other so the ripple current of the output inductor can cancel each other. Therefore, a small output inductor can be used to improve dynamic performance. In the prototype, SR1 and SR4 are driven by the same driver.

Fig 23 depicts the measured efficiency curve of the two-phase NFB and two parallel one-phase NFBs operating at 1MHZ switching frequency. At full load (1V/80A) an efficiency of 82.3% is achieved compared with 81.8% efficiency of the two paralleled NFBs (a 0.5% improvement). At light load (1V/10A), a 4% efficiency improvement is achieved.

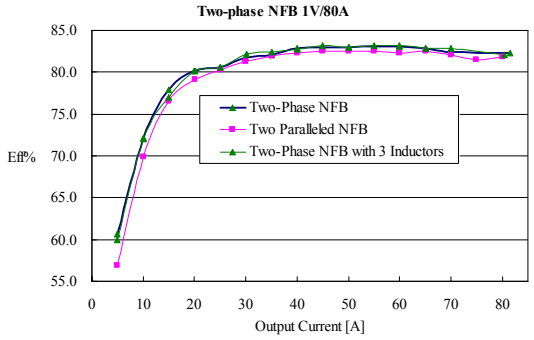

Fig 23 Measured efficiency comparison between Two-Phase NFB and two paralleled One-phase NFBs operate at 1MHz switching frequency

Another prototype with three inductors was also built and tested. It is observed from experimental results that when the number of inductors is reduced from four to three at full load (1V/80A) an efficiency of 82% is achieved. The efficiency is reduced by 0.3% because of the higher conduction loss from the output inductors, but the 82% efficiency is still better than two paralleled one-phase NFBs (81.8%).

The experimental results demonstrate that the two-phase NFB is able to achieve better efficiency compared with two paralleled one phase NFBs, and with a simplified power train

circuit and reduced cost.

A six-phase 1V/80A 1MHz Buck was also tested and with equivalent power MOSFETs. The six-phase buck is used in the comparison because a one-phase Buck reaches it peak efficiency at around 12A load. If an 80A output is required a six-phase Buck will reach peak efficiency at around 80A. From the experimental results the six-phase buck reaches a peak efficiency of 79.6% at 70A which is 2.7% lower than the peak efficiency of the two-phase NFB. Table 3 compares the number of major parts between the six-phase Buck, two one-phase NFBs and the two-phase NFB. From the comparison it is shown that the two-phase NFB has the minimum number of components and the highest efficiency.

	6 phase Buck	Two 1-phase NFBs	2-phase NFB
Total MOSFETs	12	12	10
Control MOSFETs	6	8	6
SR MOSFETs	6	4	4
Magnetics	6	6	6
Inductors	6	4	4
Transformers	0	2	2
Controllers	1	1	1
Drivers	6	4	3
Efficiency	Lowest	Medium	Highest
Cost	High	High	Low

Table 3 Number of major parts comparison between the two-phase NFB, six-phase Buck and two one-phase NFBs

VII. CONCLUSION

Two new non-isolated two phase non-isolated full bridge converter are proposed as an alternative for parallel two one-phase non-isolated full bridge converter in this paper as shown in Fig 2 and Fig 3. Compared with two paralleled one-phase NFBs, the two-phase NFB can handle the same output power. In addition, the number of MOSFETs at the primary side is reduced from eight to six. The power train is simplified and the cost is reduced. Moreover, higher efficiency can be achieved because of significant reduction of switching loss. To further reduce the cost, a further simplified two-phase NFB version also proposed and tested, from the testing results the efficiency is reduced a little due to higher conduction loss, but the cost further reduced.

To demonstrate the advantages of this topology, two VRM modules have been built and tested at 12V input and 1V output with an 80A load and a 1MHz switching frequency. The experimental results demonstrate that the two-phase NFB is able to achieve better efficiency compared with two paralleled one phase NFBs and with a simplified power train circuit and a reduced cost. The two-phase NFB is also compared with a six-phase Buck, and the testing result demonstrates that the two-phase NFB can achieve better efficiency than the six-phase Buck and with less components.

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