A Novel Isolated Two-phase Full Bridge Topology for VRM Applications

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Abstract - In this paper a new isolated full bridge is proposed. Compared with conventional full bridge the new topology can double the output power since its primary side and secondary side operate like two conventional full bridges in parallel and phase shift from each other. But it saves two switches at primary side and it achieves better efficiency. To demonstrate the advantages of the new topology two 48V input, 1V/70A output, 1MHz, power module were built on a 12 layers, 2oz copper PCB, one with four output inductors, the other with three output inductors. 81.3% &80.8% efficiency are achieved respectively at full load (1V/70A) compared with two paralleled FB 80.4% at full load (1V/70A) around 1% improvement is achieved. At light load (1V/20A), 4% improvement is achieved.

I. INTRODUCTION

Most of today's high end server and workstation use 64-bit CPUs, and 64-bit CPUs consume much more power than 32-bit CPU. In the server there will be several CPUs work in parallel, usually their power consumption is around several KW, and the power supply used for server application usually is called power pod. To meet this high power consumption requirement, 48V bus voltage has to be used for the power pod design. Since the 48V bus voltage can reduce the conduction loss, input filter size, and it is more stable than 12V bus voltage during load transition [1] [1].

There are lots of isolated topologies which can be used for power pod. Such as half bridge, push-pull ects. The major drawback of those topologies is that they operate in hard switching mode, so they are not capable to operate at 1MHz switching frequency. In the future in order to reduce the power consumption, the CPU will need supply voltage below 1V, and require tight voltage tolerance during load transition. This will push the operation frequency of power supply to operation in the MHz range [3]-[10].

For the ZVS full bridge, when the output current required is very high around 100A, two or more isolated full bridge or other topology will be needed to supply the output current in parallel. This solution makes current sharing difficult, and not cost effective

In this paper a new two-phase isolated full bridge is proposed to solve the aforementioned problem. The new topology is capable to achieve soft switching and double the output current; in addition it can achieve higher efficiency than two one-phase FBs in parallel. In following sections the detail operation of the new topology will be analyzed.

II. DERIVATION AND OPERATION OF THE TWO-PHASE NON ISOLATED FULL BRIDGE

Fig 1 illustrates the evolution of the two-phase isolated full bridge from two paralleled one-phase FBs. Fig 1 a) illustrates two one-phase FBs in parallel. Since the conduction loss of the SR is the most significant loss in low voltage high current applications, we simply parallel the two rectifier stages, and this forms the rectifier stage of the two-phase NFB shown in Fig 1b).

When the rectifier stage is in parallel, the primary side should also operate in parallel, this is illustrated in Fig 1b). Since the primary side operates in parallel, point B and D shown in Fig 1b) can be connected together. When the two primary side windings are connected at B as show in Fig 1c), it is observed that QA, Q3 and Q4, QB actually operates in parallel. Considering the conduction loss at the primary side is usually insignificant, four MOSFETs (Q3, Q4, QA and QB) can be combined to two MOSFETs (Q3 and Q4) to simplify the circuit. After making the aforementioned modifications, a new topology is created, as shown in Fig 2.

The primary side windings of T1 and T2 in Fig 2 are connected at B, which means for the secondary side windings, there are two points that have the same voltage and can be connected together. It is observed that the DS voltages of SR1 and SR4 are exactly the same, so they can be connected together and SR4 and L4 can be removed. The further simplified two-phase FB is show in Fig 3. This change will result in higher conduction loss for the rectifier stage, but the total gate loss and cost is reduced.

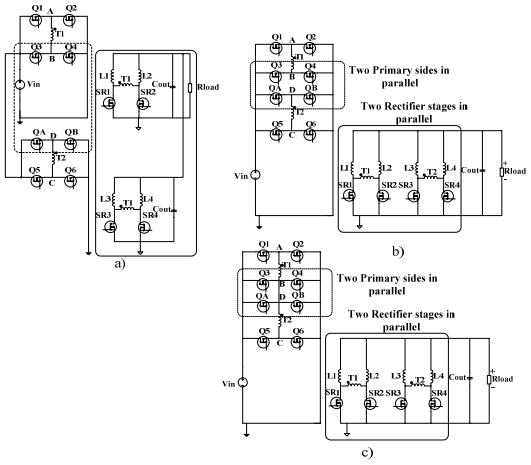

Fig 1 Evolution of the two-phase isolated full bridge from two paralleled one-phase NFBs

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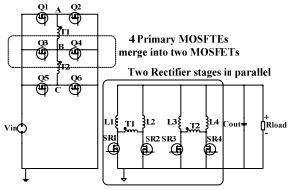

Fig 2 Proposed new two-phase isolated full bridge

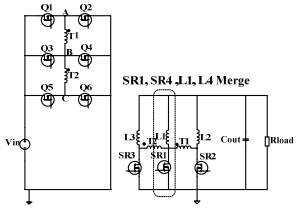

Fig 3 Two-phase isolated full bridge with simplified rectifier stage

Fig 4 depicts the key waveforms of the two-phase FB. There are thirteen operation modes and they will be analyzed in detail in section III. In Fig 4 V_{GSQ1}-V_{GSQ6} are the gate driving signals of corresponding MOSFETs in Fig 2, Ip1 and Ip2 represent the current goes through the primary windings of transformer T1 and T2 shown in Fig 2.

The synchronous MOSFET driving signal $V_{GSSR1\&SR4}$, V_{GSSR2}, and V_{GSSR3} are generated by the voltages V_A V_B V_C from point A, B, C respectively as shown in Fig 2. SR1 and SR4 are driven by the same driver because they operate in parallel.

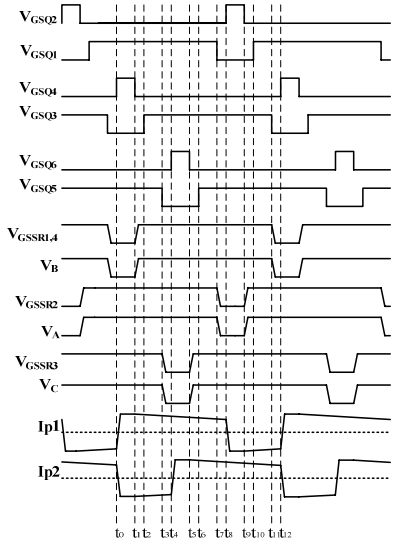

Fig 4 Key waveforms of the two-phase NFB operating in phase shift mode.

III. Operation Modes

In this section the operation modes of the new topology are analyzed in detail, and the impact of transformer's leakage inductance on the SR body diode conduction time will also be discussed. There are a total of thirteen operation modes. The thirteen operation modes are in correspondence with the key waveforms shown in Fig 4. In the analysis T1 and T2 represent the two transformers in Fig 2, and Ip1 and Ip2 represent the current goes through the primary windings of transformer T1 and T2.

The first state is shown in Fig 5 from t0- t1. In this operation mode Q1, Q4, Q5, SR2, SR3 are on. Q2, Q3, Q6 SR1 and SR4 are off. Energy is transferred by transformer T1 and T2 from the primary side to the secondary side. Two transformers operate in parallel and the input current flows to the load side directly. The current stress of the output inductors and the SRs is reduced as a result. During this time interval the current in Q1 and Q5 both conduct through Q4 causing the current stress of Q4 to be doubled compared to that of Q1 and Q5

The second state t1-t2 is shown in Fig 6. In this operation mode Q4 is turned off at t1 to prepare for the zero voltage turn-on of Q3. The load current reflected from the secondary side begins charging C4 while discharging C3. The voltage at point B(V_B) increases linearly from 0 to Vin. The gate voltage of SR1 and SR4 also begins to increase, and SR1 and SR4 will be turned on after their gate voltage increases above the threshold. However, due to the leakage inductance, SR1 and SR4 will not share the load current after they are turned on. In this transition, the gate capacitors of SR1 and SR4 are charged by a constant current source and their gate loss can be reduced.

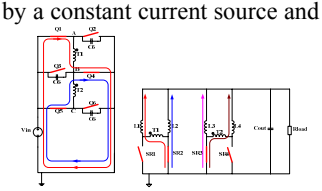

Fig 5 t0-t1

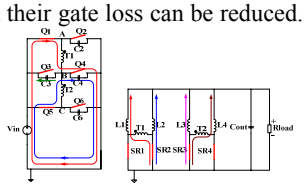

Fig 6 t1-t2

The third mode is from t2-t3 illustrated in Fig 7. When the voltage across Q3 equals zero, Q3 is turned on with ZVS at t2.

The fourth state is shown in Fig 8. Q5 is turned off at t3 to prepare for the ZVS turn-on of Q6. The energy stored in the leakage inductance of T2 charges C5 and discharges C6. The voltage at point C (V_C) decreases from Vin to 0. The gate voltage of SR3 also begins to decrease, and its body diode begins conducting for a short period of time after its gate voltage reduces below the threshold. This time interval should be as small as possible.

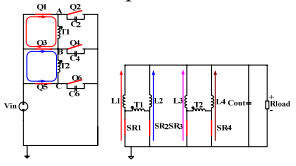

Fig 7 t2-t3

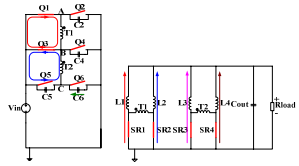

Fig 8 t3-t4

The fifth state is shown in Fig 9. Q6 is turned on at t4 after the voltage across it becomes zero. The primary side current of T2 can not change direction instantly after Q6 is turned on. Thus Vin is applied across the leakage inductance of T2 before the primary side current -Ip2 changes to +Ip2. The body diode of SR3 is conducting and will be turned off after -Ip2 changes to +Ip2.

The sixth state is shown in Fig 10. Q6 is turned off at t5 to prepare for the ZVS turn-on of Q5. The load current reflected from secondary side charges C6 and discharges C5. Vc increases from 0 to Vin. The gate voltage of SR3 also increases. SR3 is turned on after its gate voltage increases above the threshold; however SR3 will not conduct the load current immediately after it is turned on due to the leakage inductance.

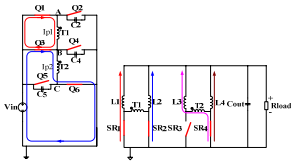

Fig 9 t4-t5

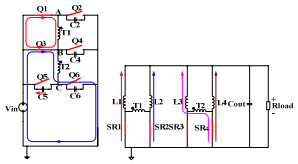

Fig 10 t5-t6

The seventh state is shown in Fig 11. Q5 is turned on at t6 after the voltage across it becomes zero. At this time the primary side and secondary side of T2 are both shortened, SR3 begins to share the load current.

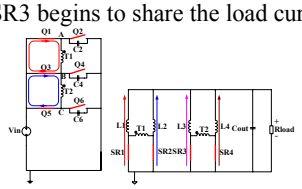

Fig 11 t6-t7

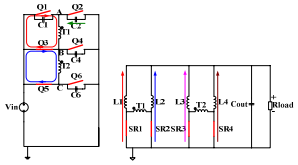

Fig 12 t7-t8

The eighth state is shown in Fig 12. Q1 is turned off at t7 to prepare for the ZVS turn-on of Q2. The energy stored in the leakage inductance of T1 charges C1 and discharges C2. The voltage at point A (V_A) decreases from Vin to 0. The gate voltage of SR2 also decreases and its body diode begins to conduct for a very short time after its gate voltage reduces below the threshold.

The ninth state is shown in Fig 13. Q2 is turned on at t8 after V_A decreases to 0. Due to the leakage inductance the primary current Ip1 can not change direction instantly; Vin will be applied across the leakage inductance of T1 before Ip1 completely changes to –Ip1. After Ip1 changes to –Ip1, SR2 is turned off completely and T1 begins to transfer energy to the secondary side.

The tenth state is shown in Fig 14. Q2 is turned off at t9 to prepare for the ZVS turn-on of Q1, the load current reflected from the secondary side charges C2 and discharges C1. V_A increases from 0 to Vin. The gate voltage of SR2 also begins to increase and SR2 is turned on after its gate voltage increases above the threshold; However, SR2 will not conduct the load current after it is turned on due to the leakage inductance

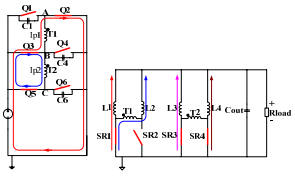

Fig 13 t8-t9

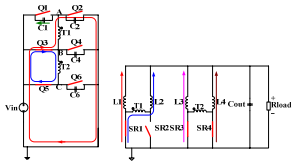

Fig 14 t9-t10

The eleventh state is shown in Fig 15. Q1 is turned on at t10 after the voltage across it becomes zero. The primary windings of T1 are shortened, the primary side and secondary side are decoupled, and SR2 begins to conduct the load current.

The twelfth operation state is shown in Fig 16. Q3 is turned off at t11 to prepare for the ZVS turn-on of Q4. The energy stored in the leakage inductance of T1 and T2 charges C3 and discharges C4. V_B decreases from Vin to 0. The gate voltage of SR1 and SR4 also begins to decrease, and their body diodes begin to conduct for a very short time after their gate voltages reduce below the threshold.

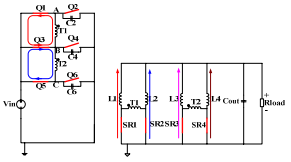

Fig 15 t10-T11

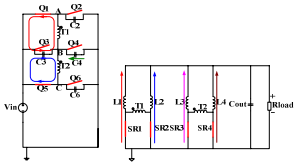

Fig 16 t11-t12

The thirteenth state is shown in Fig 17. After the voltage across Q4 becomes zero, Q4 is turned on with ZVS at t12. Due to the leakage inductance primary current can not change its direction instantly, Vin is applied across the leakage inductance of T1 and T2 and the primary current of T1:-Ip1 changes to +Ip1 and T2: +Ip2 changes to –Ip2. SR1 and SR4 are turned off completely after the primary currents of T1 and T2 change direction completely and both transformers T1 and T2 begin to transfer energy to the secondary side. At this point one cycle is completed.

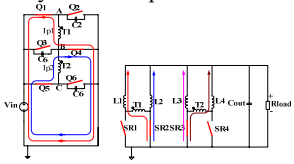

Fig 17 t12-t13

IV. Zero Voltage Transition

From the analysis in the previous sections it is shown that the Q1, Q3 and Q5 are leading leg MOSFETs. Q2, Q4 and Q6 are lagging legs MOSFETs. The output capacitors of the lagging leg MOSFETs are discharged by the energy stored in the leakage inductance, so it is more difficult for them to achieve zero voltage turn-on. The detail analysis will be

discussed in this section.

A. Leading legs transition [t9-t10]

The transition paths of the leading leg are shown in Fig 14, Q2 is turned off to prepare for the zero voltage turn on of Q1. The current reflected from the secondary side charges C2 and discharges C1. During this transition the time required to charge C2 to Vin and discharge C1 from Vin to zero voltage is dependent on the load current. Since this time interval is very short, it can be assumed that the charge current is constant during the transition. Equations (1) and (2) can be used to calculate the voltage across C1 and C2, assuming C1=C2, (3) can be used to calculate the dead time needed to achieve zero voltage switching. Equation (3) is derived based on the assumption that during the duration of [t9~t10], the current is constant to charge charges C2 and discharges C1. I_{Lavg} in (1)-(3) represents the average current in L2 and can be calculated using (4).

The minimum dead time required to achieve ZVS turn-on. is calculated by using (3). The operation parameters are as follows: Vin=48V, Np:Ns=12:1,Np:Ns=10:1, C1=350pF at 30A load, Td=53ns for N=12 and 44.8ns for N=10.

$$V_{C1}(t) = V_{in} - \frac{I_{Lavg} t}{2C2N} \tag{1}$$

$$V_{C2}(t) = \frac{I_{Lavg} t}{2C1N} \tag{2}$$

$$t_{dead\_Q12} > \frac{2C1(V_{in})N}{I_{Lavg}} \tag{3}$$

$$I_{Lavg} = \frac{(I_o)}{4} \tag{4}$$

B. Lagging Legs, transition during [t7-t8] (Q2 Q4 Q6)

The transition paths of the lagging leg are shown in Fig 18. Initially, Q1 is turned off to prepare for the zero voltage turn on of Q2. If the voltage at point A can be discharged from V_{in} to 0, the body diode of Q2 will be turned on, in this case in order to achieve ZVS turn-on, Q2 must be turn-on before the current through the leakage inductance decreases to zero. The voltages across C1 and C2 can be calculated using (5)-(8) assuming C1=C2. The leakage current, $I_{Leakage}$ in (5) represent the current at the instant Q1 is turned off and can be estimated by using (10), where I_p is the primary side current. From (5) it is observed that in order to achieve ZVS, (9) must be satisfied.

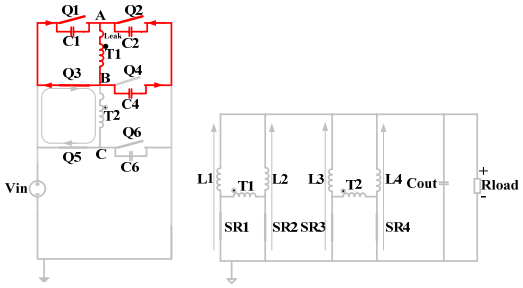

Fig 18 Lagging leg transition equivalent circuit

The minimum dead time of the lagging leg transition needed between Q1 and Q2 can be calculated by using (9) with V_{in}=48V, V_o=1V, C1=C2=350pF, $L_{Leakage}$=3uH. It is clear that it is much more difficult for the lagging leg to achieve zero voltage turn-on in comparison to the leading leg, and it seems that we need very big leakage inductor (3uH). Big leakage inductor will cause duty cycle loss and limit the operation frequency of the converter.

The calculated results: Td=35ns for N=12 and 28ns for N=10. So in the real circuit the lagging leg will be hard switching at most of the load range, since the leakage inductance required is very large, and the planar transformer used in this design has leakage inductance around 100nH. According to the calculation when leakage inductor=100nH ZVS turn on can not be achieved at full load for lagging leg.

$$V_{C2}(t) = Z_o I_{Leakage} \sin \omega t - (V_{in}) \tag{5}$$

$$I_p(t) = I_{Leakage} \cos \omega t \tag{6}$$

$$V_{C1}(t) = Z_o I_{Leakage} \sin \omega t \tag{7}$$

$$Z_o = \sqrt{L_{Leakage} / 2C_1}$$

$$\omega = 1/\sqrt{2L_{Leakage} C_1} \quad t_X = \frac{1}{\omega} \sin^{-1}\left(\frac{V_{in}}{Z_o}\right) \tag{8}$$

$$\begin{cases} Z_o I_{Leakage\min} > (V_{in}) \\ \frac{1}{\omega} \sin^{-1}\left(\frac{V_{in}}{Z_o I_{Leakage}}\right) < t_{dead\_Q34} < \frac{(I_{Leakage} L_{Leakage}) \cos \omega t_X}{(V_{in})} + t_X \end{cases} \tag{9}$$

$$I_{Leakage} = I_o / 4N \tag{10}$$

V. Loss Comparison Between Two Paralleled One-phase FB and The New Two-phase FB

In this section the losses of two paralleled FB and the new proposed two-phase FB will be compared. It will demonstrate that the new proposed two-phase FB will have better efficiency. In the comparison the conditions are: Vin=48V, Vo=1V, Iout=70A, Fs=1MHz, Np:Ns=12:1, primary side MOSFETs SI4580, SR IRF6619. The output inductor is 100nH.

A. Switching loss

The switching loss can be calculated using (11) and (12). In a real circuit, the switching loss may be larger due to parasitic components [11]-[15], but (11) and (12) can still be used to estimate the switching loss. In the new two-phase FB Q1, Q2 Q5 and Q6 will have the same current stress; Q3 and Q4 have higher current stress.

$$P_{on} = \frac{1}{2} f_s V_{ds} I_{PKon} t_r \quad (11)$$

$$P_{off} = \frac{1}{2} f_s V_{ds} I_{PKoff} t_f \quad (12)$$

Two-Phase FB	Q1,Q2, Q5,Q6	Q3	Q4	Q7,Q8
Ipkoff	1.78A	1.78A	3.54A	X
Ipkon	1.15A	1.15A	2.29A	X
Vds	48V	48V	48V	X
Fs	1MHz	1MHz	1MHz	X
Two One-Phase FB	Q1,Q2, Q5,Q6	Q3	Q4	Q7,Q8
Ipkoff	1.78A	1.78A	1.78A	1.78A
Ipkon	1.15A	1.15A	1.15A	1.15A
Vds	48V	48V	48V	48V
Fs	1MHz	1MHz	1MHz	1MHz

Table 1 Current stress comparison between two one-phase FB and two-phase FB

Table 1 lists the peak current stress comparison between two paralleled one-phase FBs and the two-phase FB (the circulating current is neglected in the calculation). Form the table it is noticed that the current stress of Q4 is doubled compared with other MOSFETs. For Q3 since Iq3=Iq2+Iq6, and Iq2 and Iq6 are 120 degree out of phase from each other, Q3 has the same peak current as Q1, Q2 Q5 Q6.

Solely considering the switching loss, the two-phase FB save one primary side MOSFETs compared with two one-phase FBs in parallel. Since the total switching loss of the two-phase FB is 7 times of the switching loss of Q1; for the two parallel one-phase FBs is 8 times the switching loss of Q1.

If only four MOSFETs at the primary side and four SRs for the rectifier stage are used, compared with two paralleled one-phase FBs no switching loss could be saved since the current stress of the MOSFETs at primary side would be doubled.

If we assume 1)Ton=10nS and Toff=15nS, 2) Lagging leg does not achieve ZVS 3) Leading legs can achieve ZVS and recovery 75% of the switching loss. The calculated results: Two-phase FB 5.77W, two paralleled FB 6.48W, therefore, 0.71W is saved.

B. Conduction loss

The conduction loss can be calculated using (13).Table 2 shows the RMS current comparison between two paralleled one-phase FBs and two-phase FB. Q4's RMS current is doubled compared with Q1. Q3's RMS current is between Q1 and Q4; this benefit is achieved by phase shifting current in Q2 and Q6 120 degree from each other.

$$P_{con} = I_{RMS} R_{on} \quad (13)$$

Two-Phase FB	Q1,Q2, Q5,Q6	Q3	Q4	Q7,Q8	SR
I_{RMS}	0.88A	1.24A	1.75A	X	21.4A
Two One-Phase FB	Q1,Q2 ,Q5,Q6	Q3	Q4	Q7,Q8	SR
I_{RMS}	0.88A	0.88A	0.88A	0.88A	21.4A

Table 2 RMS current comparison between two one-phase NFBs and two-phase NFB

Compared with two paralleled FB at the primary side the two-phase FB will have more conduction loss, at secondary side they will have the same conduction loss. The calculated total MOSFETs conduction loss: Two-phase FB 3.17W, two paralleled FB 3.143W.

C. Loss summary

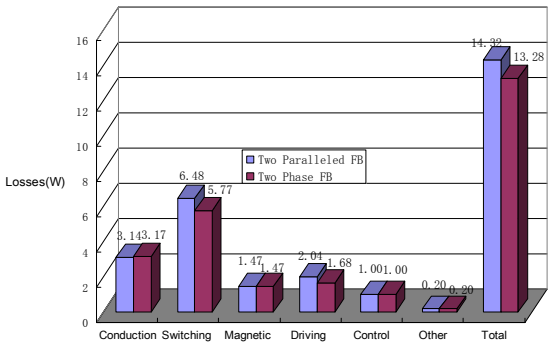

Fig 19 Losses breakdown comparison between the two-phase FB and two paralleled FB at 1MHz and 1V/70A load

The loss breakdown comparison between the two-phase FB and two paralleled FB at 1MHz switching frequency is shown in Fig 19, it is observed that the total loss is reduced form 14.32W(for two paralleled FB) to 13.28W (for two-phase FB), 1.04W loss is saved because of the fewer MOSFETs results in less gate loss and phase-shift control reduce the switching loss.

VI. Experimental Results

To verify the analysis in previous sections two prototypes were built on a 12 layers 2oz copper PCB, one with four output inductors, the other with three output inductors. Primary MOSFET is SI4850, four IRF6619s are used as synchronous MOSFETs.

Fig 20 illustrates the leading leg transition of Q5 at 50A,

1MHZ. It is observed that Vgs rises after Vds reduces to zero, and ZVS turn-on is achieved.

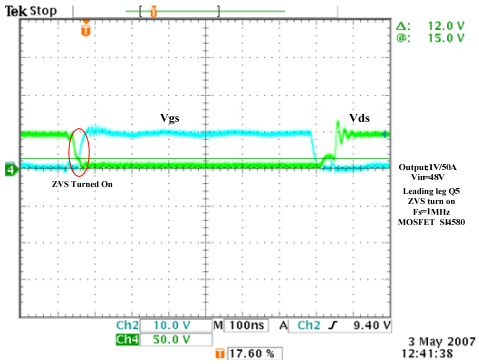

Fig 20 Zero voltage turned on of Leading Leg MOSFET Q5 at 50A

Fig 21 shows the switching transition of the lagging leg at 1V/65A, from the testing results we can see that lagging leg did not achieve ZVS turn on. The failure of ZVS turn-on occurs because at 48V input the input current is small which limit the energy stored in the leakage inductance. This is also proved the analysis in section IV.

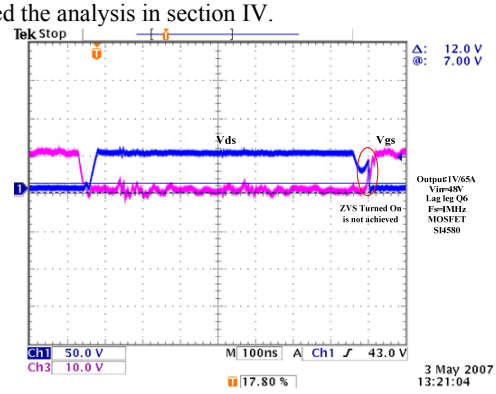

Fig 21 Zero voltage turned on of Lagging Leg MOSFET Q6 is not achieved

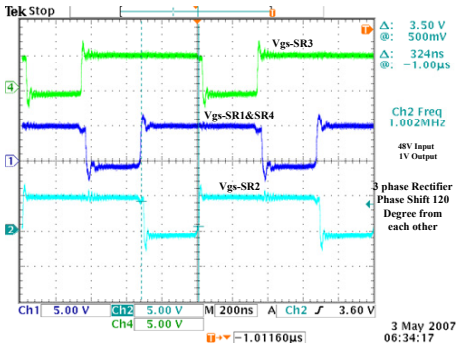

Fig 22 Gate driving signal of synchronous MOSFETs, each phase shift 120 degree.

Fig 22 shows the gate signal of the synchronous MOSFETs, each phase is 120 degree shifted from each other so the ripple current of the output inductor can cancel each other; therefore, small output inductor can be used to improve dynamic performance.

Fig 23 illustrates the synchronous MOSFETs turn-on and turn-off transition. From the waveform it is observed that during the turn-on transition SR will be turned on before it begins to conducts the current, and SR's body diode does not turn on during the turn-on transition.

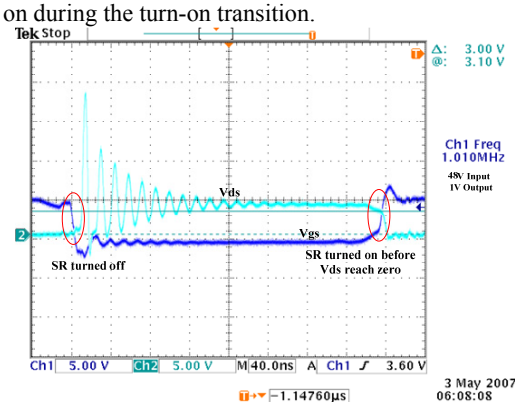

Fig 23 Synchronous MOSFET turn-on and turn-off transition

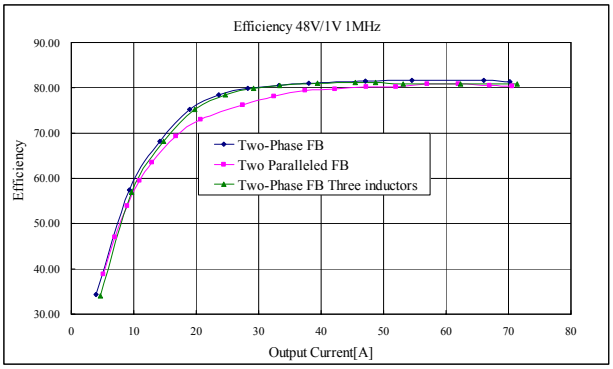

Fig 24 Measured efficiency of Two Phase Isolated Full Bridge at 1MHz switching frequency， compared with two parallel FB .

Fig 24 depicts the measured efficiency curve of the two-phase FB prototype operating at 1MHZ switching frequency, from 1V/10A till 1V/70A. From the testing result we can see that for the prototype with four output inductors 81.3% efficiency is achieved at full load compared with the two paralleled FB 80.4% around 1% improvement is achieved. At light load 20A around 4% improvement is achieved. This is because two-phase FB has fewer components at primary side and phase shift control results in less switching loss and gate loss. When the number of inductors are reduced from four to three at full load 1V/70A 80.8% is achieved, and efficiency is reduced by 0.5% because higher conduction loss from the output inductor.

Compared with the results of the one-phase FB with four

paralleled synchronous MOSFETs shown [1], at the same operation condition but with lower output voltage (reduce from 1.2V to 1V), only 0.4% efficiency is reduced (form 81.7% to 81.3%).

VII. CONCLUSION

Two new isolated two-phase full bridge topologies are proposed in this paper, one with four output inductors and one with three inductors, as shown in Fig 2 and Fig 3 respectively. The new topology save two MOSFETs at the primary side compared with two paralleled one-phase FB. The three legs in the new topology can phase shift 120 degree from each other, and ZVS turn-on can be achieved. In addition the number of inductor and synchronous can be reduced to three to further simplify the power train circuit.

The most significant advantages of the new topology is that compared with the two paralleled traditional full bridge topology, the two-phase full bridge can handle the same power but can achieve better efficiency with lower cost. And the advantages are summarized as below:

1) Components cost is reduced. At the primary side, two MOSFTEs are saved. At the secondary side, only three MOSFET drivers are needed to drive four SRs.
2) Better efficiency is achieved since fewer MOSFETs and phase shift control result in less switching loss and gate loss.
3) Current sharing is simplified due to the sharing leg (Q3, Q4) makes two power stages coupled with each other.
4) Compared with the single phase full bridge topology, a smaller output capacitor and inductor can be used to improve dynamic performance, since the two-phase FB can triple the frequency of the output ripple current. In addition, the output inductor current of the two-phase FB has a phase shift 120 degrees from each other, which also reduces the ripple current.
5) Compared with the current-tripler dc/dc converter proposed in [16] the new proposed topology reduces the power transformer from three to two.

To demonstrate the advantages of this topology, two VRM modules were built and tested at 48V input and 1V output, 70A load and 1MHz switching frequency and 81.3% efficiency is achieved at full load which is around 1% higher than the two paralleled one-phase FB. At light load 20A 4% improvement is achieved.

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