A Simple Analytical Switching Loss Model for Buck Voltage Regulators

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Abstract: **In this paper, a simple and accurate analytical switching loss model is proposed for high frequency synchronous buck voltage regulators. The proposed model uses simple equations to calculate the rise and fall times and uses piecewise linear approximations of the high side MOSFET voltage and current waveforms to allow quick and accurate calculation of switching loss in a synchronous buck voltage regulator. Effects of the common source inductance and other circuit parasitic inductances are included. Spice simulations are used to demonstrate the accuracy of the voltage source driver model operating in a 1MHz synchronous buck voltage regulator at 12V input, 1.3V output. Switching loss was estimated with the proposed model and measured with Spice for load current ranging from 10-30A, common source inductance ranging from 250-1000pH, voltage driver supply ranging from 6-12V.**

I. Introduction

In order to optimally design a high frequency switching converter, engineers and researchers begin their design by estimating the losses in a design file that is typically created using a spreadsheet, or other mathematical software. Device data sheet values and analytical models are used to calculate the losses. Using the loss models, many design parameters and components are compared to achieve a design with the optimal combination of efficiency and cost.

Analytical models are math based. Most often, piecewise linear turn on and turn off waveforms are used, or simplified equivalent circuits are used to derive switching loss equations. These methods yield closed form mathematical expressions that can be easily used to produce optimization curves within a design file, however the challenge is to improve accuracy while minimizing complexity. Most often, piecewise linear turn on and turn off waveforms are used, or simplified equivalent circuits are used to derive switching loss equations.

One of the most popular analytical models is the piecewise linear model presented in [1]. This model is referred to as the conventional model and is used as a benchmark later for comparison purposes with the proposed model. This model enables simple and rapid estimation of switching loss, however, the main drawback is that it neglects the switching loss dependences due to common source inductance and other circuit inductances. Typically, this model predicts that turn on and turn off loss are nearly similar in magnitude, however in a real converter operating at a high switching frequency, the model is highly inaccurate since turn off loss is much greater.

An analytical model is presented in [2]. This model is an extension of the model presented in [3], with the advantage that it provides accurate characterization of switching loss including common source inductance. The main drawback of the models in [2] and [3] is their complexity.

The synchronous buck remains the topology of choice for voltage regulators (VRs) in today's computers [4]-[7]. However, in order to properly model switching loss in a buck VR, a detailed understanding of the impact of MOSFET gate capacitance, common source inductance, other parasitic inductance and load current on switching loss is necessary. This is most easily accomplished through careful examination of waveforms through simulation and experiments, which are included in section II following the approach presented in [8].

In section III, a new switching loss model is proposed with the goal of maintaining the relative simplicity of the very popular conventional model in [1], while improving the accuracy for high frequency synchronous buck with parasitic circuit inductances, including common source inductance. In particular, the model predicts the large decrease in turn on loss and increase turn off loss that occurs as undesired circuit parasitic inductance increases. Model verification using Spice simulation is presented in section IV.

II. Impact of Parasitic Inductance and Load Current

A synchronous buck is illustrated in Fig. 1. In a synchronous buck VR, it is well known that the input voltage, load current and HS MOSFET gate-drain charge influence switching loss in the HS MOSFET. However, it is not well known that the inductances associated with the device packaging and PCB traces also contribute significantly to HS MOSFET switching loss. It is worth noting that with proper dead time, the SR switches with near zero switching loss.

The synchronous buck in Fig. 1 includes parasitic drain and source inductances for the high side (HS) MOSFET, M_1, and synchronous rectifier (SR) MOSFET, M_2. It can be assumed that the source inductances, L_{s1} and L_{s2} are common to their respective drive signals. Any other inductance in the source that is not common to the driver is assumed to be lumped with the drain inductances, L_{d1} and L_{d2}. These inductances have a significant impact on the switching loss behavior in high frequency synchronous buck voltage regulators.

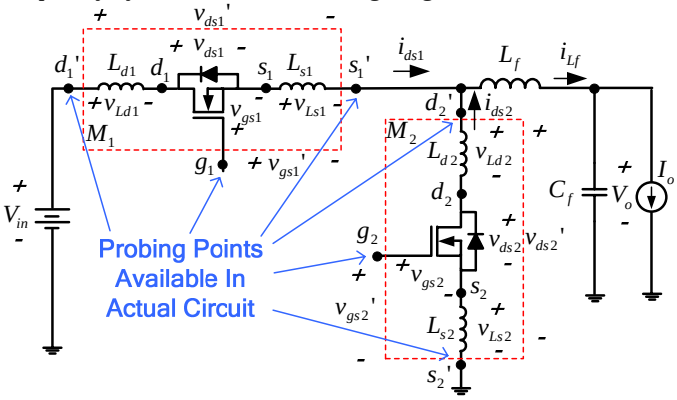

Fig. 1. Synchronous buck voltage regulator with parasitic inductances

During the switching transitions, the HS MOSFET operates in the saturation (linear) mode as a dependent current source simultaneously supporting the current through the device and voltage across it. At turn on and turn off, the gate-source

voltage, v_{gs1}, is held at the plateau voltage, V_{pl}, by the feedback mechanism provided by the voltage across the common source inductance, v_{Ls1}.

Using the circuit in Fig. 1, at turn on, as the HS MOSFET current increases, v_{Ls1} is positive in the direction noted, so this voltage subtracts from the V_{cc} voltage applied to the gate enabling $v_{gs1}=V_{pl}$ while the MOSFET operates in the saturation mode. At the same time, the four parasitic inductances provide a current snubbing effect, which virtually eliminates turn on switching loss enabling a near zero current switching (ZCS). During this transition, the rise time, t_r, is dictated by the gate driver's ability to charge the MOSFET gate capacitances (C_{iss} from V_{th} to V_{pl} and C_{gd} to V_{in}), which is the time for v_{ds1} to fall to zero. Then, it is assumed that this time is independent of the time it takes i_{ds1} to rise to its final value equal to the buck inductor current. i.e. after t_r, i_{ds1} can be less than the buck inductor current (I_o-Δi_{Lf}).

At turn off, as the HS MOSFET current decreases, v_{Ls1} is negative in the direction noted Fig. 1, so this voltage subtracts from the low impedance source voltage (ideally zero volts) applied to the gate enabling $v_{gs1}=V_{pl}$ while the MOSFET operates in the saturation mode. During this transition, the fall time, t_f, is the time for the HS MOSFET current to fall from the buck inductor current to zero. This time is dictated by both the gate driver's ability to discharge the MOSFET gate capacitances (C_{gd} from V_{in}, and C_{iss} from V_{pl} to V_{th}) and by the four parasitic inductances, which prolong the time for i_{ds1} to fall to zero by limiting the di_{ds}/dt.

As alluded to in the two paragraphs above, the MOSFET and trace parasitic inductances have vastly different effects at turn on and turn off. At turn on, the inductances provide a current snubbing effect, which decreases turn on switching loss. At turn off, the inductances increase the turn off loss by prolonging the fall time, t_f. In addition, as load current increases, fall time increases, so turn off losses increase proportionally to I_o^2 (proportional to I_o and $t_f(I_o)$). In contrast, at turn on, the load current magnitude has ideally no effect on the rise time. Therefore, in real circuits, turn off loss is much greater than turn on loss.

Another important point to note from Fig. 1 is that in a real circuit, the board mounted packaged inductances are distributed within the MOSFET devices. Therefore, when probing in the lab, one only has access to the external terminals, g_1, s_1' and d_1' for the HS MOSFET and g_2, s_2' and d_2' for the SR. However, the actual nodes that provide waveform information relevant to the switching loss are at the unavailable internal nodes s_1 and d_1 for the HS MOSFET. Using the plateau portion of the measured gate-source voltage, v_{gs1}' to determine the switching loss times is misleading since the induced voltage across L_{s1} is included. Probing v_{gs1}' in the lab, one would observe a negligible rise time at turn on, and a fall time less than one half of the actual t_f. The actual v_{gs1} waveform, which cannot be measured in a real circuit, more clearly illustrates the plateau portions in the rise and fall times.

Simulation waveforms are illustrated in Fig. 2 for a buck voltage regulator at 12V input, 30A load, 8V drive voltage and 1MHz switching frequency. Typical, parasitic inductance values for common package types are provided by the semiconductor manufacturers in application notes [9]-[10] and range from approximately 250pH-2nH, depending on the package type. Matched inductances of 500pH each for the four inductances were used in the simulation. The v_{gs1} (Actual) and v_{gs1}' (Measured; v_{gs1}',=v_{gs1}+v_{Ls1}) waveforms are included in Fig. 2 to demonstrate that measuring v_{gs1}' in the lab provides an inaccurate representation of the switching times.

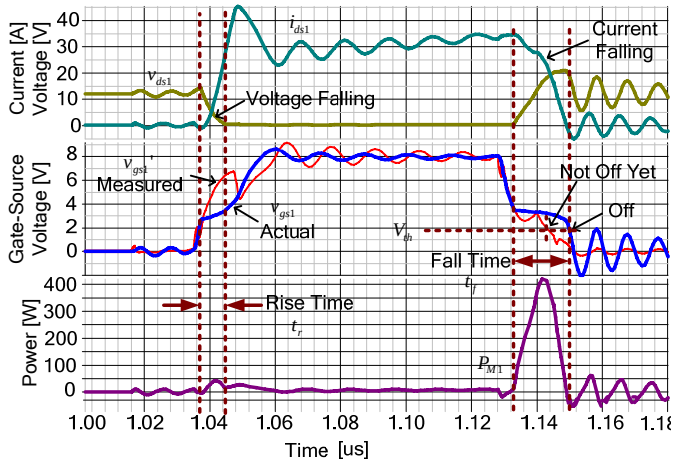

Fig. 2. Synchronous buck voltage regulator HS MOSFET waveforms (top: actual drain-source voltage, v_{ds1} and drain current, i_{ds1}; middle: measured gate-source voltage, v_{gs1}' and actual gate-source voltage (bold), v_{gs1}; bottom: HS MOSFET power, $v_{ds1}i_{ds1}$)

To demonstrate the effects of load current and common source inductance, experimental testing was done at a reduced frequency of 200kHz, with the source connection cut and a wire inserted in the common source path to measure the MOSFET current. Measurement waveforms are illustrated in Fig. 3, and Fig. 4, where the load current has been increased from 0A to 5A. With this method, the inductance of the wire (approximately 20nH) is much greater than the approximate total package inductance of 1nH, so the package inductance can be neglected allowing for measurement of v_{gs1} and v_{ds1}. It is noted that as load increases, the rise time remains nearly unchanged from 20ns to 22ns, but the fall time increases significantly from 48ns to 96ns. In addition, at a constant load current of 5A, as illustrated in Fig. 5, as L_{s1} increases with a longer 3 inch wire (approximately 30nH), t_r remains relatively unchanged from 22ns to 24ns, while t_f further increases from 96ns to 160ns.

From knowledge of the circuit operation and observation of the experimental results presented, three important observations and conclusions can be made:

1) In a practical synchronous buck voltage regulator, turn off loss is much greater than turn on loss since the circuit inductances provide a current snubbing effect, which decreases and virtually eliminates turn on switching loss, but increases the turn off loss by prolonging the t_f.
2) t_r, is dictated by the time for the voltage to fall to zero and is independent of the final value of the current. In addition, load current has negligible impact on rise time, while common source inductance has only a small impact, since as L_{s1} increases, the current di_{ds}/dt decreases.
3) t_f is dictated by the time for the current to fall to zero.

Load current, common source inductance and other circuit parasitic inductances (i.e. L_{d1}, L_{s2}, and L_{d2}) increase t_f.

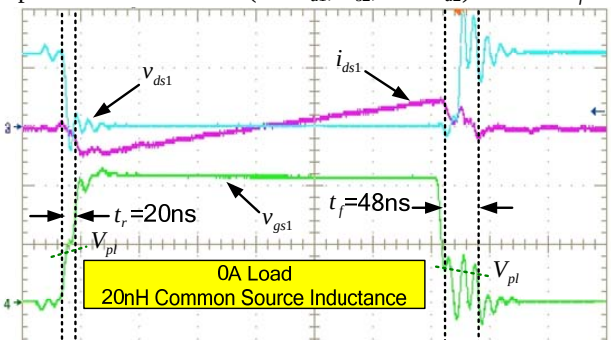

Fig. 3. Switching waveforms at 0A load and 20nH common source inductance (80ns/div; v_{ds1}: 10V/div; i_{ds1}: 5A/div; v_{gs1}: 5V/div)

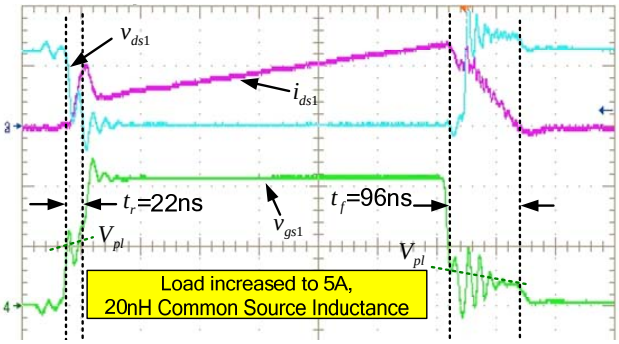

Fig. 4. Switching waveforms at 5A load and 20nH common source inductance (80ns/div; v_{ds1}: 10V/div; i_{ds1}: 5A/div; v_{gs1}: 5V/div)

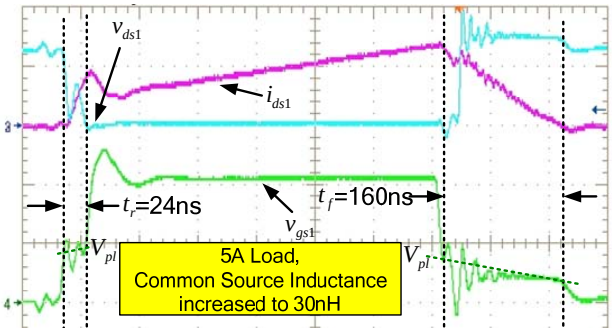

Fig. 5. Switching waveforms at 5A load with 30nH common source inductance (80ns/div; v_{ds1}: 10V/div; i_{ds1}: 5A/div; v_{gs1}: 5V/div)

III. Proposed Switching Loss Model

Typical switching waveforms for a synchronous buck VR are illustrated in Fig. 6. The proposed model uses the piecewise linear approximations (noted with thicker bold lines) of the switching waveforms in Fig. 6. Turn on switching loss occurs during t_r and turn off switching loss occurs during t_f. The key to the model is prediction of the turn on current, I_{on}, the rise and fall times, t_r and t_f, the reverse recovery current, I_{rr}, the magnitude of the rising current slope, $\Delta i_{ds}/\Delta t$, and the current drop, Δi_{1f}, when v_{ds1} rises to V_{in} at turn off. The goal of the proposed model is to predict the switching loss trends vs. load current, driver supply voltage, driver gate current and total circuit inductance in a simple manner.

The MOSFET parasitic capacitances are required in the model. They are estimated using the effective values [1] as follows in (1)-(5) using datasheet specification values for V_{ds_spec}, C_{rss_spec}, C_{oss_spec} and C_{iss_spec}.

$$C_{gd} = 2C_{rss\_spec}\sqrt{\frac{V_{ds\_spec}}{V_{in}}} \quad (1)$$

$$C_{oss} = 2C_{oss\_spec}\sqrt{\frac{V_{ds\_spec}}{V_{in}}} \quad (2)$$

$$C_{ds} = C_{oss} - C_{gd} \quad (3)$$

$$C_{iss} = C_{iss\_spec} \quad (4)$$

$$C_{gs} = C_{iss} - C_{gd} \quad (5)$$

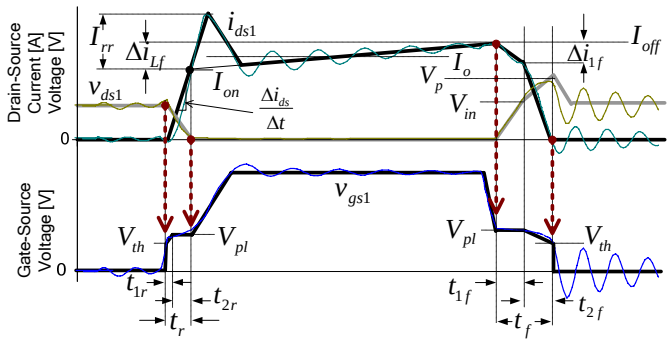

Fig. 6. Synchronous buck HS MOSFET waveforms with piecewise linear approximations of these waveforms in bold

A. Turn On Switching Loss Model

Using the piecewise linear geometry for the voltage and current waveforms at turn on in Fig. 7, the turn on loss is approximated using (6). During the rise time, the average HS switch voltage is $0.5V_{in}$, while the average current is $0.5I_{on}$. The linearized power loss in (6) is the product of the average voltage, average current, switching frequency and rise time. The two parameters that are key to accurate prediction of P_{on} are the current at turn on, I_{on} and the rise time, t_r.

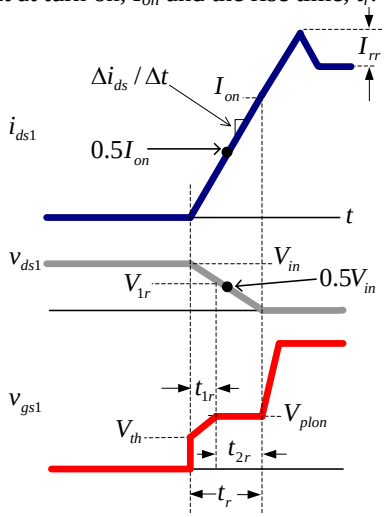

Fig. 7. Synchronous buck HS MOSFET waveforms at turn on with piecewise linear approximations

$$P_{on} = 0.25V_{in}I_{on}t_r f_s \quad (6)$$

As discussed in section II, the rise time, t_r, is dictated by the gate driver's ability to charge the MOSFET gate capacitances, which is the time for v_{ds1} to fall to zero. This time is assumed independent of the time it takes i_{ds1} to rise to its final value. Under this assumption, the rise time consists of two intervals, t_{1r} and t_{2r} as given by (7).

$$t_r = t_{1r} + t_{2r} \tag{7}$$

The HS MOSFET equivalent circuit during t_{1r} is given in Fig. 8. The gate resistance, R_r, represents the total series resistance in the gate drive path, i.e. R_r=R_{hi}+R_{ext}+R_g, where R_{hi} is the resistance of the driver switch, R_{ext} is any external resistance and R_g represents the internal gate resistance.

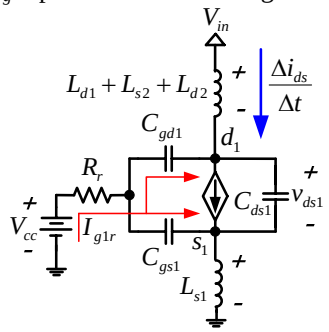

Fig. 8. Synchronous buck HS MOSFET equivalent circuit during t_{1r}

During t_{1r}, the C_{gs1} capacitance is charged from V_{th} to V_{plon}, while the gate side of C_{gd1} charges from V_{th} to V_{plon} and the drain side of the C_{gd1} capacitance discharges from V_{in} to V_{1r}. Therefore, the change in voltage across C_{gd1} during t_{1r} is [(V_{in}-V_{1r})+(V_{plon}-V_{th})]. Then, t_{1r} is given by (8), assuming an average gate charging current I_{g1r}, where V_{plon} is given by (9), and ΔV_{gsr}=V_{plon}-V_{th}.

$$t_{1r} = \frac{C_{gs1}\Delta V_{gsr} + C_{gd1}[\Delta V_{gsr} + (V_{in} - V_{1r})]}{I_{g1r}} \tag{8}$$

$$V_{plon} = V_{th} + \frac{I_o - 0.5\Delta i_{Lf}}{g_{fs}} \tag{9}$$

The drain-source voltage during t_{1r} is given by (10), where L_{loop}= L_{s1}+L_{d1}+L_{s2}+L_{d2}.

$$v_{ds1} = V_{in} - L_{loop}\frac{\mathrm{d}i_{ds1}}{\mathrm{d}t} \tag{10}$$

Neglecting the gate current through the inductances, the rate of change of current in (10) is given by (11), which is approximated by (13) using (12) and the piecewise linear approximation of the gate-source voltage waveform during t_{1r}.

$$\frac{\mathrm{d}i_{ds1}}{\mathrm{d}t} = \frac{\mathrm{d}g_{fs}(v_{gs1} - V_{th})}{\mathrm{d}t} = \frac{g_{fs}\mathrm{d}v_{gs1}}{\mathrm{d}t} \tag{11}$$

$$\frac{\mathrm{d}i_{ds}}{\mathrm{d}t} \approx \frac{\Delta i_{ds}}{\Delta t} \tag{12}$$

$$\frac{\Delta i_{ds}}{\Delta t} = \frac{g_{fs}\Delta v_{gs1}}{\Delta t} = \frac{g_{fs}\Delta V_{gsr}}{t_{1r}} \tag{13}$$

Using (10)-(13), V_{1r} is given by (14).

$$V_{1r} = V_{in} - L_{loop}\frac{g_{fs}\Delta V_{gsr}}{t_{1r}} \tag{14}$$

The driver equivalent circuit during t_{1r} is illustrated in Fig. 8. During this time interval, it is assumed that v_{gs1} is the average value of the plateau, V_{plon}, and threshold voltages, V_{th}. In addition, in the proposed model, the slope of the drain current is assumed constant; therefore the voltage v_{Ls1}=$L_{s1}\Delta i_{ds}/\Delta t$ is constant, so the L_{s1} inductance is replaced by an ideal voltage source in the drive circuit. The gate current is given by (15).

$$I_{g1r} = \frac{V_{cc} - 0.5(V_{plon} + V_{th}) - L_{s1}\frac{\Delta i_{ds}}{\Delta t}}{R_r} \tag{15}$$

Using (8) and (13)-(15), solving for t_{1r} yields (16), where V_{gs1r}=0.5(V_{plon}+V_{th}).

$$t_r = t_{1ra} + t_{1rb}$$
$$t_{1ra} = \frac{\Delta V_{gsr}(L_{s1}g_{fs} + R_r C_{iss1})}{2V_{gs1r}} \tag{16}$$
$$t_{1rb} = \frac{\sqrt{[\Delta V_{gsr}(L_{s1}g_{fs} + R_r C_{iss1})]^2 + 4\Delta V_{gsr}(V_{cc} - V_{gs1r})R_r C_{rss1\_spec} L_{loop} g_{fs}}}{2V_{gs1r}}$$

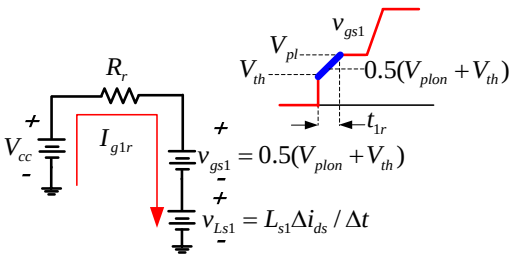

Fig. 9. Driver equivalent circuit during t_{1r}

During t_{2r}, the gate voltage of the C_{gd1} capacitance remains constant at V_{plon}, while the drain of C_{gd1} is discharged by current I_{g2r}, allowing t_{2r} to be given by (17).

$$t_{2r} = \frac{C_{gd1}V_{1r}}{I_{g2r}} \tag{17}$$

The driver equivalent circuit during t_{2r} is illustrated in Fig. 9. Due to the assumed constant $\Delta i_{ds}/\Delta t$, the L_{s1} inductance is replaced by an ideal voltage source. Under these assumptions, the gate current is given by (18).

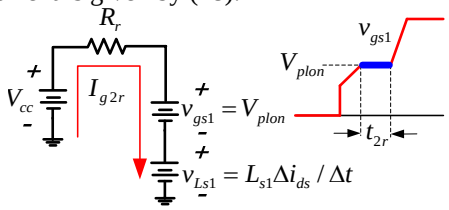

Fig. 10. Driver equivalent circuit during t_{2r}

$$I_{g2r} = \frac{V_{cc} - V_{plon} - L_{s1}\frac{\Delta i_{ds}}{\Delta t}}{R_r} \tag{18}$$

Using (13),(14),(16),(17) and (18), solving for t_{2r} yields (19).

$$t_{2r} = \frac{R_r C_{gd1}\left(V_{in} - L_{loop}g_{fs}\frac{\Delta V_{gsr}}{t_{1r}}\right)}{V_{cc} - V_{plon} - L_{s1}g_{fs}\frac{\Delta V_{gsr}}{t_{1r}}} \tag{19}$$

The final step to determine the turn on loss is to estimate the current I_{on} at the end of t_r. Depending on the load current and parasitic inductances, I_{on} can require calculation of the reverse recovery current, I_{rr}. The waveform in Fig. 11 is used to estimate I_{rr}. When the HS MOSFET turns on, the SR body diode cannot reverse block, so the SR current goes negative and the HS current spikes by the same magnitude. The total reverse recovery time is t_{rr}. The rising slope magnitude is $\Delta i_{ds}/\Delta t$ and the reverse recovery charge is Q_{rr}, which represents the shaded area as given by (20). Using the geometry, the reverse recovery current as a function of t_{rr} is given by (21). Then, eliminating t_{rr} from (20) and (21), (23) is derived, which represents I_{rr} as a function of Q_{rr} and the known slope. In addition, since reverse recovery charge

increases with load current, Q_{rr} is approximated using (22), where Q_{rr_spec} and I_{rr_spec} are the datasheet specification values.

$$Q_{rr} = \frac{1}{2} I_{rr} t_{rr} \tag{20}$$

$$I_{rr} = \frac{\Delta I_{ds}}{\Delta t} \frac{1}{2} t_{rr} \tag{21}$$

$$Q_{rr} = \frac{Q_{rr\_spec}}{I_{rr\_spec}} I_o \tag{22}$$

$$I_{rr} = \sqrt{\frac{\Delta I_{ds}}{\Delta t} Q_{rr}} \tag{23}$$

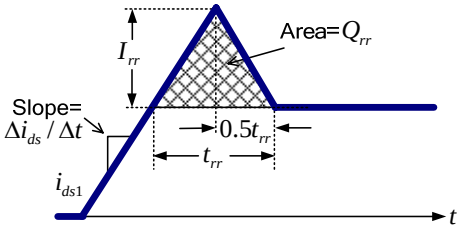

Fig. 11. Synchronous buck HS MOSFET current waveform approximation during reverse recovery at turn on

Since the rise time is dictated by the time for the HS MOSFET voltage, v_{ds1}, to fall to zero, the current at the end of t_r can be at any value equal to, or less than the inductor current plus the reverse recovery current (i.e. I_{on} is not necessarily equal to the inductor current, as in the conventional model [1], or the inductor current plus the reverse recovery current). Therefore, the current at the end of tr is give by (24).

$$\begin{aligned} I_{on} &= \frac{\Delta i_{ds}}{\Delta t} t_r \quad \text{if} \quad \frac{\Delta i_{ds}}{\Delta t} t_r < I_o - 0.5\Delta i_{Lf} + I_{rr} \\ &= I_o - 0.5\Delta i_{Lf} + I_{rr} \quad \text{otherwise} \end{aligned} \tag{24}$$

B. Turn Off Switching Loss Model

Using the piecewise linear geometry for the voltage and current waveforms at turn off in Fig. 12, the turn off loss is approximated using (25), which consists of two intervals with different falling current slopes during t_{1f} and t_{2f}. The first component of the power loss is during t_{1f}. During t_{1f}, the average HS switch voltage is $(1/2)V_{in}$, while the average current is $[I_{off}\text{-}(1/2)\Delta i_{1f}]$. In the second interval, t_{2f}, the average HS switch voltage is $(1/2)(V_{in}+V_p)$, while the average current is $(1/2)(I_{off}\text{-}\Delta i_{1f})$. The linearized power loss in (25) is the sum of the power in the two intervals consisting of the product of the average voltage, average current, switching frequency and fall time interval.

$$P_{off} = 0.5V_{in}(I_{off} - 0.5\Delta i_{1f})t_{1f} f_s + 0.25(V_{in} + V_p)(I_{off} - \Delta i_{1f})t_{2f} f_s \tag{25}$$

The parameters that are key to accurate prediction of the turn off loss are the HS MOSFET current at turn off, I_{off}, the value of the current drop, Δi_{1f} during the first falling slope interval t_{1f}, and the duration of the second interval t_{2f} and the peak overshoot voltage of v_{ds1}, V_p. The turn off current is the load current, I_o, plus half of the filter inductor peak-to-peak ripple current, Δi_{Lf}, as:

$$I_{off} = I_o + 0.5\Delta i_{Lf} \tag{26}$$

The turn off loss estimated using (25) is a function of the fall time, t_f. The fall time occurs for the duration of the current falling from I_{off} to zero. It is a function of the driver capability to discharge C_{gd1} and C_{iss}, but in addition, it is a function of circuit parasitic inductances which limit the falling time. It consists of two components, t_{1f} and t_{2f} as given by (27). t_{1f} is the time required to discharge the C_{gd1} capacitance by gate current I_{g1f} as given by (28).

$$t_f = t_{1f} + t_{2f} \tag{27}$$

$$t_{1f} = \frac{C_{gd1} V_{in}}{I_{g1f}} \tag{28}$$

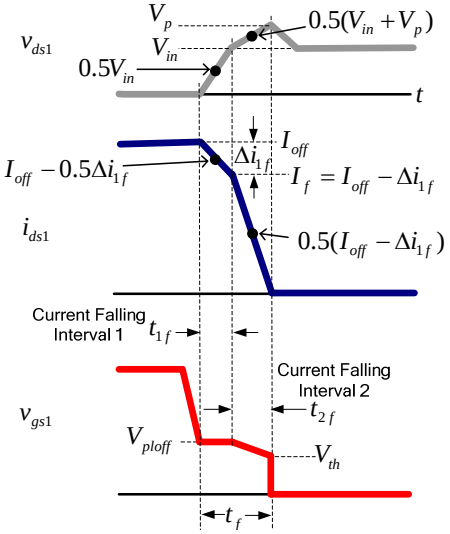

Fig. 12. Synchronous buck HS MOSFET waveforms at turn off with piecewise linear approximations

The driver equivalent circuit during t_{1f} is illustrated in Fig. 13. During this time interval, it is assumed that v_{gs1} remains constant at the plateau, V_{ploff}. As above, the L_{s1} inductance is replaced by an ideal voltage source; however the current slope during this interval is approximated as $\Delta i_{1f}/t_{1f}$. Under these assumptions, the gate current is easily derived as given by (29) where $R_f=R_{lo}+R_{ext}+R_g$, and V_{ploff} is given by (30).

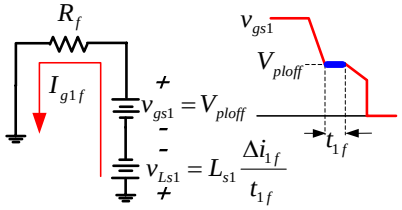

Fig. 13. Driver equivalent circuit during t_{1f}

$$I_{g1f} = \frac{V_{plon} - L_{s1} \frac{\Delta i_{1f}}{t_{1f}}}{R_f} \tag{29}$$

$$V_{plon} = V_{th} + \frac{I_o + 0.5\Delta i_{Lf}}{g_{fs}} \tag{30}$$

The fall time, t_{1f}, during this interval is given by (31) using (28) and (29),

$$t_{1f} = \frac{C_{gd1} V_{in} R_f}{V_{ploff} - L_{s1} \frac{\Delta i_{1f}}{t_{1f}}} \tag{31}$$

In (31), the current drop, Δi_{1f} is unknown, so we cannot solve for t_{1f}. In order to estimate Δi_{1f}, we use the synchronous buck equivalent circuit given in Fig. 14. As previously stated, during t_{1f}, the voltage across the HS switch rises linearly from

zero to V_{in}. Additionally, the voltage across the synchronous rectifier drops from V_{in} to zero as the C_{ds2} and C_{gd2} capacitors discharge into the d_2 node. During this interval, the current decrease in i_{ds1} is equal to the increase in current through C_{gd2} and C_{ds2}. Neglecting the drive circuits, the current drop of Δi_{1f} is estimated using the increase in discharging current in C_{gd2} and C_{ds2} as given by (32).

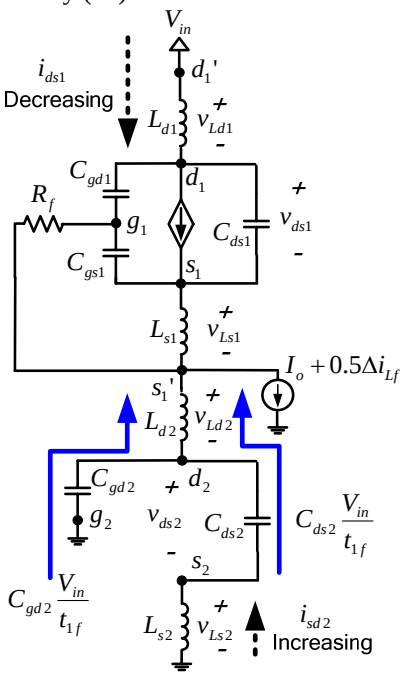

Fig. 14. Synchronous buck equivalent circuit during turn off during t_{1f}

$$\Delta i_{1f} = (C_{gd2} + C_{ds2})\frac{V_{in}}{t_{1f}} \tag{32}$$

Using (31) and (32), solving for t_{1f} yields (33).

$$t_{1f} = \frac{C_{gd1}V_{in}R_f + \sqrt{(C_{gd1}V_{in}R_f)^2 + 4V_{ploff}L_{s1}V_{in}(C_{gd2}+C_{ds2})}}{2V_{ploff}} \tag{33}$$

During t_{2f}, the C_{gs1} capacitance is discharged from the plateau voltage to the threshold, while the drain side of the C_{gd1} capacitance charges from V_{in} to V_p and the gate side of C_{gd1} discharges from V_{ploff} to V_{th}. Therefore, the change in voltage across C_{gd1} during t_{2f} is $[(V_p\text{-}V_{in})+(V_{ploff}\text{-}V_{th})]$. Then, t_{2f} is given by (34), where $\Delta V_{gsf}=V_{ploff}\text{-}V_{th}$.

$$t_{2f} = \frac{C_{gs1}\Delta V_{gsf} + C_{gd1}[(V_p - V_{in}) + \Delta V_{gsf}]}{I_{g2f}} \tag{34}$$

The drain-source voltage during t_{2f} is given by (35), where $L_{loop}= L_{s1}+L_{d1}+L_{s2}+L_{d2}$.

$$v_{ds} = V_{in} + L_{loop}\frac{di_{ds1}}{dt} \tag{35}$$

Following the approach of the approximations made in (11) and (12), the peak overshoot voltage, V_p is given by (36).

$$V_p = V_{in} + L_{loop}\frac{g_{fs}\Delta V_{gsf}}{t_{2f}} \tag{36}$$

The driver equivalent circuit during t_{2f} is illustrated in Fig. 16. During this time interval, it is assumed that v_{gs1} is the average value of the plateau, V_{ploff}, and threshold voltages, V_{th}. As above, the L_{s1} inductance is replaced by an ideal voltage source, where the di_{ds}/dt is assumed constant at I_f/t_{2f} and $I_f=I_{off}$-Δi_{1f}. Under these assumptions, the gate current is given by (37).

$$I_{g2f} = \frac{\frac{1}{2}(V_{pl}+V_{th}) - L_{s1}\frac{I_f}{t_{2f}}}{R_f} \tag{37}$$

Using (34), (36) and (37), solving for t_{2f} yields (38), where $V_{gs2f}=0.5(V_{ploff}+V_{th})$.

$$\begin{aligned} t_{2f} &= t_{2fa} + t_{2fb} \\ t_{2fa} &= \frac{L_{s1}I_f + \Delta V_{gs2f}R_fC_{iss1}}{2V_{gs2f}} \\ t_{2fb} &= \frac{\sqrt{[L_{s1}I_f + \Delta V_{gs2f}R_fC_{iss1}]^2 + 4\Delta V_{gs2f}V_{gs2f}R_fC_{gd1}L_{loop}g_{fs}}}{2V_{gs2f}} \end{aligned} \tag{38}$$

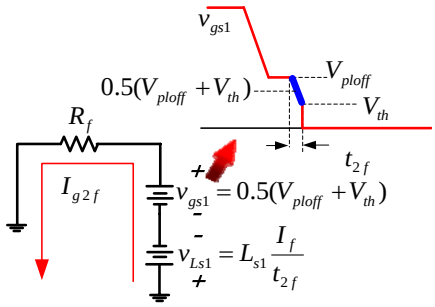

Fig. 15. Driver equivalent circuit during t_{2f}

IV. Model Verification

The analytical switching loss model with a voltage source drive was compared to SIMetrix Spice simulation and the conventional model in [1]. Results were calculated at 12V input, 1MHz switching frequency, and 10A peak-to-peak inductor ripple (100nH), R_{hi}=2Ω, R_{lo}=2Ω, R_g=1.5Ω, R_{ext}=0Ω. Results are included in the following sub-sections for both models. MOSFET parameters: Si7860DP HS and Si7336ADP SR; V_{th}=2V, V_{ds_spec1}=15V, C_{rss_spec1}=175pF, C_{oss_spec1}=500pF, C_{iss_spec1}=1800pF (model).

Curves of total switching loss vs. common source inductance (assuming matched inductances; i.e. L_{s1}=L_{d1}=L_{s2}=L_{d2}) for the proposed model, Spice simulation and the conventional model are given in Fig. 16. The proposed model follows the trends of the Spice simulation results very well. The accuracy of the proposed model total switching loss is within 0.5W. In Fig. 16, it is noted that the conventional model does a very poor job predicting the total switching loss as total circuit inductance increases. In particular, at 1000pH, the conventional model predicts 1.5W loss, while the Spice results indicate total switching loss of 3.4W – a difference of 1.9W.

Curves of total switching loss vs. load current for the proposed model, Spice simulation and the conventional model are given in Fig. 17. The proposed model follows the trends of the Spice simulation results very well. The accuracy of the proposed model total switching loss is within 0.5W. In Fig. 17, it is noted that the conventional model does a very poor job predicting the total switching loss as the load current increases. In particular, at 30A, the conventional model predicts 2.2W loss, while the Spice results indicate total switching loss of 4.2W – a difference of 2.0W.

Curves of total switching loss vs. driver supply voltage for the proposed model, Spice simulation and the conventional

model are given in Fig. 18. The proposed model follows the trends of the Spice simulation results very well. The accuracy of the proposed model total switching loss is within 0.1W.

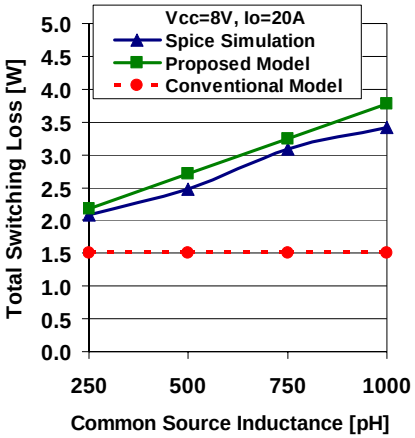

Fig. 16. Total switching loss at 1MHz, 12V input vs. common source circuit inductance (V_{cc}=8V, I_o=20A)

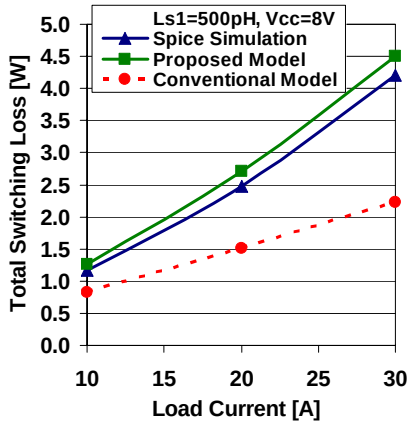

Fig. 17. Total switching loss at 1MHz, 12V input vs. load current (V_{cc}=8V, L_{s1}=500pH)

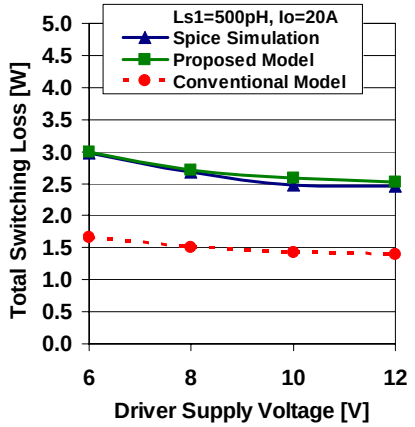

Fig. 18. Total switching loss at 1MHz, 12V input vs. driver supply voltage (L_{s1}=500pH, I_o=20A)

V. Conclusions

The switching loss characteristics and behavior in a high frequency synchronous buck VR have been reviewed. Following the demonstrated switching loss characteristics, a new simple and practical analytical switching loss model has been proposed for voltage source drivers. The model quickly and accurately predicts the switching loss in a high frequency synchronous buck voltage regulator. The model uses piecewise linear approximations of the actual v_{ds1} and i_{ds1} switching waveforms. The average value of the piecewise waveforms are then used to provide expressions for the turn on and turn off loss including the effects of common source inductance and other parasitic inductances.

To verify the proposed model, it was compared to Spice simulation results. It was demonstrated that the proposed model follows the trends in turn on and turn off switching loss for variations in load current, driver supply voltage and total circuit inductance. The accuracy of the proposed voltage source drive model was demonstrated to be within 0.5W for calculation of the total switching loss.

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