# A New Current-Source Gate Driver for a Buck Voltage Regulator

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***Abstract*- A new current-source gate drive circuit is proposed for a synchronous buck voltage regulator (VR). The proposed driver can drive two MOSFETs independently with different drive currents for optimal design. Furthermore, the new drive circuit can achieve 1) significant switching loss reduction; 2) gate energy recovery; 3) reduced body diode losses and reverse recovery losses; 4) ZVS of all the drive switches. The improved driver using integrated inductors is also presented for a buck VR to reduce the number of magnetic cores and the core loss. The experimental results prove that a significant efficiency improvement has been achieved. At 1.5V output, the new driver improves the efficiency from 84% using a conventional driver to 87.3% (an improvement of 3.3%) at 20A, and at 30A, from 79.4% to 82.8% (an improvement of 3.4%). Overall, the new driver approach is very attractive from the standpoints of both performance and cost-effectiveness.**

## I. INTRODUCTION

In recent years, MHz voltage regulators (VRs) show significant advantages over the conventional hundreds of KHz VRs in terms of cost, power density and dynamic response etc [1]-[4]. The multi-phase synchronous buck converter is used nearly exclusively as VRs to power microprocessors due to its simplicity and low component count.

However, an increase in switching frequency could lead to poor efficiency due to excessive switching loss and gate drive loss. More importantly, it has been noticed that with a conventional voltage driver, the parasitic inductance, especially, the common source inductance has a serious propagation effect during the switching transition and thus results in high switching loss in a 1-MHz synchronous buck VR [5].

One of the interesting topics of VR technologies is resonant gate drive technique, which is originally been proposed with the objective of recovering gate energy lost in a conventional gate driver. The resonant driver in [6] features simplicity and low circulating. However, the disadvantage is that the power MOSFET gate is not actively clamped high or low, which results in lower noise immunity. The resonant drivers using a coupled inductor [7] and using a transformer [8] are able to drive two MOSFETs. Nevertheless, the leakage inductance becomes a big concern at MHz frequency. A full-bridge topology drive circuit with one inductor is proposed to drive two ground-sharing MOSFETs in a 1MHz Boost converter in [9]. An assessment of resonant drive techniques for use in low power dc/dc converters is presented in [10] and the mathematical model is built to estimate the power loss of the drive circuit in [11]. Unfortunately, all these investigations are generally emphasizing gate energy savings by the resonant driver and concentrating on the drive topologies, but ignore the potential switching loss savings that are much more dominant in a MHz buck VR.

In [12]-[13], it was noted that the resonant gate driver can also reduce the switching transition time and switching loss significantly due to the parasitics by a constant drive current. Actually, these gate drivers can be recognized as current-source drivers (CSDs). An analytical switching loss model with the current-source driver for the purpose of the optimal design was developed due to the parasitic inductance in [16]. Particularly, in Fig. 1, the current-source driver for a buck VR presented in [12]-[13] has been reported to achieve a significant efficiency improvement over the conventional voltage driver at the switching frequency of 1MHz.

However, carefully investigating the equivalent circuits of operation in [12], it should be pointed that this driver circuit of Fig. 1 has several drawbacks: (1) in a buck VR, high drive current is desired for the control MOSFET to ensure the fast switching speed and reduce the switching loss while low drive current is desired for the synchronous MOSFET to achieve high efficiency of gate energy recovery. Therefore, it is very beneficial to have different gate drive currents for optimal design. But, this drive circuit can only provide identical drive currents for the two different MOSFETs; (2) due to the reverse recovery of the body diode, the switching node has severe oscillation as shown in Fig. 2, however, this switching node is actually in series with the level-shift capacitor of the drive circuit, which makes the circuit very sensitive to the reverse recovery noise in practical applications; (3) the resonant inductor current flows through the control MOSFET and synchronous MOSFET, which causes additional conduction losses; (4) to improve the light load efficiency, the switching frequency may change and the converter may operate under burst mode. It is difficult to achieve this feature by this drive topology.

In order to solve the above problems and improve the driver's performance, an improved current-source gate driver is proposed in this paper.

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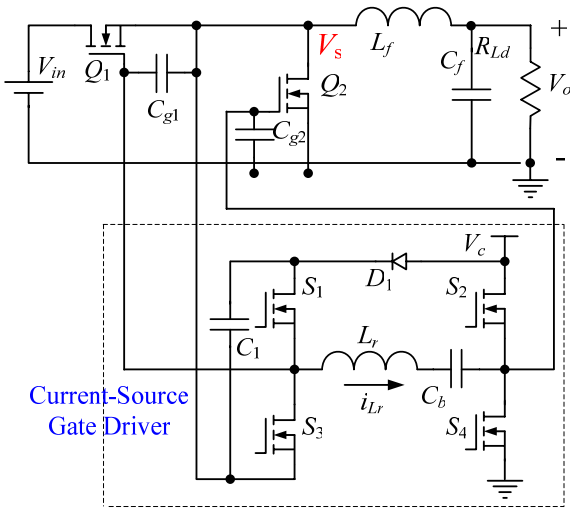



Fig. 1 Buck VR with current-source gate drive circuit

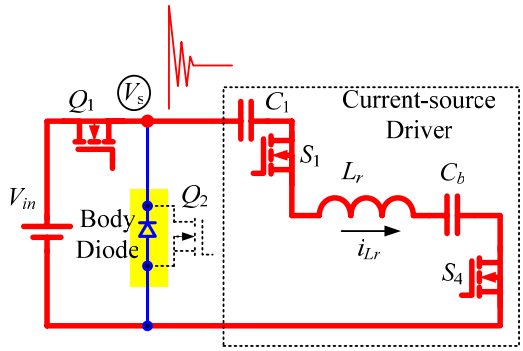



Fig. 2 Equivalent circuit during switching transition

## II. Proposed New Current-Source Gate Driver

One objective of the proposed current-source driver is to achieve the independent drive control of the control MOSFET and the synchronous MOSFET for different optimal design. For the control MOSFET, the optimal design involves a tradeoff between switching loss reduction and drive circuit loss; while for the synchronous rectifier MOSFET, the optimal design involves a tradeoff between body diode conduction loss and drive circuit loss. Moreover, the gate drive current should not flows through the main power MOSFET.

All the above features can be achieved by the proposed new circuit in Fig. 3. $Q_1$ is the control MOSFET and $Q_2$ is the synchronous MOSFET. $C_{g1}$ and $C_{g2}$ are the gate-source capacitors of $Q_1$ and $Q_2$ respectively. Fig. 4 gives the key waveforms.

### A. Principle of Operation

Basically, there are two sets of the drive circuit (#1 and #2) and each of them has the structure of half-bridge topology, consisting of $S_1$&$S_2$ and $S_3$&$S_4$ respectively. With the asymmetrical control, all the drive switches can achieve zero-voltage-switching (ZVS). Drive #1 can also be regarded as a level-shift version of drive #2. $V_{c1}$ and $V_{c2}$ are the drive voltages and they could use the same drive voltage. The diode $D_f$ provides the path to charge $C_f$ to the voltage of the drive voltage $V_{c2}$. $C_{b1}$ and $C_{b2}$ are the blocking capacitors. $S_1$ and $S_2$ are switched out of phase with complimentary control to drive $Q_1$, while $S_3$ and $S_4$ are switched out of phase with complimentary control to drive $Q_2$.

The switching transitions of charging and discharging $C_{g1}$ and $C_{g2}$ are during the interval of $[t_0, t_2]$ and $[t_3, t_5]$. The peak currents $i_{G\_Q1}$ and $i_{G\_Q2}$ during $[t_0, t_2]$ and $[t_3, t_5]$ are constant during switching transition as seen in Fig. 4, which ensure fast charging and discharging of MOSFET gate, including miller capacitor of $Q_1$.

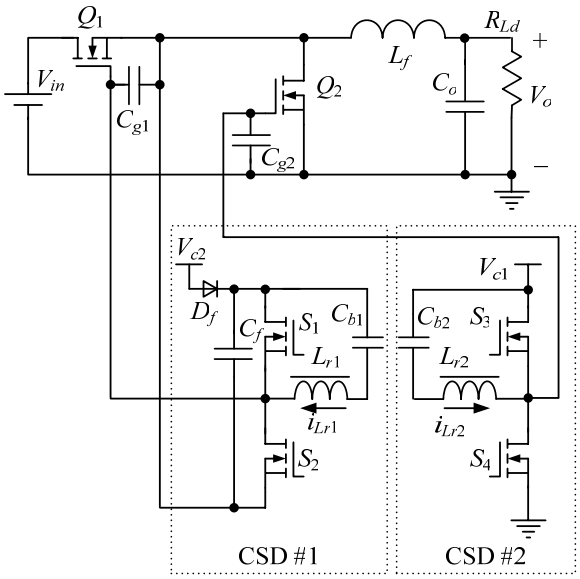



Fig. 3 Buck VR with proposed current-source driver

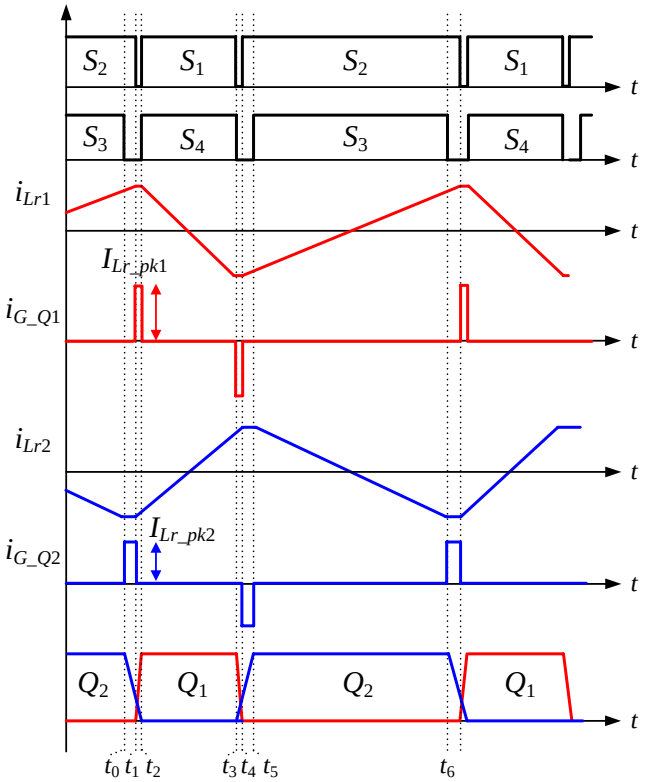



Fig. 4 Key waveforms of the new drive circuit

There are six switching modes in a switching period and the equivalent circuits are given in Fig. 5 accordingly. $D_1$-$D_4$ are the body diodes and $C_1$-$C_4$ are the intrinsic capacitors of $S_1$-$S_4$ respectively.

1) Mode 1 [$t_0$, $t_1$] [Fig. 5(a)]: Prior to $t_0$, $S_2$ and $S_3$ conduct and the inductor current $i_{Lr1}$ increases in the positive direction while $i_{Lr2}$ increases in the negative direction. $Q_2$ is on. At $t_0$, $S_3$ turns off. $i_{Lr2}$ charges $C_3$ and discharges $C_4$ plus the input capacitor $C_{gs2}$ simultaneously. Due to $C_3$ and $C_4$, $S_3$ is zero-voltage turn-off. The voltage of $C_2$ rises linearly and the voltage of $C_4$ decays linearly.

2) Mode 2 [$t_1$, $t_2$] [Fig. 5(b)]: At $t_1$, $v_{c3}$ rises to $V_{c1}$ and $v_{c4}$ decays to zero. The body diode $D_4$ conducts and $S_4$ turns on under zero-voltage condition. The gate-to-source voltage of $Q_2$ is clamped to ground through $S_4$. At $t_1$, $S_2$ turns off. $i_{Lr1}$ charges $C_2$ plus the input capacitor $C_{gs1}$ and discharges $C_1$ simultaneously. Due to $C_1$ and $C_2$, $S_2$ is zero-voltage turn-off. The voltage of $C_2$ rises linearly and the voltage of $C_1$ decays linearly.

3) Mode 3 [$t_2$, $t_3$] [Fig. 5(c)]: At $t_2$, $v_{c2}$ rises to $V_{c2}$ and $v_{c1}$ decays to zero. The body diode $D_1$ conducts and $S_1$ turns on under zero-voltage condition. The gate-to-source voltage of $Q_1$ is clamped to $V_{c2}$ through $S_1$. $i_{Lr1}$ and $i_{Lr2}$ both decrease.

4) Mode 4 [$t_3$, $t_4$] [Fig. 5(d)]: Before $t_3$, $i_{Lr1}$ and $i_{Lr1}$ changed polarity respectively. At $t_3$, $S_4$ and $S_1$ turns off. $i_{Lr2}$ charges $C_4$ plus $C_{gs2}$ and discharges $C_3$ simultaneously. Due to $C_3$ and $C_4$, $S_4$ is zero-voltage turn-off. The voltage of $C_4$ rises linearly and the voltage of $C_3$ decays linearly. $i_{Lr1}$ charges $C_1$ and discharges $C_3$ plus $C_{gs2}$ simultaneously. Due to $C_1$ and $C_2$, $S_1$ is zero-voltage turn-off.

5) Mode 5 [$t_4$, $t_5$] [Fig. 5(e)]: At $t_4$, $v_{c1}$ rises to $V_{c2}$ and $v_{c2}$ decays to zero. The body diode $D_2$ conducts and $S_2$ turns on under zero-voltage condition. The gate-to-source voltage of $Q_1$ is clamped to zero through $S_2$.

6) Mode 6 [$t_5$, $t_6$] [Fig. 5(f)]: At $t_5$, $v_{c4}$ rises to $V_{c1}$ and $v_{c3}$ decays to zero. The body diode $D_3$ conducts and $S_3$ turns on under zero-voltage condition. The gate-to-source voltage of $Q_2$ is clamped to $V_{c1}$ through $S_3$.

*B. Drive Circuit Loss Analysis*

Basically, the two current-source drivers (#1 and #2) are similar in the driver losses except for different inductor peak currents. For each of them, the drive loss includes: 1) the resistive loss and gate drive loss of switches ($S_1$- $S_4$); 2) the loss of the resonant inductor ($L_{r1}$ and $L_{r2}$); 3) the resistive loss caused by the internal gate mesh resistance of the power MOSFETs.

From the volt-second balance condition across the resonant inductor, the DC voltage $v_{cb}$ across the blocking capacitor $C_b$ is derived as Equation (1)

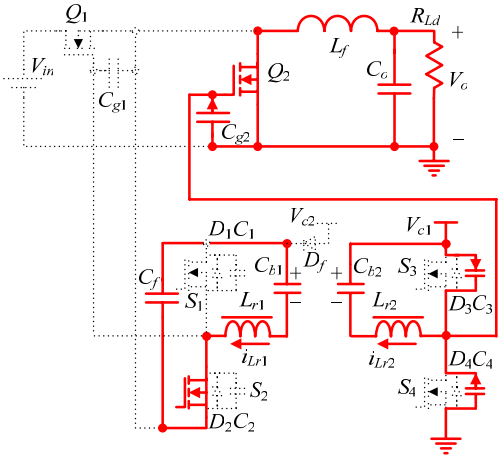
$$v_{Cb} = (1-D)\cdot V_c \tag{1}$$

where $D$ is the duty cycle of $S_1$, $V_c$ is the drive voltage.

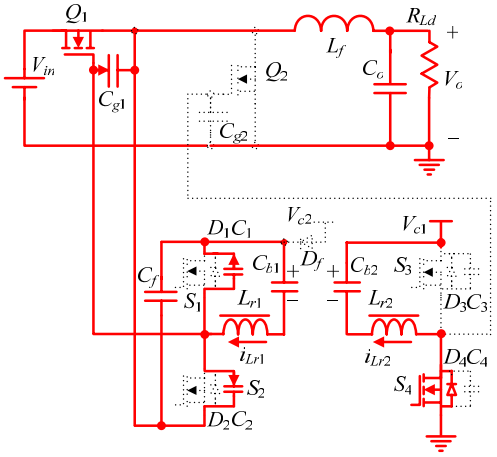
The relationship of the inductor value $L_r$ and the peak inductor current $I_{Lr\_pk}$ is given by Equation (2)

$$L_r = \frac{V_c \cdot D \cdot (1-D)}{2 \cdot I_{Lr\_pk} \cdot f_s} \tag{2}$$

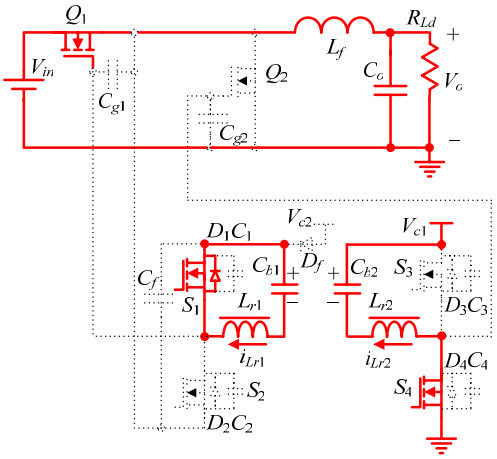
where $D$ is the duty cycle of $S_1$, $V_c$ is the drive voltage and $f_s$ is the switching frequency. By choosing the proper peak inductor current (drive current for MOSFET), the resonant inductor value can be obtained by Equation (2).



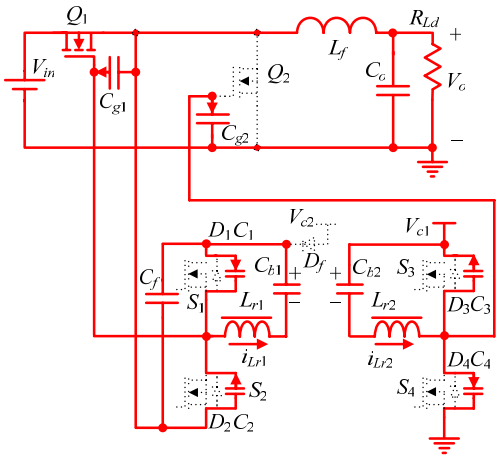

(a) [$t_0$, $t_1$]



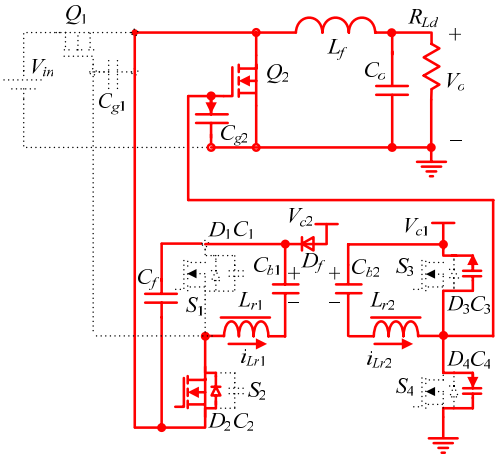

(b) [$t_1$, $t_2$]



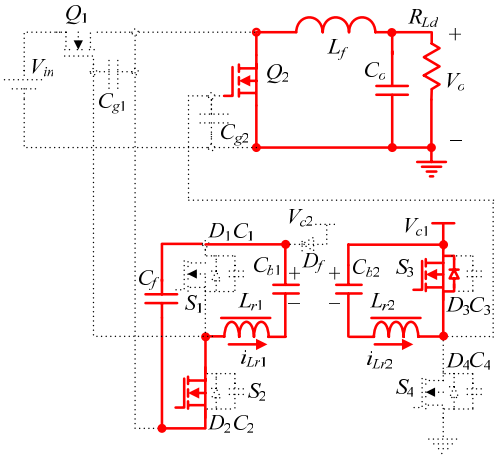

(c) [$t_2$, $t_3$]




(d) [$t_3$, $t_4$]




(e) [$t_4$, $t_5$]




(f) [$t_5$, $t_6$]

Fig. 5 Equivalent circuits of operation

The inductor current waveform indicated in Fig. 2 can be regarded as a triangular waveform since the charging/ discharging time [$t_0$, $t_2$] and [$t_3$, $t_5$] are very small and can be neglected. Therefore, the RMS value of the inductor current $I_{Lr\_RMS}$ is $I_{Lr\_pk}/\sqrt{3}$.

Take driver #1 as an example. The RMS currents flowing through the switches $S_1$ and $S_4$ can be derived as

$$I_{s1\_RMS} = I_{Lr\_pk1} \cdot \sqrt{\frac{D}{3}} \tag{3}$$

The RMS currents flowing through switches $S_2$ is

$$I_{s2\_RMS} = I_{Lr\_pk1} \cdot \sqrt{\frac{1-D}{3}} \tag{4}$$

The conduction loss of $S_1$ and $S_2$ is expressed as

$$P_{cond} = I_{s1\_RMS}{}^2 \cdot R_{ds(on)} + I_{s2\_RMS}{}^2 \cdot R_{ds(on)} \tag{5}$$

Substituting (3) and (4) into (5) yields

$$P_{cond} = \frac{1}{3} \cdot I_{Lr\_pk1}{}^2 \cdot R_{ds(on)} \tag{6}$$

The copper loss of the inductor winding is expressed as

$$P_{copper} = R_{ac} \cdot I^2_{Lr\_RMS1} \tag{7}$$

where $R_{ac}$ is the AC resistance of the inductor winding. $I_{Lr\_RMS1}$ is the RMS value of the inductor current. Core loss of the resonant inductor should be also included. The total inductor loss is given in Equation (8):

$$P_{ind} = P_{copper} + P_{core} \tag{8}$$

Both the charge and discharge currents flow through the internal gate mesh resistance $R_G$ of the power MOSFET and cause resistive loss. The charge and discharge current is the peak value of the inductor current. Thus the total loss caused by the internal resistance of the power MOSFET $Q_1$ during turn-on ($t_{on1}$) and turn-off ($t_{off1}$) is expressed as

$$P_{RG} = R_{G1} I^2_{Lr\_pk1} \cdot (t_{on1} + t_{off1}) \cdot f_s \tag{9}$$

where $R_{G1}$ is the internal gate resistors of $Q_1$ and $f_s$ is the switching frequency.

The gate drive loss of $S_1$ and $S_2$ is expressed as

$$P_{gate} = 2 \cdot Q_{g\_s} \cdot V_{gs\_s} \cdot f_s \tag{10}$$

where $Q_{g\_s}$ is the total gate charge of a drive switch and $V_{gs\_s}$ is the drive voltage, which is typically 5V.

In conclusion, the total loss of the gate drive circuit of #1 is expressed as

$$P_{Drvie} = P_{cond} + P_{gate} + P_{ind} + P_{RG} \tag{11}$$

### C. Optimal Design

One advantage of this new drive circuit is that it can drive the control MOSFET and the synchronous MOSFET independently with different gate drive currents for optimal design.

For the control MOSFET $Q_1$, this involves a tradeoff between the switching loss reduction and the drive circuit loss. Following optimal design procedure based on the analytical loss model in [16], the gate drive current can be decided and then the inductor value is calculated according to Equation (2).

For the synchronous rectifier MOSFET $Q_2$, this involves a tradeoff between body diode conduction loss and gate drive loss. The body diode conduction loss can be estimated using Equation (12).

$$P_{body\_Q2} = V_{body\_Q2} \cdot I_o \cdot f_s \cdot t_{body} \tag{12}$$

In Equation (12), $t_{body}$ is body diode conduction time and it can be estimated by Equation (13). Equation (13) assumes that the body diode will conduct during the interval when the gate voltage is between the threshold and until the gate voltage is large enough so that $R_{ds(on)}$ of the synchronous MOSFET is less than about 20mOhms, which means the voltage drop across the channel is less than the body diode drop. The values for $Q_{gQ2}(V_{20\text{mohm}})$ and $Q_{gQ2}(V_{thQ2})$ can be estimated using the MOSFET manufacturer datasheet and the body diode conduction time can be calculated as

$$t_{body} = 2\left[\frac{Q_{gQ2}(V_{20mohm}) - Q_{gQ2}(V_{thQ2})}{I_{gQ2}}\right] \quad (13)$$

Using $P_{Drive}$ given in Equation (11), and $P_{body\_Q2}$ given by (12), the sum of the two loss components can be plotted as $P_{optimal}$ and the optimal gate current, $I_{G\_Q2}$ can be determined from the graph (at the minimum point of $P_{Optimal}$). For the given application and parameters in the experimental results section, the curves are given in Fig. 6. In Fig. 6, the optimal gate current is 1.1A.

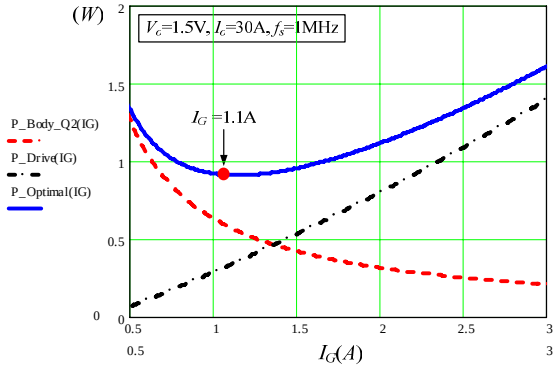



Fig. 6 Principle of Operation Optimization curves for the synchronous rectifier MOSFET Q2; power loss vs. gate current

### D. *Application Extension*

The proposed new gate drive circuit can also be used to drive two MOSFETs in a leg of half-bridge topology or full-bridge topology to achieve the switching loss reduction and gate energy savings as shown in Fig. 7.

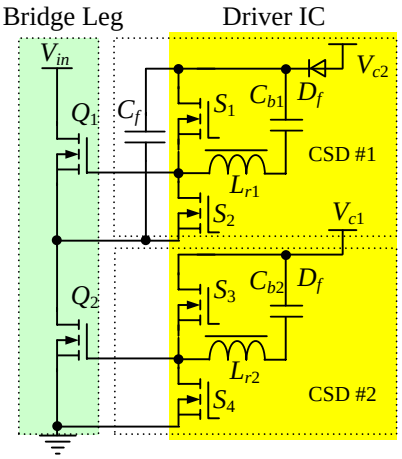



Fig. 7 Bridge leg with the new current-source driver

## III. New Current-Source Gate Driver with Integrated Magnetics

It is observed from the waveforms of two inductor current $i_{Lr1}$ and $i_{Lr2}$ in Fig. 4 that $i_{Lr1}$ is almost a mirror image about the time axis of $i_{Lr2}$, which has the very good ripple cancellation effect of magnetic flux. This makes the inductors integration possible.

Fig. 8 shows the proposed current-source gate driver with integrated magnetics. It is noted that the references of two drivers do not need to be the same.

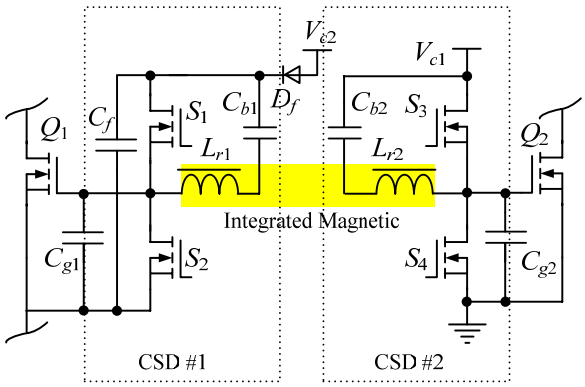



Fig. 8 Proposed current-source driver with integrated inductor

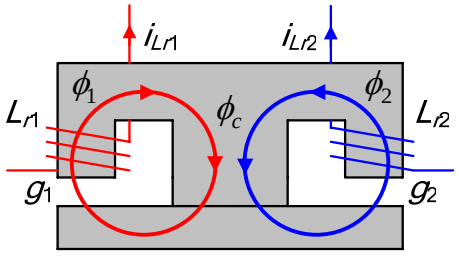



Fig. 9 Integrated inductor structure

Fig. 9 gives one integrated inductor structure for current-source driver circuits. The two resonant inductors ($L_{r1}$ and $L_{r2}$) are built on the two outer legs of one E-I core with different air gaps ($g_1$ and $g_2$) respectively. The fluxes $\Phi_1$ and $\Phi_2$ in the two outer legs generated by the two windings based on the directions of the currents will all flow through the center leg, which is a low-reluctance magnetic path with no air gap. Though $L_{r1}$ and $L_{r2}$ are built on the same E-I core, there is no interaction between the two flux loops of $\Phi_1$ and $\Phi_2$ and there is no coupling effect between $L_{r1}$ and $L_{r2}$.

Therefore, the principle of operation of the driver circuits with the integrated inductor does not change. But the core number is reduced to one instead of two. Another benefit using the integrated inductor is that the flux $\Phi$ ( $\Phi=\Phi_1+\Phi_2$) in the center leg has smaller ripples owing to the flux ripple cancellation effect of the current $i_{Lr1}$ and $i_{Lr2}$ as shown in Fig. 10. The smaller flux ripples help to reduce the core losses in the center leg at high frequency.

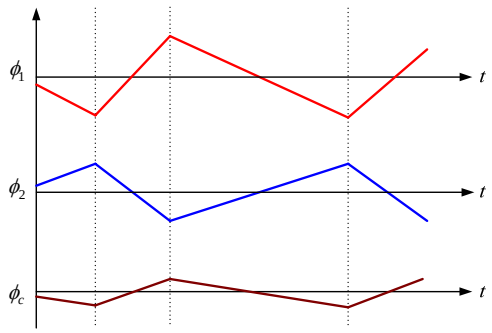



Fig. 10 Flux ripple cancellation effect

## IV. Experimental Results and Discussion

In order to verify the advantages of the new current-source gate drive circuit, a synchronous buck converter with the proposed driver was built. The specifications are as follows: input voltage $V_{in}$=12V; output voltage $V_o$=1.5V; output current $I_o$=30A; switching frequency $f_s$=1MHz; gate driver voltage $V_{c1}$=$V_{c2}$=8V. The PCB uses six-layer 2 oz copper. The components used in the circuit are listed as follows: $Q_1$: Si7860DP; $Q_2$: Si7336ADP; output filter inductance: $L_f$=330nH; resonant inductors: $L_{r1}$=1.0uH and $L_{r2}$=1.2uH.

Fig. 11 shows the gate drive signals $v_{gs\_Q1}$ (control MOSFET) and $v_{gs\_Q2}$ (synchronous MOSFET). It is observed that the dead time between two gate signals is minimized to reduce the body diode conduction. It is also observed that $v_{gs\_Q1}$ is very smooth and no miller plateau is observed as the miller charge is removed fast with the constant charging current. Moreover, the rise time and fall time of $v_{gs\_Q1}$ is less than 15ns, which means quick switching speed. It is also noted that owing to the gate energy recovery, 8V drive voltage is used to reduce the $R_{ds\_(on)}$ and the conduction loss of the synchronous MOSFET further.

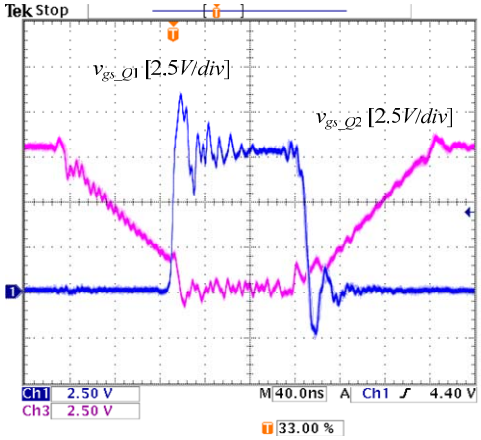



Fig. 11 The gate signals $v_{gs\_Q1}$(control FET) and $v_{gs\_Q2}$(synchronous FET)

Fig. 12 and Fig. 13 show the resonant inductor current $i_{Lr1}$ and $i_{Lr2}$ with discreet inductors and integrated inductors respectively. It is observed that the mirror relationship between $i_{Lr1}$ and $i_{Lr2}$ leads to the feasibility of inductor integration and lower core loss due the magnetic flux cancellation effect. In addition, the integrated inductor does not change the operation of the drive circuits.

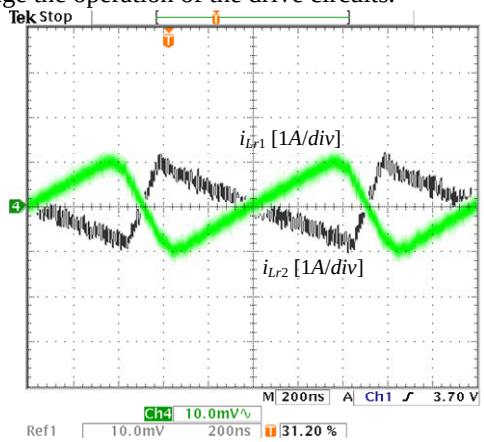



Fig. 12 Waveforms of resonant inductor currents (discreet resonant inductors)

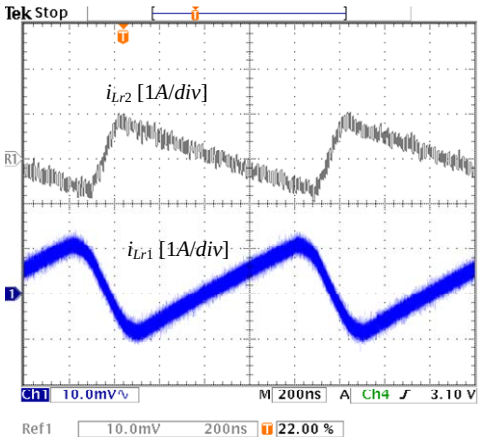



Fig. 13 Waveforms of resonant inductor currents (with integrated inductors)

A benchmark of a synchronous buck converter with the same parameters and conventional gate driver was built. A predictive gate drive UCC 27222 from Texas Instruments was used as the conventional voltage-source gate driver.

Fig. 14 shows the measured efficiency comparison for the current-source gate driver and the conventional gate driver at 1.5V output. It is observed that at 20A, the efficiency is improved from 84% to 87.3% (an improvement of 3.3%) and at 30A, the efficiency is improved from 79.4% to 82.8% (an improvement of 3.4%). The current-source driver with one integrated inductor achieves the similar efficiency as the driver with two discrete inductors.

Fig. 15 shows the converter power loss comparison for the resonant gate driver and the conventional driver. It is noted that 30A load, the proposed current source gate driver saves approximately 2.2W (a reduction of 23%) compared to the conventional driver. This loss savings is significant for a multi-phase VRs. For example, in five phase VRs, the total loss savings would be 11W.

Another interesting observation is that if the power loss per phase is limited to 9.5W, the buck converter with conventional gate drive can only provide 26A output current, while the buck converter with current source gate driver can provide

30A (an improvement of 15%). In other words, if the total output current is 120A, we need 5 phases (120A/26A per phase) for the conventional gate driver and only 4 phases (120A/30A per phase) for the current source driver. This will yield a significant cost savings and space savings.

Fig. 16 shows the measured efficiency for the current-source driver at different output voltages and load currents.

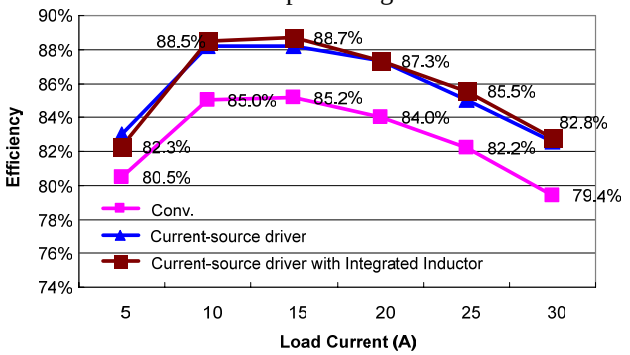



Fig. 14 Efficiency comparison at1.5V/ 30A/ 1MHz

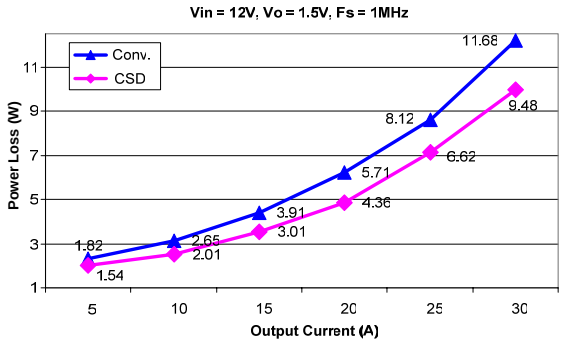



Fig. 15 Power loss comparison at 1.5V/ 30A condition; Top: Conventional driver (Conv), bottom: Current-source driver (CSD)

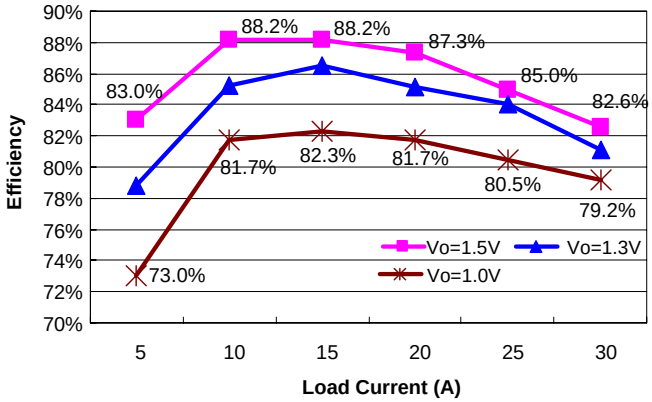



Fig. 16 Efficiency with different output voltages

## V. Conclusion

In this paper, a new current-source MOSFET gate drive circuit is proposed for a synchronous buck converter. The proposed gate driver is able to drive the control MOSFET and the synchronous MOSFET independently with different drive currents for optimal design.

The new drive circuit maintains the following advantages: 1) gate energy recovery; 2) significant switching loss reduction; 3) reduced body diode losses and reverse recovery losses; 4) ZVS of all the driver switches.

The improved current-source driver using integrated inductors is also presented to reduce the magnetic core number and the core loss due to magnetic flux cancellation effect.

The experimental results prove the advantages of the new drive circuit and a significant efficiency improvement has been achieved. At 1.5V output, the new driver improves the efficiency from 84% using a conventional driver to 87.3% (an improvement of 3.3%) at 20A, and at 30A, from 79.4% to 82.8% (an improvement of 3.4%).

Overall, the new driver approach is very promising from the standpoints of both performance and cost-effectiveness.

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