# Controlled Current Source Circuit (CCSC) for Reduction of Output Voltage Overshoot in Buck Converters

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*Abstract*— **In this paper, an auxiliary circuit is presented to improve the dynamic response of a Buck converter. Since it is well established that for typical voltage regulator applications, voltage overshoots (due to step-down load transients) are much larger than voltage undershoots (due to step-up load transients), the goal of the proposed method is to reduce the former. The circuit only functions during step-down load transients and operates by rapidly transferring excess load current from the output of the Buck converter to its input. Unlike previous unloading auxiliary circuits, the proposed method uses a controlled current source circuit (CCSC) to remove a constant regulated current from the output. The CCSC has the following advantages over previous circuits: a) predictable behavior allowing for simplified design, b) inherent over-current protection, c) low peak current to average current ratio allowing for use of smaller components. Through selection of the auxiliary current, it is possible to obtain a balanced overshoot/undershoot response for a Buck converter, significantly reducing the required output capacitance. In this paper, it is shown through analysis, simulation and experimental results that for a modest increase in component cost, a large reduction of voltage overshoot and output capacitor requirement can be realized.**

## I. INTRODUCTION

For microprocessors and other digital devices, the DC-DC converter standard has typically been the voltage-mode controlled Buck converter due to its simplicity and familiarity. Unfortunately, in order to adhere to transient voltage specifications, numerous bulk output capacitors must be utilized, driving up the cost of the converter and consuming valuable real estate. Therefore, research has been focused on alternatives to the standard voltage-mode controlled Buck in order to improve the dynamic performance of DC-DC converters.

A relatively inexpensive method to improve the dynamic response of a Buck converter is to improve its controller. In [1]-[3], various control schemes are presented which improve the transient response (due to a rapid load variation) of a Buck converter, to its optimal level. By using second-order switching surfaces [3] or energy balancing techniques [1]-[2], it is possible to minimize the settling time and the voltage overshoot/undershoot due to a load transient. However, while employing the so-called "optimal control" methods, it is clear that the limiting factor of dynamic performance becomes the inductor current slew rate. In fact, it is demonstrated in [2]-[3] that for low duty cycle conversion applications, the voltage overshoot caused by a step-down load current transient may be more than 5 times as large as the corresponding voltage undershoot caused by a positive current step of equal magnitude. Therefore, to adhere to voltage specifications, capacitor selection must be based on the larger voltage overshoot condition.

In order to address the large overshoots typical of voltage regulator module (VRM) applications, numerous auxiliary circuits have been proposed for the Buck converter [4]-[9].

In [4]-[5], a transformer is connected across the impedance of the output trace of a Buck converter in order to inject/absorb excess load current to improve the dynamic performance.

In [6], an auxiliary switch is used to bypass the output inductor of a Buck converter in order to provide a very low inductance path to the output. The switch remains full-on for the duration that the output voltage deviation exceeds a pre-determined threshold.

An auxiliary switch in series with a small inductor is utilized in [7] to recover excess current to the input during step-down load transients. The circuit also provides a low-impedance auxiliary path for step-up load transients. The auxiliary circuit is controlled using a differentiator in an attempt to instantaneously track the capacitor current.

In [8], the output of an isolated DC-DC converter is connected through an auxiliary circuit (similar to [7]) to a voltage rail (fed by the rectified voltage of the secondary winding) in order to inject/absorb excess current. The auxiliary circuit is controlled linearly based on the magnitude of the voltage overshoot.

An auxiliary circuit (similar to [7]) is connected to the output of a Buck converter in [9]. The switch is turned full-on for the duration that the output voltage deviation exceeds a pre-determined threshold.

While all the aforementioned topology modifications improve the dynamic response of a DC-DC converter during a load transient, they suffer from at least one of the following conditions:

1. Complicated transformer design due to high-frequency operation [4]-[5]
2. Auxiliary switch control susceptible to noise caused by auxiliary switching [7]

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3. Unpredictable auxiliary switching frequencies [7], [9]
4. No direct current-mode control of the auxiliary circuit resulting in unpredictable and potentially damaging currents [6], [8]-[9]; this may be particularly problematic for [6] which relies on the trace and switch inductance to limit the auxiliary current slew rate
5. High auxiliary peak current to average current ratio resulting in necessity of relatively large auxiliary switches for desired dynamic performance [7]-[9]

In this paper, an auxiliary controlled current source circuit (CCSC) is proposed which significantly improves the voltage overshoot due to a step-down load transient by rapidly transferring excess inductor current from the output of a Buck converter to the input. The CCSC operates at high frequency, with a controlled, constant current. A low peak current to average current ratio allows for the use of a small MOSFET (SOT-23) and a small diode for similar dynamic response improvements demonstrated in the aforementioned papers. Since the auxiliary current is known and constant, the design of the converter is simplified. A converter utilizing the CCSC (for step-down load transients) and an optimal control method, as proposed in [1]-[3], (for step-up load transients) would yield superior dynamic performance with minimal output capacitor requirements.

## II. Concept of Operation

The CCSC can be modeled as a current source drawing current from the output of the Buck converter and transferring it to the input of the Buck converter. Figure 1a) shows the model of the proposed method. The CCSC is only active during step-down load current transients. Typically, $I_{aux}$ has a small ripple and is controlled based on a preferred constant value. Figure 1b) shows one possible implementation of the CCSC, used in this paper. An alternate implementation would involve using a second MOSFET (in lieu of $D_{aux}$) for synchronous switching.

The CCSC is controlled using a peak-current mode, constant off-time scheme as shown in Figure 2. Since it is assumed that the input voltage and the output voltage of the Buck converter remain relatively constant during a transient event, the control scheme will produce a constant average current through the CCSC. The auxiliary current can be sensed using the $R(ds)_{on}$ of the auxiliary MOSFET $Q_{aux}$, a current sense resistor or an RC network in parallel with the auxiliary inductor $L_{aux}$. In this paper, a small current sense resistor was employed.

$L_{aux}$ is typically chosen to be 1/10 of $L_o$. Due to the short duration of operation, $Q_{aux}$ can be chosen based on

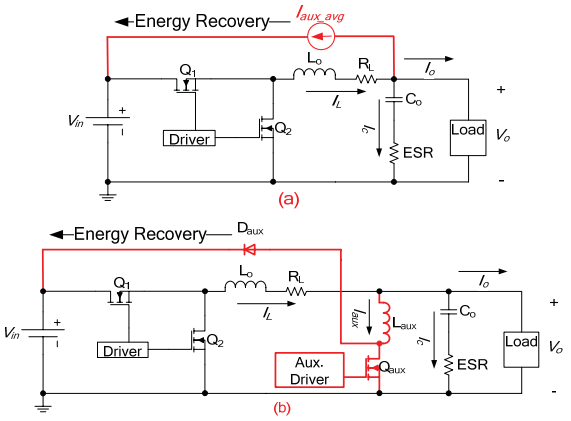


Figure 1 a) Model of CCSC; b) MOSFET-diode implementation of CCSC

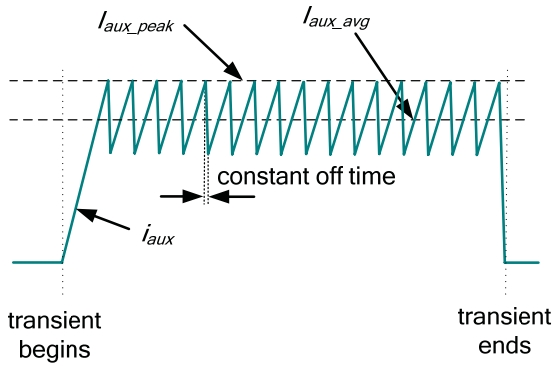


Figure 2 Peak-current mode, constant off-time control of CCSC

its "pulsed" current limit rather than its continuous current limit (allowing for the use of small SOT-23 MOSFETs for $I_{aux\_avg} < 15A$).

Since the duty cycle of the diode is typically very small (<15%), a small Schottky diode may be used.

Figure 3 depicts the operation of the CCSC in comparison to a control method which turns the auxiliary current "full-on" ($d$ = 100%) for the duration of the transient. For "full-on" operation, the auxiliary inductor value may need to be increased in order to limit the auxiliary current from reaching excessive levels. The CCSC's current is controlled, thus a small inductor can be safely used. It is clear that, for a fixed average auxiliary current and operation time, the proposed method operates with a much smaller peak auxiliary current. This allows for the use of a smaller package MOSFET. Also, due to the controlled, high frequency operation, a smaller auxiliary inductor may also be used. In addition, it is shown in Figure 3 that for a fixed average auxiliary current and operation time, the CCSC provides a significant improvement in voltage overshoot reduction by removing excess capacitor charge at a faster rate.

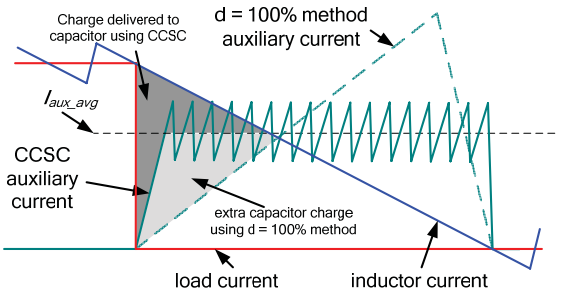


Figure 3 CCSC vs. d = 100% method during a negative load step

As mentioned, the CCSC uses peak-current, constant off-time control to maintain a constant average current. Selection of the peak auxiliary current $I_{aux\_peak}$ and the constant off time $t_{off}$ will determine the average auxiliary current $I_{aux\_avg}$ and the auxiliary switching frequency $f_{aux}$, as calculated in (1) and (2) respectively.

$$I_{aux\_avg} = \frac{2 \cdot I_{aux\_peak} \cdot L_{aux} - (V_{in} + V_{diode} - V_o) \cdot t_{off}}{2 \cdot L_{aux}} \quad (1)$$

$$f_{aux} \approx \frac{V_o - Rds_{on} \cdot I_{aux\_avg}}{t_{off}(V_{in} + V_{diode} - R(ds)_{on\_aux} \cdot I_{aux\_avg})} \quad (2)$$

The block diagram of the CCSC is illustrated in Figure 4.

Referring to Figure 5 and Figure 6, the operation of the CCSC can be described in three steps:

*$t_0$: Step-down load transient detected (Case #1 and Case #2)*

During steady-state operation, the Buck converter is controlled by a conventional controller (such as a voltage-mode or a current-mode controller).

The proposed method estimates the capacitor current by using a trans-impedance amplifier configuration, fed by the output voltage, as shown in Figure 4. A low-pass filter connected to the input of the capacitor current sensor is used to attenuate the ESL noise caused by high-frequency auxiliary switching. When the capacitor current exceeds a pre-determined threshold, the CCSC is activated and the duty cycle of $Q_1$ is set to 0%. The control voltage of the conventional controller is held constant to prevent loop upsetting.

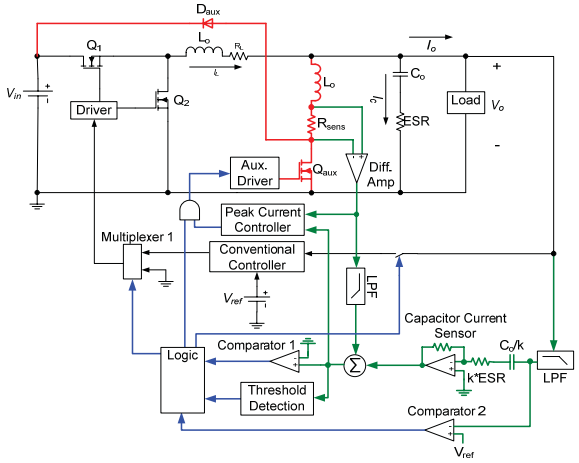


Figure 4 Block diagram of CCSC control

*$t_a$: Reduce auxiliary peak current (Case #2 only)*

Following relatively small load current steps, it is possible that the output voltage will equal the reference voltage before the inductor current equals the new load current. In this case, the average auxiliary current is reduced and held constant at $I_{aux\_avg} = 0.5(i_{L(ta)}-I_{o2})$. This may be accomplished by using a simple sample/hold circuit. $i_L$-$I_{o2}$ is estimated by adding the output of the capacitor current estimator to the filtered output of the auxiliary current sensing amplifier, as shown in Figure 4. Case #2 is illustrated in Figure 6. This method will ensure that the output voltage does not significantly deviate from the reference voltage from point $t_a$ to $t_1$.

*$t_1$: End of transient (Case #1 and Case #2)*

When $i_L$-$I_{o2} = 0$, the CCSC is deactivated and $Q_1$ and $Q_2$ are controlled by the conventional controller.

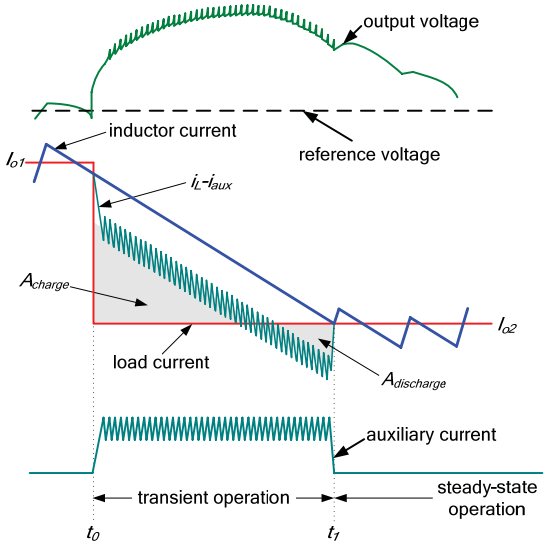


Figure 5 CCSC operation following a negative load current step (Case #1)

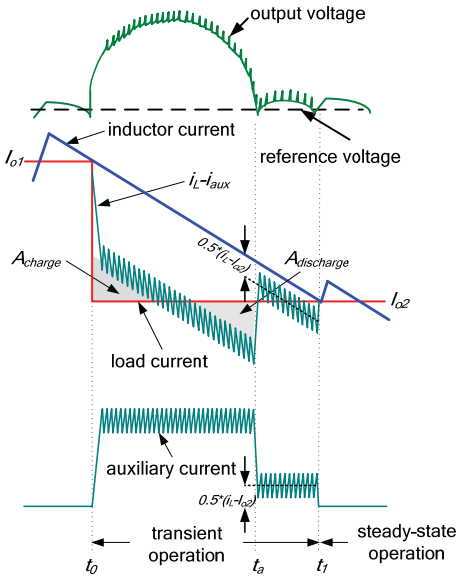


Figure 6 CCSC operation following a negative load current step (Case #2)

## III. Loss Analysis

In this section, the conduction and switching losses, caused by the CCSC, are analyzed and evaluated for the designed prototype. It is important to note that the CCSC is only activated during load current step-down transient events; therefore, for scenarios in which load transients occur at low frequencies, the CCSC loss will become insignificant.

### A. Conduction Loss

There are three main sources of conduction loss pertaining to the CCSC: a) the auxiliary inductor $L_{aux}$, b) the auxiliary FET $Q_{aux}$, and c) the auxiliary diode $D_{aux}$.

In order to calculate the conduction loss of the inductor, the root mean square (RMS) current must first be calculated. The auxiliary inductor RMS current (a DC current with a superimposed linear ripple) is calculated using (3).

$$I_{L\_aux(rms)} = I_{aux\_avg}\sqrt{1+\frac{1}{3}\left(\frac{I_{aux\_pk-pk}}{2\cdot I_{aux\_avg}}\right)^2} \tag{3}$$

$I_{aux\_avg}$ is previously calculated in (1) and $I_{aux\_pk\text{-}pk}$ is calculated in (4).

$$I_{aux\_pk-pk} = t_{off}\frac{V_{in}+V_{d\_aux}-V_o}{L_{aux}} \tag{4}$$

By calculating the RMS auxiliary current in (3), the inductor conduction loss can be calculated using (5).

$$Pcon_{L\_aux} = I_{L\_aux(rms)}{}^2\cdot R_{L\_aux} \tag{5}$$

The RMS current for the auxiliary FET and the auxiliary diode (a pulsating current with a linear ripple) can be calculated using (6) and (7) respectively.

$$I_{Q\_aux(rms)} = I_{aux\_avg}\sqrt{D_{aux}}\sqrt{1+\frac{1}{3}\left(\frac{I_{aux\_pk-pk}}{2\cdot I_{aux\_avg}}\right)^2} \tag{6}$$

$$I_{D\_aux(rms)} = I_{aux\_avg}\sqrt{1-D_{aux}}\sqrt{1+\frac{1}{3}\left(\frac{I_{aux\_pk-pk}}{2\cdot I_{aux\_avg}}\right)^2} \tag{7}$$

$D_{aux}$ can be calculated using (8).

$$D_{aux} = 1 - f_{aux}t_{off} \tag{8}$$

$f_{aux}$ is previously estimated in (2). The conduction loss for the auxiliary FET and auxiliary diode can be calculated using (9) and (10) respectively.

$$Pcon_{Q\_aux} = I_{Q\_aux(rms)}{}^2\cdot R(ds)_{on\_aux} \tag{9}$$

$$Pcon_{Q\_aux} = I_{Q\_aux(rms)}\cdot V_{d\_aux} \tag{10}$$

The resultant conduction loss for the CCSC can be calculated using (11).

$$Pcon_{CCSC} = D_{CCSC}\cdot(Pcon_{L\_aux} + Pcon_{Q\_aux} + Pcon_{D\_aux}) \tag{11}$$

$D_{CCSC}$ represents the time ratio that the CCSC is activated. As previously mentioned, the on time of the CCSC is equal to the time required for the inductor current to decrease to the new load current. The $D_{CCSC}$ can be calculated using (12).

$$D_{CCSC} = f_{I_o}\frac{\Delta I_o\cdot L_o}{V_o} \tag{12}$$

$f_{Io}$ equals the frequency at which the load current varies and $\Delta I_o$ equals the magnitude of the load current change.

### B. Switching Loss

The switching loss of the auxiliary FET is analyzed in this sub-section. Since a Schottky diode is utilized, it is assumed that the switching loss of the diode is small compared to the FET switching loss and the total conduction loss. The switching loss for the auxiliary FET can be calculated using (13).

$$Psw_{Q\_aux} = \frac{1}{2}f_{aux}V_{in}\left(t_{rise}I_{on} + t_{fall}I_{off}\right) \tag{13}$$

$t_{rise}$ and $t_{fall}$ equals the typical rise time and fall time of the auxiliary FET respectively. $I_{off}$ equals the instantaneous auxiliary current when $Q_{aux}$ is turned off which is equal to the chosen peak auxiliary current. $I_{on}$ equals the instantaneous auxiliary current when $Q_{aux}$ is turned on and can be calculated using (14). The resultant switching loss for the CCSC is calculated in (15).

$$I_{on} = I_{aux\_peak} - t_{off}\frac{V_{in}+V_{d\_aux}-V_o}{L_{aux}} \tag{14}$$

$$Psw_{CCSC} = D_{CCSC}\cdot Psw_{Q\_aux} \tag{15}$$

A Buck converter was evaluated with the following parameters: $V_{in}$ = 12V, $V_o$ = 1.5V, $L_o$ = 1uH, $f_s$= 400kHz, $L_{aux}$ = 100nH, $R_{L\_aux}$ = 0.3mΩ, $f_{aux}$ = 1.8MHz, *ESR* = 0.5mΩ, *ESL* = 100pH. A small (SOT-23) Fairchild FDN359BN was used for $Q_{aux}$. The MOSFET parameters are: $R(ds)_{on}$ = 30mΩ, $t_{rise}$ = 5ns, $t_{fall}$ = 2ns. It should be noted that a larger MOSFET can easily be utilized for better efficiency. A Schottky diode with a forward voltage of $V_{d\_aux}$ = 0.32V was used for $D_{aux}$. The loss analysis was performed for 10A load steps at varying load frequencies, as shown in Figure 7.

For a 15W converter, it is shown that at load frequencies of 50kHz, the power consumption of the CCSC is approximately 3.74% of the output power. The power consumption of the CCSC may be improved by increasing the size of the auxiliary MOSFET and/or implementing synchronous switching.

For example, if the auxiliary MOSFET $R(ds)_{on}$ resistance were reduced to 7mΩ, the power consumption would be reduced to 2.52% of the output power at a 50kHz load frequency. In this scenario, the diode contributes to the majority of the conduction loss.

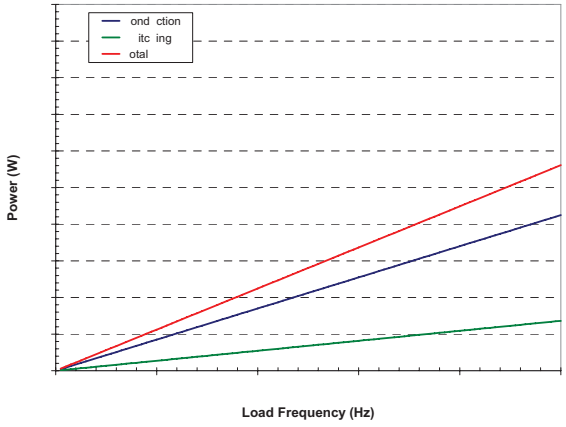


Figure 7 CCSC power loss for varying load step frequencies

## IV. Design Example and Simulation Results

Neglecting ESL, the best possible overshoot of a Buck converter undergoing a negative load step (without the CCSC) can be calculated using (16). The overshoot of a Buck converter with the CCSC can be estimated by (17).

$$\Delta v_o = \frac{ESR^2 \cdot C^2 \cdot V_o^2 + \Delta I_o{}^2 L^2}{2V_o \cdot L \cdot C} \tag{16}$$

$$\Delta v_o\_improved \approx \frac{ESR^2 \cdot C^2 \cdot V_o^2 + (\Delta I_o - I_{aux\_avg})^2 L^2}{2V_o \cdot L \cdot C} + \frac{I_{aux\_avg}{}^2 \cdot L_{aux}}{2V_o \cdot C} \tag{17}$$

Figure 8 plots the expected voltage overshoot, for various values of $I_{aux\_avg}$ and $C_o$, of a converter undergoing a 10A step-down load transient. The converter parameters are identical to that of the converter analyzed in Section III. For reference, the dashed blue curve refers to the best possible calculated voltage undershoot due to a positive 10A load step.

Referring to Figure 8, with no overshoot reduction, in order to limit the voltage overshoot to 50mV, an output capacitance of 650uF is required. However, by using the CCSC with $I_{aux\_avg}$ = 4.8A, the required output capacitance is reduced to approximately 190uF (a reduction of 71%). Larger auxiliary currents will yield better dynamic performance at the price of efficiency.

A Buck converter with an output capacitance of 650uF (without CCSC) undergoing a negative 10A step was simulated, as illustrated in Figure 9. For comparison, the converter analysed in Section III (with $C_o$ = 190uF, $I_{aux\_avg}$ = 4.8A) was simulated, as illustrated in Figure 10.

It is shown in Figure 10 that the capacitor ESL causes small high-frequency voltage spikes when using the CCSC. These spikes can be reduced by using an increased number of ceramic bypass capacitors in parallel.

In order to illustrate Case #2 (as previously mentioned in Section II), the aforementioned converter was simulated with a 7.5A negative load current step. A simulated occurrence of Case #2 is displayed in Figure 11. As shown, the auxiliary current is reduced when the output voltage returns to the reference voltage in order to prevent a large voltage undershoot before the inductor current equals the new load current.

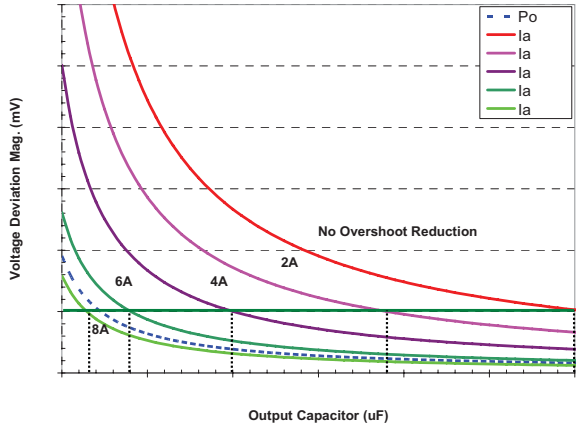


Figure 8 Calculated voltage deviation for various values of $I_{aux\_avg}$ and $C_o$

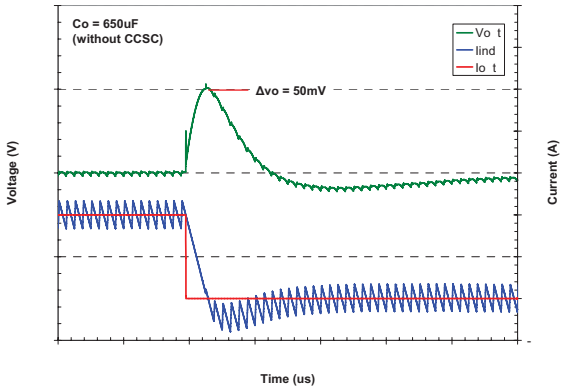


Figure 9 Buck converter (w/o CCSC), $C_o$ = 650uF

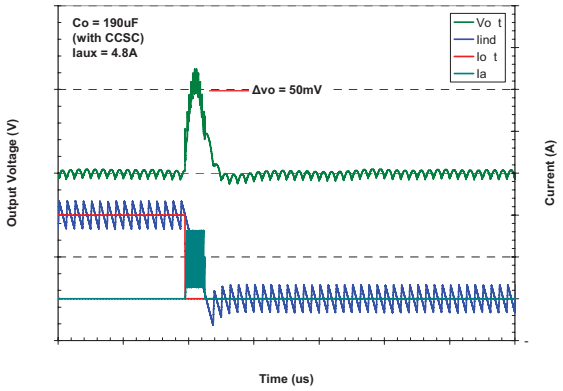


Figure 10 Buck converter (with CCSC, $I_{aux\_avg}$ = 4.8A), $C_o$ = 190uF

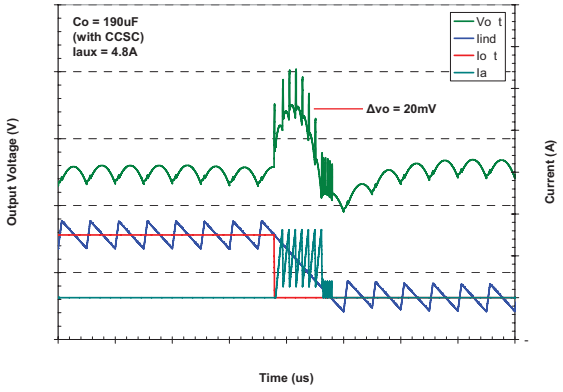


Figure 11 Case #2, Buck converter (with CCSC, $I_{aux\_avg}$ = 4.8A, $C_o$ =190uF)

## V. Experimental Results

A prototype of the converter analyzed in Section III (with $C_o$ = 190uF) was built and tested in order to verify functionality. The prototype was subjected to a 10A→0A step change with a slew rate greater than -100A/us.

For reference, Figure 12 illustrates the converter reaction to the aforementioned current step change with the CCSC disabled. As predicted by (16), the voltage overshoot is approximately 160mV.

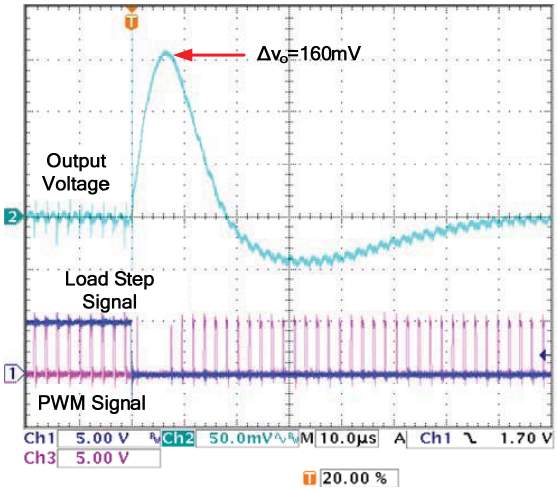


Figure 12 Output voltage response of a Buck converter undergoing a 10A→0A load step change (CCSC disabled)

Figure 13 illustrates the converter reaction to a 10A→0A current step with the CCSC enabled. The auxiliary frequency was measured to be $f_{aux}$ = 1.8-1.9MHz and the average auxiliary current was measured to be $I_{aux\_avg}$≈4.8A which is in correspondence to the desired specifications. As predicted by (17), the voltage overshoot is approximately 50mV.

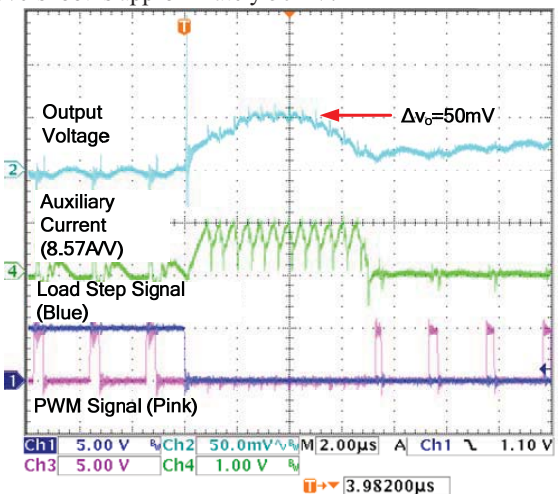


Figure 13 Output voltage response of Buck converter undergoing a 10A→0A load step change (CCSC enabled, $I_{aux\_avg}$ = 4.8A)

By utilizing the CCSC, the voltage overshoot of the Buck converter was reduced from 160mV to 50mV (a reduction of 69%).

## VI. Conclusion

For low duty cycle Buck applications, voltage overshoots tend to be much larger than voltage undershoots for load current transients of equal magnitude. Unfortunately, engineers must design for the larger overshoot criteria when choosing output capacitors. The proposed CCSC overshoot reduction method allows for a more balanced overshoot/undershoot response of a Buck converter, allowing an engineer to meet voltage criteria with fewer output capacitors. The circuit operates with a small MOSFET, diode and inductor. It has been shown through analysis, simulation, and experimental results that for a fixed voltage overshoot, the capacitor requirement can be reduced by 71%. By increasing the auxiliary current of the CCSC, the voltage overshoot can be further reduced.

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